1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0041595700	ENGINEERING RELEASED	2023-02-09

X2482 MLB

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44	84	MPMU: MISC CKT, VSS	T585_REF_PMU_STOWE_VALE_H15G_0.36.0	
45	85	MPMU: GPIO	T585_REF_PMU_STOWE_VALE_H15G_0.36.0	
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50	128	POWER: EXTERNAL SWITCHES	J404_MLB_4.24.0	
51	129	POWER: EXTERNAL LDOS	J404_MLB_4.24.0	
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59	137	SENSORS: POWER LOAD SIDE (2/3)	KEI_X2482_MLB 06/10/2022	
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85	197	SDCARD IO LS/BUF SUPPORT	T585_REF_SDCARD_GL9755_V2_0.13.0	
86	198	SDCARD POWER SUPPORT	T585_REF_SDCARD_GL9755_V2_0.13.0	
87	200	WIFI/BT: MODULE	T585_REF_WIRELESS_WILLAMETTE_0.30.0	
88	201	WIFI/BT: ANTENNA and GND	T585_REF_WIRELESS_WILLAMETTE_0.30.0	
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97	239	BCON CONNECTOR	J404_MLB_4.24.0	
98	242	SECDIS: LID ANGLE SENSOR	T585_REF_SECDIS_LAS_H14X_0.3.0	
99	243	SECDIS: SAK	T585_REF_SECDIS_H14X_0.9.0	
100	244	SECDIS: SUPPORT	PATRICK_X2482_MLB 02/01/2022	
101	245	AUDIO JACK CODEC	T585_REF_CODEC_CARLOW_1.6.0	
102	246	AUDIO AMPLIFIERS (1/2)	T585_REF_SPKRAMP_SN012776_3.9.0	
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REF DESIGNS AND PROJECTS X2482 SYNCS FROM

SOURCE PROJECT	SUB-DESIGN NAME	SUB-DESIGN PAGES	VERSION	HARD/ SOFT	SYNC_DATE/TIME
T585	REF_SOC_H15G	6-12,14,19,23-30,40,41	0.0.26	H	2022_08_17_09:54:38
T585	REF_SE_EOS	50	0.2.3	H	2022_09_09_10:45:36
T585	REF_CHARGER_WHAMOLA_MP_NEWFET	52,53	0.1.15	H	2022_09_20_15:52:06
T585	REF_VR_ICEMAN	57,58	1.55.0	H	2022_02_25_08:08:28
T585	REF_PMU_STOWE_VALE_H15G	77-85	0.37.0	H	2022_09_22_11:34:26
T585	REF_VR_5V_TPS62130	122	0.22.0	H	2022_08_10_18:16:52
T585	REF_IMU_SOVEREIGN	144	0.16.0	H	2022_06_23_12:17:32
T585	REF_USBC_LFKA_MACAW_DUAL_KIS	150-157,159	0.33.0	H	2022_09_19_10:58:48
T585	REF_USBC_VR_LT8642_1	158	0.11.0	H	2022_02_25_17:49:50
T585	REF_HDMI_COBRA	176-178	0.59.0	H	2022_11_23_11:16:05
T585	REF_SDCARD_GL9755_V2	195-196,198	0.13.0	H	2022_05_20_14:58:12
T585	REF_WIRELESS_WILLAMETTE	201	0.30.0	H	2023_01_24_17:43:22
T585	REF_STORAGE_S5E_MARK2	220,221	0.26.0	H	2022_03_15_10:36:33
T585	REF_PANELPWR_2D	237	0.9.0	H	2022_06_23_12:18:16
T585	REF_BLC_LUXE	238	0.36.0	H	2022_07_07_11:22:06
T585	REF_SECDIS_LAS_H14X	242	0.3.0	H	2021_12_02_13:27:13
T585	REF_SECDIS_H14X	243	0.9.0	H	2022_07_07_11:22:15
T585	REF_CODEC_CARLOW	245	1.6.0	H	2021_12_02_13:30:46
T585	REF_SPKRAMP_SN012776	246,247	3.9.0	H	2023_01_24_17:42:17
T585	REF_TPAD_IF_PKG_LARGE	253	0.15.0	H	2022_09_26_11:04:49

REF DESIGNS X2482 DOES NOT SYNC FROM

REF_PMU_STOWE_VALE_H15G	CSA 77-85 ARE SYNCED, BUT DRI IS BRANCHING AND MAKING CHANGES ON CSA 86-88, SO THOSE 3 ARE NOT SYNCED
REF_HDMI_COBRA	CSA 175. BROKE SYNC TO ADD CORRECT CONNECTOR, SAME AS X2371 <RDAR://88448603>
REF_KBD_34PIN	CSA 251. BROKE SYNC AFTER 0.4.0 PER WUDI REQUEST IN <RDAR://88595486>
REF_BLC_BEN_KBD_ONLY	CSA 250. BROKE SYNC AFTER 0.7.1 TO FLIP LEVEL SHIFTER DIR <RDAR://88843535>
REF_HDMI_COBRA	CSA 179. BROKE SYNC AFTER 4.3.0 TO ADD RESISTORS PER RDAR://101100575 AND RDAR://101960830
REF_SDCARD_GL9755_V2	CSA 197. BROKE SYNC AFTER 4.1.0 TO CHANGE I2C PULL-UPS PER RDAR://101549949

REF DESIGNS X2482 SYNCS FROM, BUT THEN MUST MAKE MODIFICATION TO

REF_HDMI_COBRA	CSA 177 DPRX* GND VOIDS NEED TO BE DELETED PER <RDAR://99397066>
REF_WIRELESS_WILLAMETTE	CSA 200 PCIE WIFI PLACE NEARS MUST BE UPDATED TO ALLOW PROPER PLACEMENT FOR OPTIMAL EYE MEASUREMENT
REF STORAGE_S5E_MARK2	CSA 220/221 GND VOIDS MUST BE DELETED FOR PCIE_NAND0_R2D/D2R
REF_PANELPWR_2D	CSA 237 CHANGE UP710.3 TO PMU_SYS_ALIVE_1V8
REF_PMU_STOWE_VALE_H15G	CSA 77,84 CHANGE C7700,C7701,C8430,C8431 TO 138S00078

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BOTTOM STANDOFFS

860-01714
ALLOW_APPLE_PREFIX=BS
BS0450
2.7X1.8R-1.4ID-1.7H-SM

860-01714
ALLOW_APPLE_PREFIX=BS
BS0451
2.7X1.8R-1.4ID-1.7H-SM

860-01714
ALLOW_APPLE_PREFIX=BS
BS04F0
2.7X1.8R-1.4ID-1.7H-SM

860-01714
ALLOW_APPLE_PREFIX=BS
BS04F1
2.7X1.8R-1.4ID-1.7H-SM

860-01714
ALLOW_APPLE_PREFIX=BS
BS04F2
2.7X1.8R-1.4ID-1.7H-SM

860-01714
ALLOW_APPLE_PREFIX=BS
BS04L0
2.7X1.8R-1.4ID-1.7H-SM

860-01714
ALLOW_APPLE_PREFIX=BS
BS04L1
2.7X1.8R-1.4ID-1.7H-SM

860-01924
ALLOW_APPLE_PREFIX=BS
BS04P0
BOSS-3.2OD1.4D-1.7H-SM

860-01924
ALLOW_APPLE_PREFIX=BS
BS04P1
BOSS-3.2OD1.4D-1.7H-SM

860-01924
ALLOW_APPLE_PREFIX=BS
BS04P2
BOSS-3.2OD1.4D-1.7H-SM

860-01924
ALLOW_APPLE_PREFIX=BS
BS04P3
BOSS-3.2OD1.4D-1.7H-SM

860-01714
ALLOW_APPLE_PREFIX=BS
BS04R0
2.7X1.8R-1.4ID-1.7H-SM

860-01714
ALLOW_APPLE_PREFIX=BS
BS04R1
2.7X1.8R-1.4ID-1.7H-SM

860-01714
ALLOW_APPLE_PREFIX=BS
BS04R4
2.7X1.8R-1.4ID-1.7H-SM

860-01714
ALLOW_APPLE_PREFIX=BS
BS04R5
2.7X1.8R-1.4ID-1.7H-SM

860-01936
ALLOW_APPLE_PREFIX=BS
BS04T2
2.7X1.8R-1.34H-SM

860-01936
ALLOW_APPLE_PREFIX=BS
BS04T3
2.7X1.8R-1.34H-SM

TOP BUMPERS

860-01819
ALLOW_APPLE_PREFIX=BM
BM0400
2.8OD1.2ID-1.703H-SM

860-01819
ALLOW_APPLE_PREFIX=BM
BM0413
2.8OD1.2ID-1.703H-SM

860-01819
ALLOW_APPLE_PREFIX=BM
BM0402
2.8OD1.2ID-1.703H-SM

860-01819
ALLOW_APPLE_PREFIX=BM
BM0403
2.8OD1.2ID-1.703H-SM

860-01819
ALLOW_APPLE_PREFIX=BM
BM0404
2.8OD1.2ID-1.703H-SM

860-01819
ALLOW_APPLE_PREFIX=BM
BM0405
2.8OD1.2ID-1.703H-SM

860-01819
ALLOW_APPLE_PREFIX=BM
BM0406
2.8OD1.2ID-1.703H-SM

860-01819
ALLOW_APPLE_PREFIX=BM
BM0407
2.8OD1.2ID-1.703H-SM

860-01819
ALLOW_APPLE_PREFIX=BM
BM0408
2.8OD1.2ID-1.703H-SM

860-01819
ALLOW_APPLE_PREFIX=BM
BM0409
2.8OD1.2ID-1.703H-SM

860-01819
ALLOW_APPLE_PREFIX=BM
BM0410
2.8OD1.2ID-1.703H-SM

860-01819
ALLOW_APPLE_PREFIX=BM
BM0412
2.8OD1.2ID-1.703H-SM

860-01819
ALLOW_APPLE_PREFIX=BM
BM0414
2.8OD1.2ID-1.703H-SM

BOTTOM BUMPERS

860-01820
ALLOW_APPLE_PREFIX=BM
BM0456
2.8OD1.2ID-3.416H-SM

860-01820
ALLOW_APPLE_PREFIX=BM
BM0451
2.8OD1.2ID-3.416H-SM

860-01820
ALLOW_APPLE_PREFIX=BM
BM0452
2.8OD1.2ID-3.416H-SM

860-01820
ALLOW_APPLE_PREFIX=BM
BM0453
2.8OD1.2ID-3.416H-SM

860-01820
ALLOW_APPLE_PREFIX=BM
BM0454
2.8OD1.2ID-3.416H-SM

860-01820
ALLOW_APPLE_PREFIX=BM
BM0455
2.8OD1.2ID-3.416H-SM

BOTTOM TP COWLING

860-01805
ALLOW_APPLE_PREFIX=BS
BS0420
3.4OD1.75ID-2.01H-SM

860-01805
ALLOW_APPLE_PREFIX=BS
BS0421
3.4OD1.75ID-2.01H-SM

CPU THERMAL STAGE HOLES

998-0845
ALLOW_APPLE_PREFIX=ZT
ZT0400
3P9R3P15

998-21974
ALLOW_APPLE_PREFIX=ZT
ZT0401
TH-NSP
SL-3.65X3.15-4.5X4.0

998-03850
ALLOW_APPLE_PREFIX=ZT
ZT0402
4.0R3.6-NSP

998-03850
ALLOW_APPLE_PREFIX=ZT
ZT0403
4.0R3.6-NSP

STIFFNERS

806-29572
ALLOW_APPLE_PREFIX=ST
ST0414
STIFFENER-MLB-CORNER-LOWER-X1930

806-29572
ALLOW_APPLE_PREFIX=ST
ST0415
STIFFENER-MLB-CORNER-LOWER-X1930

806-29573
ALLOW_APPLE_PREFIX=ST
ST0413
STIFFENER-RT-MID-MLB-X1930

806-29574
ALLOW_APPLE_PREFIX=ST
ST0412
STIFFENER-LEFT-MID-MLB-X1930

806-29575
ALLOW_APPLE_PREFIX=ST
ST0411
STIFFENER-CORNER-RT-UP-MLB-X1930

806-29576
ALLOW_APPLE_PREFIX=ST
ST0410
STIFFENER-CORNER-LT-UP-MLB-X1930

COAX STANDOFF

860-01841
ALLOW_APPLE_PREFIX=BS
BS04A0
BOSS-2.9X4.7-2.1H-SM

CPU SLEDS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
806-37511	4	SLED,CPU,SNOWSHOE,X2659	CPU_SLED_1,CPU_SLED_2,CPU_SLED_3,CPU_SLED_4	CPU_SLEDS:YES

BOM_COST_GROUP=MECHANICALS

PAGE TITLE: PD PARTS

Apple Inc.

DRAWING NUMBER: 051-07754
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
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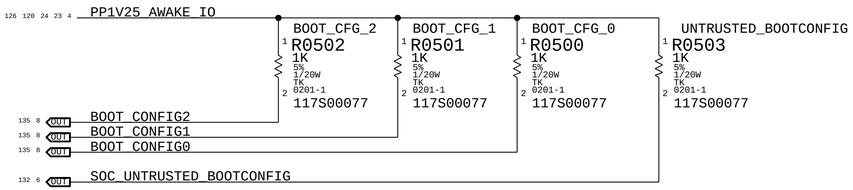
A BOOT CONFIG ID

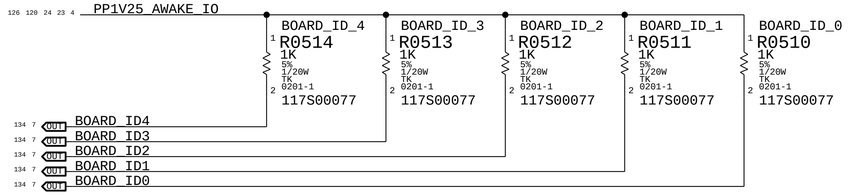


BOOT_CFG[2:0]	MODE	V	BUS	FREQ	USAGE
000	NAND,	1.2V	SPI0,	12MHZ,	PRODUCTION
001	NAND,	1.2V	SPI0,	40MHZ,	PRODUCTION
010	QUADNOR,	1.2V	SPI1,	24MHZ,	BACKUP PRODUCTION
011	RESERVED,	1.2V	NA,	NA,	M ONLY
100	NOR,	1.2V	SPI1,	6MHZ,	BRINGUP
101	NOR,	1.2V	SPI1,	12MHZ,	MANUFACTURING/SIVAL
110	QUADNOR,	1.2V	SPI1,	40MHZ,	PRODUCTION
111	NOR,	1.2V	SPI1,	40MHZ,	LEGACY PRODUCTION

SOC BOOT AND POWER ARCH SPEC 1.0.4 TABLE 2.4

STUFF R0503 FOR UNTRUSTED_BOOTCONFIG

B BOARD ID

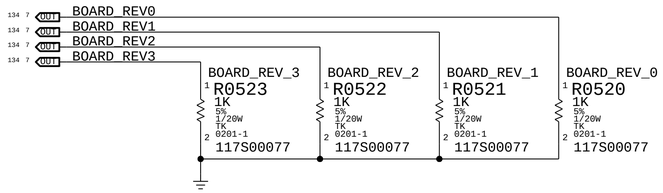


MLB BOARD_ID[7:0]:

BOARD_ID[7:5] COMES FROM SOC INTERNALLY

BOARD_ID[4:0] ARE THE STRAPS ON MLB, SAMPLED 100US AFTER COLD RESET DEASSERT

C BOARD REV



STUFFING RESISTOR MEANS BIT=0, START AT REV 0000 AND COUNT UP TO 1111

0000: P1BU
0001: P1
0010: P2
0011: EVT
0100: DVT
0101:
0110:
0111:
1000:
1001:
1010:
1011:
1100:
1101:
1110:
1111:

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: CONFIG STRAPS

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DRAWING NUMBER: 051-07754 SIZE: D

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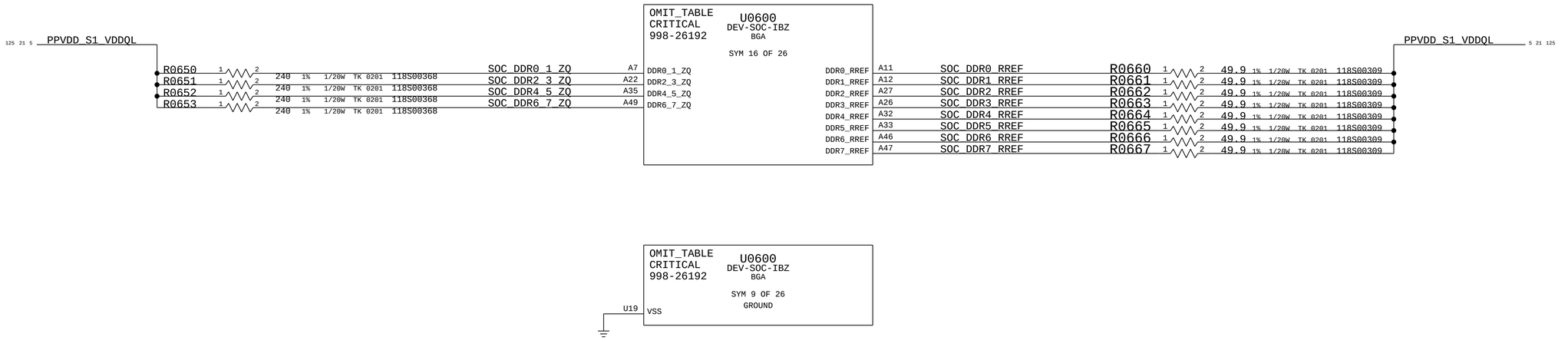

PAGE TITLE

SOC: MISC

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DRAWING NUMBER 051-07754 | SIZE D

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BRANCH dvt-1

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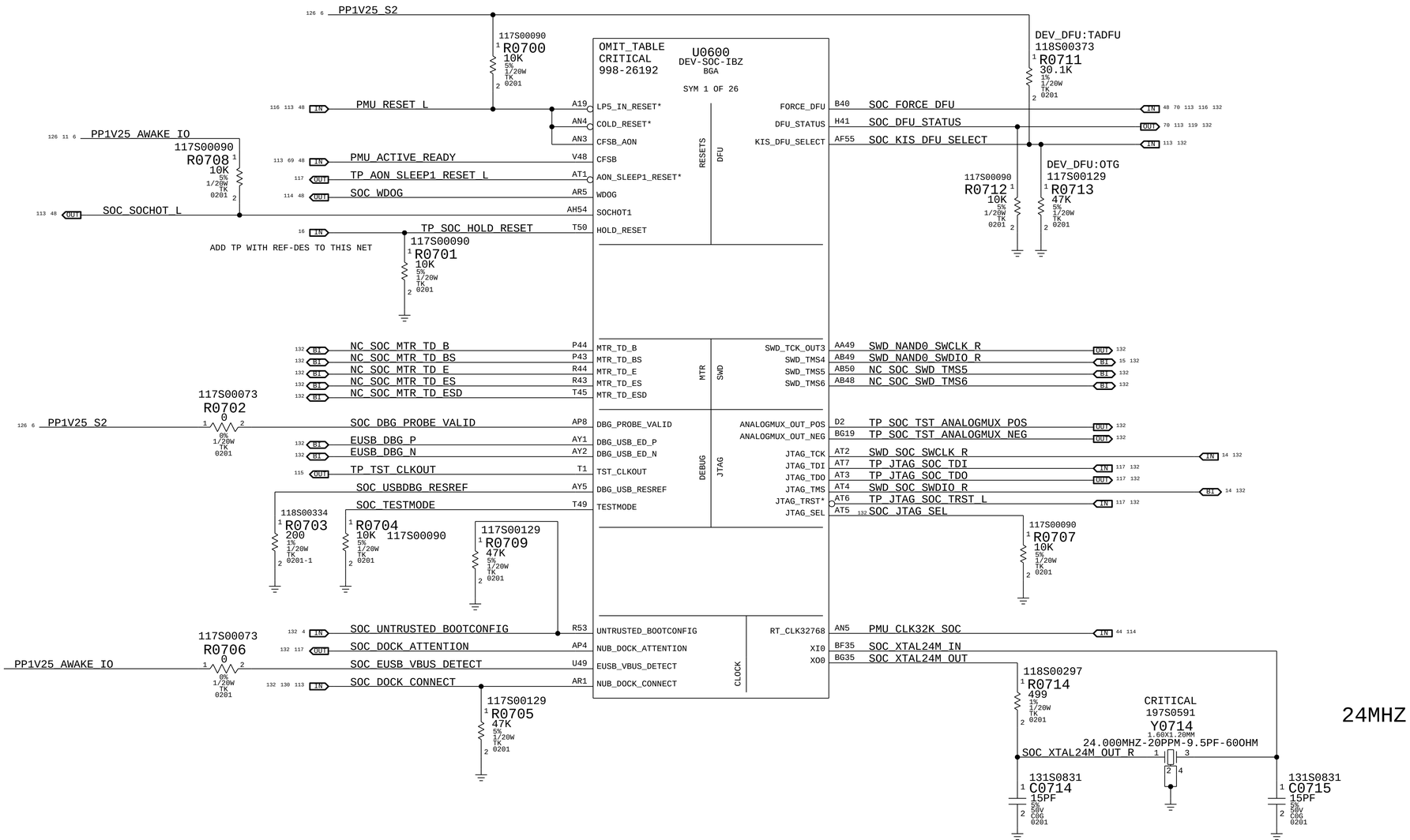

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: RESETS,CLOCKS,DEBUG

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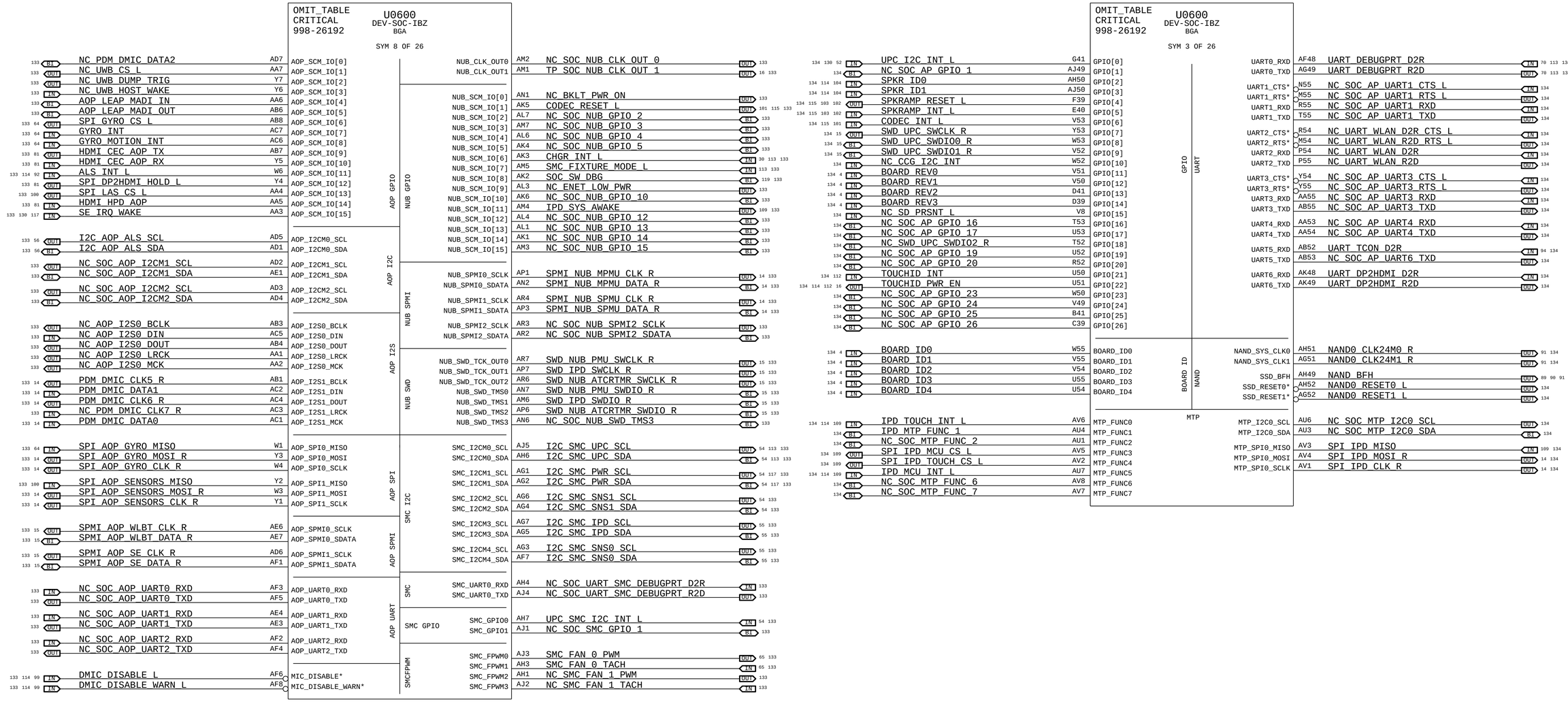
OMIT_TABLE
CRITICAL
998-26192
U0600
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SYM 8 OF 26
NC_PDM_DMIC_DATA2 AD7
NC_UWB_CS_L AA7
NC_UWB_DUMP_TRIG Y7
NC_UWB_HOST_WAKE Y6
AOP_LEAP_MADI_IN AA6
AOP_LEAP_MADI_OUT AB6
SPI_GYRO_CS_L AB8
GYRO_INT AC7
GYRO_MOTION_INT AC6
HDMI_CEC_AOP_TX AB7
HDMI_CEC_AOP_RX Y5
ALS_INT_L W6
SPI_DP2HDMI_HOLD_L Y4
SPI_LAS_CS_L AA4
HDMI_HPD_AOP AA5
SE_IRQ_WAKE AA3
I2C_AOP_ALS_SCL AD5
I2C_AOP_ALS_SDA AD1
NC_SOC_AOP_I2CM1_SCL AD2
NC_SOC_AOP_I2CM1_SDA AE1
NC_SOC_AOP_I2CM2_SCL AD3
NC_SOC_AOP_I2CM2_SDA AD4
NC_AOP_I2S0_BCLK AB3
NC_AOP_I2S0_DIN AC5
NC_AOP_I2S0_DOUT AB4
NC_AOP_I2S0_LRCK AA1
NC_AOP_I2S0_MCK AA2
PDM_DMIC_CLK5_R AB1
PDM_DMIC_DATA1 AC2
PDM_DMIC_CLK6_R AC4
NC_PDM_DMIC_CLK7_R AC3
PDM_DMIC_DATA0 AC1
SPI_AOP_GYRO_MISO W1
SPI_AOP_GYRO_MOSI_R Y3
SPI_AOP_GYRO_CLK_R W4
SPI_AOP_SENSORS_MISO Y2
SPI_AOP_SENSORS_MOSI_R W3
SPI_AOP_SENSORS_CLK_R Y1
SPMI_AOP_WLBT_CLK_R AE6
SPMI_AOP_WLBT_DATA_R AE7
SPMI_AOP_SE_CLK_R AD6
SPMI_AOP_SE_DATA_R AF1
NC_SOC_AOP_UART0_RXD AF3
NC_SOC_AOP_UART0_TXD AF5
NC_SOC_AOP_UART1_RXD AE4
NC_SOC_AOP_UART1_TXD AE3
NC_SOC_AOP_UART2_RXD AF2
NC_SOC_AOP_UART2_TXD AF4
DMIC_DISABLE_L AF6
DMIC_DISABLE_WARN_L AF8
AOP_SCM_IO[0]
AOP_SCM_IO[1]
AOP_SCM_IO[2]
AOP_SCM_IO[3]
AOP_SCM_IO[4]
AOP_SCM_IO[5]
AOP_SCM_IO[6]
AOP_SCM_IO[7]
AOP_SCM_IO[8]
AOP_SCM_IO[9]
AOP_SCM_IO[10]
AOP_SCM_IO[11]
AOP_SCM_IO[12]
AOP_SCM_IO[13]
AOP_SCM_IO[14]
AOP_SCM_IO[15]
AOP GPIO
AOP_I2CM0_SCL
AOP_I2CM0_SDA
AOP_I2CM1_SCL
AOP_I2CM1_SDA
AOP_I2CM2_SCL
AOP_I2CM2_SDA
AOP I2C
AOP_I2S0_BCLK
AOP_I2S0_DIN
AOP_I2S0_DOUT
AOP_I2S0_LRCK
AOP_I2S0_MCK
AOP_I2S1_BCLK
AOP_I2S1_DIN
AOP_I2S1_DOUT
AOP_I2S1_LRCK
AOP_I2S1_MCK
AOP I2S
AOP_SPI0_MISO
AOP_SPI0_MOSI
AOP_SPI0_SCLK
AOP_SPI1_MISO
AOP_SPI1_MOSI
AOP_SPI1_SCLK
AOP SPI
AOP_SPMI0_SCLK
AOP_SPMI0_SDATA
AOP_SPMI1_SCLK
AOP_SPMI1_SDATA
AOP SPMI
AOP_UART0_RXD
AOP_UART0_TXD
AOP_UART1_RXD
AOP_UART1_TXD
AOP_UART2_RXD
AOP_UART2_TXD
AOP UART
MIC_DISABLE*
MIC_DISABLE_WARN*
NUB_CLK_OUT0 AM2 NC_SOC_NUB_CLK_OUT_0
NUB_CLK_OUT1 AM1 TP_SOC_NUB_CLK_OUT_1
NUB_SCM_IO[0] AN1 NC_BKLT_PWR_ON
NUB_SCM_IO[1] AK5 CODEC_RESET_L
NUB_SCM_IO[2] AL7 NC_SOC_NUB_GPIO_2
NUB_SCM_IO[3] AM7 NC_SOC_NUB_GPIO_3
NUB_SCM_IO[4] AL6 NC_SOC_NUB_GPIO_4
NUB_SCM_IO[5] AK4 NC_SOC_NUB_GPIO_5
NUB_SCM_IO[6] AK3 CHGR_INT_L
NUB_SCM_IO[7] AM5 SMC_FIXTURE_MODE_L
NUB_SCM_IO[8] AK2 SOC_SW_DBG
NUB_SCM_IO[9] AL3 NC_ENET_LOW_PWR
NUB_SCM_IO[10] AK6 NC_SOC_NUB_GPIO_10
NUB_SCM_IO[11] AM4 IPD_SYS_AWAKE
NUB_SCM_IO[12] AL4 NC_SOC_NUB_GPIO_12
NUB_SCM_IO[13] AL1 NC_SOC_NUB_GPIO_13
NUB_SCM_IO[14] AK1 NC_SOC_NUB_GPIO_14
NUB_SCM_IO[15] AM3 NC_SOC_NUB_GPIO_15
NUB GPIO
NUB_SPMI0_SCLK AP1 SPMI_NUB_MPMU_CLK_R
NUB_SPMI0_SDATA AN2 SPMI_NUB_MPMU_DATA_R
NUB_SPMI1_SCLK AR4 SPMI_NUB_SPMU_CLK_R
NUB_SPMI1_SDATA AP3 SPMI_NUB_SPMU_DATA_R
NUB_SPMI2_SCLK AR3 NC_SOC_NUB_SPMI2_SCLK
NUB_SPMI2_SDATA AR2 NC_SOC_NUB_SPMI2_SDATA
NUB SPMI
NUB_SWD_TCK_OUT0 AR7 SWD_NUB_PMU_SWCLK_R
NUB_SWD_TCK_OUT1 AP7 SWD_IPD_SWCLK_R
NUB_SWD_TCK_OUT2 AR6 SWD_NUB_ATCRTMR_SWCLK_R
NUB_SWD_TMS0 AN7 SWD_NUB_PMU_SWDIO_R
NUB_SWD_TMS1 AM6 SWD_IPD_SWDIO_R
NUB_SWD_TMS2 AP6 SWD_NUB_ATCRTMR_SWDIO_R
NUB_SWD_TMS3 AN6 NC_SOC_NUB_SWD_TMS3
NUB SWD
SMC_I2CM0_SCL AJ5 I2C_SMC_UPC_SCL
SMC_I2CM0_SDA AH6 I2C_SMC_UPC_SDA
SMC_I2CM1_SCL AG1 I2C_SMC_PWR_SCL
SMC_I2CM1_SDA AG2 I2C_SMC_PWR_SDA
SMC_I2CM2_SCL AG6 I2C_SMC_SNS1_SCL
SMC_I2CM2_SDA AG4 I2C_SMC_SNS1_SDA
SMC_I2CM3_SCL AG7 I2C_SMC_IPD_SCL
SMC_I2CM3_SDA AG5 I2C_SMC_IPD_SDA
SMC_I2CM4_SCL AG3 I2C_SMC_SNS0_SCL
SMC_I2CM4_SDA AF7 I2C_SMC_SNS0_SDA
SMC I2C
SMC_UART0_RXD AH4 NC_SOC_UART_SMC_DEBUGPRT_D2R
SMC_UART0_TXD AJ4 NC_SOC_UART_SMC_DEBUGPRT_R2D
SMC
SMC_GPIO0 AH7 UPC_SMC_I2C_INT_L
SMC_GPIO1 AJ1 NC_SOC_SMC_GPIO_1
SMC GPIO
SMC_FPWM0 AJ3 SMC_FAN_0_PWM
SMC_FPWM1 AH3 SMC_FAN_0_TACH
SMC_FPWM2 AH1 NC_SMC_FAN_1_PWM
SMC_FPWM3 AJ2 NC_SMC_FAN_1_TACH
SMCFPWM
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GPIO[0] UPC_I2C_INT_L G41
GPIO[1] NC_SOC_AP_GPIO_1 AJ49
GPIO[2] SPKR_ID0 AH50
GPIO[3] SPKR_ID1 AJ50
GPIO[4] SPKRAMP_RESET_L F39
GPIO[5] SPKRAMP_INT_L E40
GPIO[6] CODEC_INT_L V53
GPIO[7] SWD_UPC_SWCLK_R Y53
GPIO[8] SWD_UPC_SWDIO0_R W53
GPIO[9] SWD_UPC_SWDIO1_R V52
GPIO[10] NC_CCG_I2C_INT W52
GPIO[11] BOARD_REV0 V51
GPIO[12] BOARD_REV1 V50
GPIO[13] BOARD_REV2 D41
GPIO[14] BOARD_REV3 D39
GPIO[15] NC_SD_PRSNT_L V8
GPIO[16] NC_SOC_AP_GPIO_16 T53
GPIO[17] NC_SOC_AP_GPIO_17 U53
GPIO[18] NC_SWD_UPC_SWDIO2_R T52
GPIO[19] NC_SOC_AP_GPIO_19 U52
GPIO[20] NC_SOC_AP_GPIO_20 R52
GPIO[21] TOUCHID_INT U50
GPIO[22] TOUCHID_PWR_EN U51
GPIO[23] NC_SOC_AP_GPIO_23 W50
GPIO[24] NC_SOC_AP_GPIO_24 V49
GPIO[25] NC_SOC_AP_GPIO_25 B41
GPIO[26] NC_SOC_AP_GPIO_26 C39
GPIO
BOARD_ID0 W55
BOARD_ID1 V55
BOARD_ID2 V54
BOARD_ID3 U55
BOARD_ID4 U54
BOARD ID
IPD_TOUCH_INT_L AV6
IPD_MTP_FUNC_1 AU4
NC_SOC_MTP_FUNC_2 AU1
SPI_IPD_MCU_CS_L AV5
SPI_IPD_TOUCH_CS_L AV2
IPD_MCU_INT_L AU7
NC_SOC_MTP_FUNC_6 AV8
NC_SOC_MTP_FUNC_7 AV7
MTP_FUNC0
MTP_FUNC1
MTP_FUNC2
MTP_FUNC3
MTP_FUNC4
MTP_FUNC5
MTP_FUNC6
MTP_FUNC7
MTP
UART0_RXD AF48 UART_DEBUGPRT_D2R
UART0_TXD AG49 UART_DEBUGPRT_R2D
UART1_CTS* N55 NC_SOC_AP_UART1_CTS_L
UART1_RTS* M55 NC_SOC_AP_UART1_RTS_L
UART1_RXD R55 NC_SOC_AP_UART1_RXD
UART1_TXD T55 NC_SOC_AP_UART1_TXD
UART2_CTS* R54 NC_UART_WLAN_D2R_CTS_L
UART2_RTS* M54 NC_UART_WLAN_R2D_RTS_L
UART2_RXD P54 NC_UART_WLAN_D2R
UART2_TXD P55 NC_UART_WLAN_R2D
UART3_CTS* Y54 NC_SOC_AP_UART3_CTS_L
UART3_RTS* Y55 NC_SOC_AP_UART3_RTS_L
UART3_RXD AA55 NC_SOC_AP_UART3_RXD
UART3_TXD AB55 NC_SOC_AP_UART3_TXD
UART4_RXD AA53 NC_SOC_AP_UART4_RXD
UART4_TXD AA54 NC_SOC_AP_UART4_TXD
UART5_RXD AB52 UART_TCON_D2R
UART5_TXD AB53 NC_SOC_AP_UART6_TXD
UART6_RXD AK48 UART_DP2HDMI_D2R
UART6_TXD AK49 UART_DP2HDMI_R2D
GPIO
UART
NAND_SYS_CLK0 AH51 NAND0_CLK24M0_R
NAND_SYS_CLK1 AG51 NAND0_CLK24M1_R
SSD_BFH AH49 NAND_BFH
SSD_RESET0* AH52 NAND0_RESET0_L
SSD_RESET1* AG52 NAND0_RESET1_L
BOARD ID
NAND
MTP_I2C0_SCL AU6 NC_SOC_MTP_I2C0_SCL
MTP_I2C0_SDA AU3 NC_SOC_MTP_I2C0_SDA
MTP_SPI0_MISO AV3 SPI_IPD_MISO
MTP_SPI0_MOSI AV4 SPI_IPD_MOSI_R
MTP_SPI0_SCLK AV1 SPI_IPD_CLK_R
BOM_COST_GROUP=SOC
PAGE TITLE
SOC: GPIOS,NAND,MTP,UART
Apple Inc.
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REVISION 6.0.0
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135 14	OUT	TDM_SPKRAMP_L_BCLK_R	V7	I2S0_BCLK	I2S	SPI	
135 131	IN	TDM_SPKRAMP_L_D2R	V6	I2S0_DIN			
135 14	OUT	TDM_SPKRAMP_L_R2D_R	U5	I2S0_DOUT			
135 14	OUT	TDM_SPKRAMP_L_FSYNC_R	U7	I2S0_LRCK			
135	OUT	NC_SOC_AP_I2S0_MCK	U6	I2S0_MCK			
135 14	OUT	TDM_SPKRAMP_R_BCLK_R	W7	I2S1_BCLK			
135 131	IN	TDM_SPKRAMP_R_D2R	V4	I2S1_DIN			
135 14	OUT	TDM_SPKRAMP_R_R2D_R	U3	I2S1_DOUT			
135 14	OUT	TDM_SPKRAMP_R_FSYNC_R	V5	I2S1_LRCK			
135	OUT	NC_SOC_AP_I2S1_MCK	U4	I2S1_MCK			
135 14	OUT	TDM_CODEC_BCLK_R	BC20	I2S2_BCLK			
135 115 101	IN	TDM_CODEC_D2R	BF20	I2S2_DIN			
135 14	OUT	TDM_CODEC_R2D_R	BG20	I2S2_DOUT			
135 14	OUT	TDM_CODEC_FSYNC_R	BE20	I2S2_LRCK			
135	OUT	NC_SOC_AP_I2S2_MCK	BD20	I2S2_MCK			
135	OUT	NC_TDM_SPKRAMP_TOP_BCLK_R	V3	I2S3_BCLK			
135	IN	NC_TDM_SPKRAMP_TOP_D2R	U2	I2S3_DIN			
135	OUT	NC_TDM_SPKRAMP_TOP_R2D_R	V2	I2S3_DOUT			
135	OUT	NC_TDM_SPKRAMP_TOP_FSYNC_R	U1	I2S3_LRCK			
135 88 87	IN	BT_TIME_SYNC	V1	I2S3_MCK			

SPI0_MISO	R3	BOOT_CONFIG2	IN	4 135			
SPI0_MOSI	R4	BOOT_CONFIG1	IN	4 135			
SPI0_SCLK	R6	BOOT_CONFIG0	IN	4 135			
SPI1_MISO	R1	SPI_SOCROM_IO1	BI	13 135			
SPI1_MOSI	N1	SPI_SOCROM_IO0	BI	13 135			
SPI1_SCLK	P1	SPI_SOCROM_CLK_R	OUT	14 135			
SPI1_SSIN	P2	SPI_SOCROM_CS_L	OUT	13 135			
SPI2_MISO	AT55	SPI_TOUCHID_MISO	IN	111 135			
SPI2_MOSI	AR55	SPI_TOUCHID_MOSI_R	OUT	14 135			
SPI2_SCLK	AT54	SPI_TOUCHID_CLK_R	OUT	14 135			
SPI2_SSIN	AT53	NC_SOC_AP_SPI2_CS_L	OUT	135			
SPI3_MISO	AP55	NC_SOC_AP_SPI3_MISO	IN	135			
SPI3_MOSI	AR53	NC_SOC_AP_SPI3_MOSI	OUT	135			
SPI3_SCLK	AR54	NC_SOC_AP_SPI3_SCLK	OUT	135			
SPI3_SSIN	AT52	NC_SOC_AP_SPI3_CS_L	OUT	135			
SPI4_MISO	AT50	SPI_TCON_MISO	IN	94 135			
SPI4_MOSI	AR51	SPI_TCON_MOSI_R	OUT	14 135			
SPI4_SCLK	AR52	SPI_TCON_CLK_R	OUT	14 135			
SPI4_SSIN	AT51	SPI_TCON_CS_L	OUT	94 113 135			
SPI5_MISO	AP50	NC_SOC_AP_SPI5_MISO	IN	135			
SPI5_MOSI	AR50	NC_SOC_AP_SPI5_MOSI	OUT	135			
SPI5_SCLK	AP52	NC_SOC_AP_SPI5_SCLK	OUT	135			
SPI5_SSIN	AP53	NC_SOC_AP_SPI5_CS_L	OUT	135			

135 113 52	OUT	I2C_UPC_SCL	AK53	I2C0_SCL	I2C	SEP	
135 113 52	BI	I2C_UPC_SDA	AK55	I2C0_SDA			
135	OUT	I2C_SPKRAMP_L_CODEC_SCL	AH55	I2C1_SCL			
135	BI	I2C_SPKRAMP_L_CODEC_SDA	AJ55	I2C1_SDA			
135 52	OUT	I2C_ATCRTMR_SCL	T6	I2C2_SCL			
135 52	BI	I2C_ATCRTMR_SDA	T3	I2C2_SDA			
135	OUT	I2C_HDMI_SPKRAMP_R_SCL	T7	I2C3_SCL			
135	BI	I2C_HDMI_SPKRAMP_R_SDA	T4	I2C3_SDA			
135 53	OUT	I2C_SD_DISP_BKLT_SCL	AJ53	I2C4_SCL			
135 53	BI	I2C_SD_DISP_BKLT_SDA	AJ54	I2C4_SDA			

SI2C0_SCL	BD19	I2C_SEEPROM_SCL	OUT	13 135			
SI2C0_SDA	BC18	I2C_SEEPROM_SDA	BI	13 135			
SSPI0_MISO	BE19	NC_SOC_SSPI0_MISO	IN	135			
SSPI0_MOSI	BC19	NC_SOC_SSPI0_MOSI	OUT	135			
SSPI0_SCLK	BE18	NC_SOC_SSPI0_SCLK	OUT	135			

135 88 87	IN	WLAN_TIME_SYNC	D40	FPWM0			
135 114 106	OUT	KBD_BKLT_PWM	H40	FPWM1			
135	OUT	P3V8AON_ILIMIT_DIV_PULL_PWM	F40	FPWM2			
135 114 48	IN	DBL_CLICK_DET	BF19	SGPIO0			
135	BI	NC_SOC_SGPIO1	BG18	SGPIO1			

THROTTLE_TRIGGER0*	K55	BUCK0_THERMAL_THROTTLE_L	IN	48 114 135			
THROTTLE_TRIGGER1*	J55	BUCK1_THERMAL_THROTTLE_L	IN	48 114 135			
THROTTLE_TRIGGER2*	G55	SPMU_VDDMAIN_UVWARN_L	IN	135			
THROTTLE_TRIGGER3*	H55	MPMU_VDDHI_UVWARN_L	IN	135			
THROTTLE_TRIGGER4*	L55	MPMU_VDDMAIN_UVWARN_L	IN	36 48 114 135			

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: I2S,I2C,SPI,THROT,CFG

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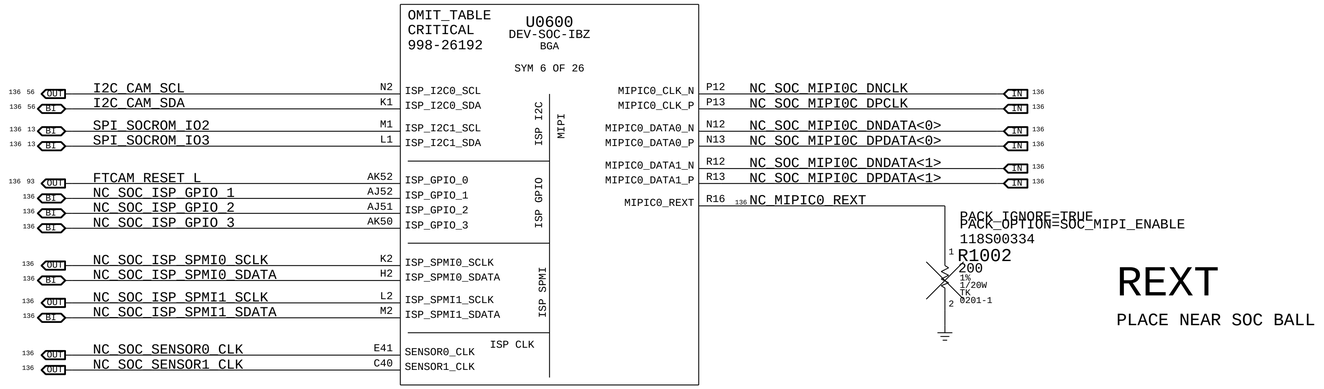
ISP / MIPI



BOM_COST_GROUP=SOC

PAGE TITLE	SOC: ISP, MIPI
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LPDP

OMIT_TABLE
CRITICAL
998-26192

U0600
DEV-SOC-IBZ
BGA

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137	BI	NC_LPDP_FTCAM_AUX_C	BD9	LPDPRX_AUX_D0	
137	BI	NC_SOC_LPDP_RX_AUX_D1	BD10	LPDPRX_AUX_D1	
137	BI	NC_SOC_LPDP_RX_AUX_D2	BD12	LPDPRX_AUX_D2	
137	BI	NC_SOC_LPDP_RX_AUX_D3	BD13	LPDPRX_AUX_D3	
137	BI	NC_SOC_LPDP_RX_AUX_D4	BC9	LPDPRX_AUX_D4	
137	BI	NC_SOC_LPDP_RX_AUX_D5	BC10	LPDPRX_AUX_D5	
137	BI	NC_SOC_LPDP_RX_AUX_D6	BC12	LPDPRX_AUX_D6	
137	BI	NC_SOC_LPDP_RX_AUX_D7	BC13	LPDPRX_AUX_D7	
137 92	IN	LPDP_FTCAM_DATA_P<0>	BB2	LPDPRX_D0_P	
137 92	IN	LPDP_FTCAM_DATA_N<0>	BB1	LPDPRX_D0_N	
137	IN	NC_SOC_LPDP_RX_D1_P	BC2	LPDPRX_D1_P	
137	IN	NC_SOC_LPDP_RX_D1_N	BC1	LPDPRX_D1_N	
137	IN	NC_SOC_LPDP_RX_D2P	BF4	LPDPRX_D2_P	
137	IN	NC_SOC_LPDP_RX_D2N	BG4	LPDPRX_D2_N	
137	IN	NC_SOC_LPDP_RX_D3P	BF5	LPDPRX_D3_P	
137	IN	NC_SOC_LPDP_RX_D3N	BG5	LPDPRX_D3_N	
137	IN	NC_SOC_LPDP_RX_D4P	BF7	LPDPRX_D4_P	
137	IN	NC_SOC_LPDP_RX_D4N	BG7	LPDPRX_D4_N	
137	IN	NC_SOC_LPDP_RX_D5P	BF8	LPDPRX_D5_P	
137	IN	NC_SOC_LPDP_RX_D5N	BG8	LPDPRX_D5_N	
137	IN	NC_SOC_LPDP_RX_D6P	BF10	LPDPRX_D6_P	
137	IN	NC_SOC_LPDP_RX_D6N	BG10	LPDPRX_D6_N	
137	IN	NC_SOC_LPDP_RX_D7P	BF11	LPDPRX_D7_P	
137	IN	NC_SOC_LPDP_RX_D7N	BG11	LPDPRX_D7_N	
137		SOC_LPDP_RX0_RCAL_POS	BD2	LPDPRX0_RCAL_POS	
137		SOC_LPDP_RX0_RCAL_NEG	BD1	LPDPRX0_RCAL_NEG	
137		NC_SOC_LPDP_RX1_RCAL_POS	BF9	LPDPRX1_RCAL_POS	
137		NC_SOC_LPDP_RX1_RCAL_NEG	BG9	LPDPRX1_RCAL_NEG	

LPDP TX

		LPDPTX_D0_P	BA55	LPDP_INT_DATA_C_P<0>	OUT 94 137
		LPDPTX_D0_N	BA54	LPDP_INT_DATA_C_N<0>	OUT 94 137
		LPDPTX_D1_P	AY55	LPDP_INT_DATA_C_P<1>	OUT 94 137
		LPDPTX_D1_N	AY54	LPDP_INT_DATA_C_N<1>	OUT 94 137
		LPDPTX_D2_P	AW55	LPDP_INT_DATA_C_P<2>	OUT 94 137
		LPDPTX_D2_N	AW54	LPDP_INT_DATA_C_N<2>	OUT 94 137
		LPDPTX_D3_P	AV55	LPDP_INT_DATA_C_P<3>	OUT 94 137
		LPDPTX_D3_N	AV54	LPDP_INT_DATA_C_N<3>	OUT 94 137
		LPDPTX_AUX_P	AY52	LPDP_INT_AUX_C_P	BI 94 137
		LPDPTX_AUX_N	AY51	LPDP_INT_AUX_C_N	BI 94 137
		LPDPTX_RCAL_POS	AW52	SOC_LPDP_INT_RCAL_POS	
		LPDPTX_RCAL_NEG	AW51	SOC_LPDP_INT_RCAL_NEG	

LPDP RX
LPDP EXT

		LPDPTX_EXT_D0_P	BF13	LPDP_DP2HDMI_DATA_C_P<0>	OUT 130 137
		LPDPTX_EXT_D0_N	BG13	LPDP_DP2HDMI_DATA_C_N<0>	OUT 130 137
		LPDPTX_EXT_D1_P	BF14	LPDP_DP2HDMI_DATA_C_P<1>	OUT 130 137
		LPDPTX_EXT_D1_N	BG14	LPDP_DP2HDMI_DATA_C_N<1>	OUT 130 137
		LPDPTX_EXT_D2_P	BF15	LPDP_DP2HDMI_DATA_C_P<2>	OUT 130 137
		LPDPTX_EXT_D2_N	BG15	LPDP_DP2HDMI_DATA_C_N<2>	OUT 130 137
		LPDPTX_EXT_D3_P	BF16	LPDP_DP2HDMI_DATA_C_P<3>	OUT 130 137
		LPDPTX_EXT_D3_N	BG16	LPDP_DP2HDMI_DATA_C_N<3>	OUT 130 137
		LPDPTX_EXT_AUX_P	BC15	LPDP_DP2HDMI_AUX_C_P	BI 130 137
		LPDPTX_EXT_AUX_N	BD15	LPDP_DP2HDMI_AUX_C_N	BI 130 137
		LPDPTX_EXT_RCAL_POS	BC16	SOC_LPDP_DP2HDMI_RCAL_POS	
		LPDPTX_EXT_RCAL_NEG	BD16	SOC_LPDP_DP2HDMI_RCAL_NEG	

DISPLAY

		DISP_HPD	R50	LPDP_INT_HPD	IN 16 94 113 137
		DISP_EXT_HPD	R51	LPDP_DP2HDMI_HPD	IN 16 117 130 137
		DISP_SPI_MISO	H1	SPI_DISP_BKLT_MISO	IN 97 137
		DISP_SPI_MOSI	F1	SPI_DISP_BKLT_MOSI_R	OUT 14 137
		DISP_SPI_SCLK	E1	SPI_DISP_BKLT_CLK_R	OUT 14 137
		DISP_SPI_SSIN	D1	SPI_DISP_BKLT_CS_L	OUT 97 113 137
		DISP_SPMI_SCLK	G2	SPMI_DISP_BKLT_CLK_R	OUT 14 137
		DISP_SPMI_SDATA	G1	SPMI_DISP_BKLT_DATA_R	BI 14 137
		DISP_POL	AF54	NC_SOC_DISP_POL	BI 137
		DISP_FSYNC	F41	DISP_BKLT_FSYNC	BI 113 130 137
		DISP_LSYNC	G39	DISP_BKLT_LSYNC	BI 97 113 137
		DISP_TOUCH_BSYNC0	AF51	NC_SOC_DISP_TOUCH_BSYNC0	BI 137
		DISP_TOUCH_BSYNC1	AF50	NC_SOC_DISP_TOUCH_BSYNC1	BI 137
		DISP_TOUCH_EB	AF53	NC_SOC_DISP_TOUCH_EB	IN 137
		DISP_INT	G40	BKLT_BOOST_THROTTLE_L	IN 137

118S00334
R1123
200 PACK_OPTION=LPDP_INT_RCAL
1% 1/20W TK
0201-1

131S00003
C1123
10PF PACK_OPTION=LPDP_INT_RCAL
5% 25V C0G
0201

RCAL
PLACE NEAR SOC BALL

118S00334
R1122
200 PACK_OPTION=LPDP_EXT
1% 1/20W TK
0201-1

131S00003
C1122
10PF PACK_OPTION=LPDP_EXT
5% 25V C0G
0201

RCAL
PLACE NEAR SOC BALL

PACK_OPTION=LPDPRX0_RCAL

RCAL
PLACE NEAR SOC BALL

118S00334
R1121
200
1% 1/20W TK
0201-1

131S00003
C1121
10PF
5% 25V C0G
0201

PACK_OPTION=LPDPRX0_RCAL

PACK_IGNORE=TRUE
PACK_OPTION=LPDPRX1_RCAL

RCAL
PLACE NEAR SOC BALL

118S00334
R1120
200
1% 1/20W TK
0201-1

131S00003
C1120
10PF
5% 25V C0G
0201

PACK_IGNORE=TRUE
PACK_OPTION=LPDPRX1_RCAL

PAGE TITLE
SOC: LPDP

Apple Inc.

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PCIE

PP1V25_AWAKE_IO

OMIT_TABLE
CRITICAL
998-26192

U0600
DEV-SOC-IBZ
BGA

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PCIE ST0 / PCIE GP0

PCIE_NAND0_D2R_P<0>	BG23	ST_PCIE_RX0_P	
PCIE_NAND0_D2R_N<0>	BF23	ST_PCIE_RX0_N	
PCIE_NAND0_R2D_C_P<0>	BD22	ST_PCIE_TX0_P	
PCIE_NAND0_R2D_C_N<0>	BE22	ST_PCIE_TX0_N	
PCIE_CLK100M_NAND0_0_P	BD38	ST_PCIE_REF_CLK0_P	
PCIE_CLK100M_NAND0_0_N	BC38	ST_PCIE_REF_CLK0_N	
NAND0_CLKREQ0_L	AH53	ST_PCIE_CLKREQ0*	
NAND0_PCIE_RESET_L	AG55	ST_PCIE_PERST0*	
		GP_PCIE_RX0_P	BG27 PCIE_WLBT_D2R_P
		GP_PCIE_RX0_N	BF27 PCIE_WLBT_D2R_N
		GP_PCIE_TX0_P	BD26 PCIE_WLBT_R2D_C_P
		GP_PCIE_TX0_N	BE26 PCIE_WLBT_R2D_C_N
		GP_PCIE_REF_CLK0_P	BC35 PCIE_CLK100M_WLBT_P
		GP_PCIE_REF_CLK0_N	BD35 PCIE_CLK100M_WLBT_N
		GP_PCIE_CLKREQ0*	AA52 WLBT_CLKREQ_L
		GP_PCIE_PERST0*	Y50 WLBT_RESET_L

PCIE ST1 / PCIE GP1

PCIE_NAND0_D2R_P<1>	BG25	ST_PCIE_RX1_P	
PCIE_NAND0_D2R_N<1>	BF25	ST_PCIE_RX1_N	
PCIE_NAND0_R2D_C_P<1>	BD24	ST_PCIE_TX1_P	
PCIE_NAND0_R2D_C_N<1>	BE24	ST_PCIE_TX1_N	
PCIE_CLK100M_NAND0_1_P	BD37	ST_PCIE_REF_CLK1_P	
PCIE_CLK100M_NAND0_1_N	BC37	ST_PCIE_REF_CLK1_N	
NAND0_CLKREQ1_L	AG53	ST_PCIE_CLKREQ1*	
		GP_PCIE_RX1_P	BG29 PCIE_SD_D2R_P
		GP_PCIE_RX1_N	BF29 PCIE_SD_D2R_N
		GP_PCIE_TX1_P	BD28 PCIE_SD_R2D_C_P
		GP_PCIE_TX1_N	BE28 PCIE_SD_R2D_C_N
		GP_PCIE_REF_CLK1_P	BF37 PCIE_CLK100M_SD_P
		GP_PCIE_REF_CLK1_N	BG37 PCIE_CLK100M_SD_N
		GP_PCIE_CLKREQ1*	Y52 SD_CLKREQ_L
		GP_PCIE_PERST1*	AA50 SD_RESET_L

PCIE GP2

		GP_PCIE_RX2_P	BG31 NC_PCIE_USBHC_D2R_P
		GP_PCIE_RX2_N	BF31 NC_PCIE_USBHC_D2R_N
		GP_PCIE_TX2_P	BD30 NC_PCIE_USBHC_R2D_C_P
		GP_PCIE_TX2_N	BE30 NC_PCIE_USBHC_R2D_C_N
		GP_PCIE_REF_CLK2_P	BC34 NC_PCIE_CLK100M_USBHC_P
		GP_PCIE_REF_CLK2_N	BD34 NC_PCIE_CLK100M_USBHC_N
		GP_PCIE_CLKREQ2*	AA51 NC_USBHC_CLKREQ_L
		GP_PCIE_PERST2*	W49 NC_USBHC_RESET_L

PCIE GP3

		GP_PCIE_RX3_P	BG33 NC_SOC_GP_PCIE_RX3_P
		GP_PCIE_RX3_N	BF33 NC_SOC_GP_PCIE_RX3_N
		GP_PCIE_TX3_P	BD32 NC_SOC_GP_PCIE_TX3_P
		GP_PCIE_TX3_N	BE32 NC_SOC_GP_PCIE_TX3_N
		GP_PCIE_REF_CLK3_P	BF38 NC_SOC_GP_PCIE_CLK3_100M_P
		GP_PCIE_REF_CLK3_N	BG38 NC_SOC_GP_PCIE_CLK3_100M_N
		GP_PCIE_CLKREQ3*	Y51 NC_SOC_GP_PCIE_CLKREQ_3_L
		GP_PCIE_PERST3*	Y49 NC_SOC_GP_PCIE_PERST_3_L

SOC_ST_PCIE_RCAL_POS	BB27	ST_PCIE_RCAL_POS	
SOC_ST_PCIE_RCAL_NEG	BB26	ST_PCIE_RCAL_NEG	
		GP_PCIE_RCAL_POS	BB30 SOC_GP_PCIE_RCAL_POS
		GP_PCIE_RCAL_NEG	BB29 SOC_GP_PCIE_RCAL_NEG

118S00373
R1204 30.1K 1% 1/20W TK 0201

117S00129
R1214 47K 5% 1/20W TK 0201

118S00373
R1205 30.1K 1% 1/20W TK 0201

118S00373
R1200 30.1K 1% 1/20W TK 0201

R1210 47K 5% 1/20W TK 0201 117S00129 PACK_OPTION=PCIE_GP0

R1201 30.1K 1% 1/20W TK 0201 118S00373 PACK_OPTION=PCIE_GP1

R1211 47K 5% 1/20W TK 0201 117S00129 PACK_OPTION=PCIE_GP1

R1202 30.1K 1% 1/20W TK 0201 118S00373 PACK_IGNORE=TRUE PACK_OPTION=PCIE_GP2

R1212 47K 5% 1/20W TK 0201 117S00129 PACK_IGNORE=TRUE PACK_OPTION=PCIE_GP2

R1203 30.1K 1% 1/20W TK 0201 118S00373 PACK_IGNORE=TRUE PACK_OPTION=PCIE_GP3

R1213 47K 5% 1/20W TK 0201 117S00129 PACK_IGNORE=TRUE PACK_OPTION=PCIE_GP3

RCAL

PLACE NEAR SOC BALL

118S00334
R1224 200 1% 1/20W TK 0201-1

131S00003
C1224 10PF 5% 25V C0G 0201

RCAL

PLACE NEAR SOC BALL

118S00334
R1225 200 1% 1/20W TK 0201-1

131S00003
C1225 10PF 5% 25V C0G 0201

PAGE TITLE: SOC: PCIE

Apple Inc.

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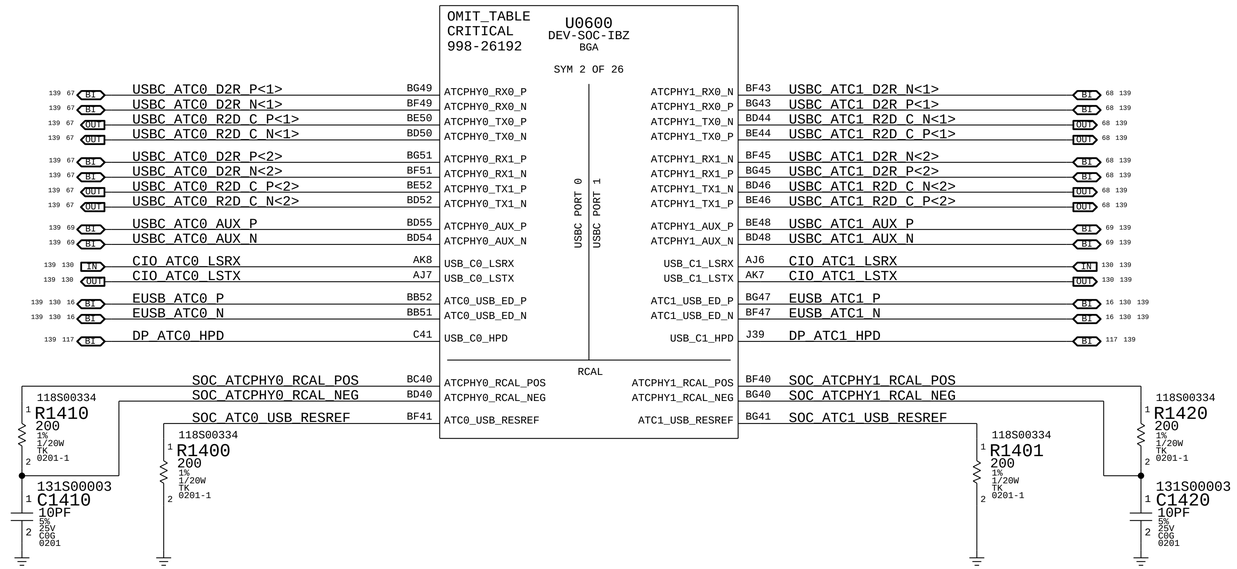
CIO



RCAL

PLACE NEAR SOC BALL

RCAL

PLACE NEAR SOC BALL

BOM_COST_GROUP=SOC

PAGE TITLE	SOC: CIO
	Apple Inc.
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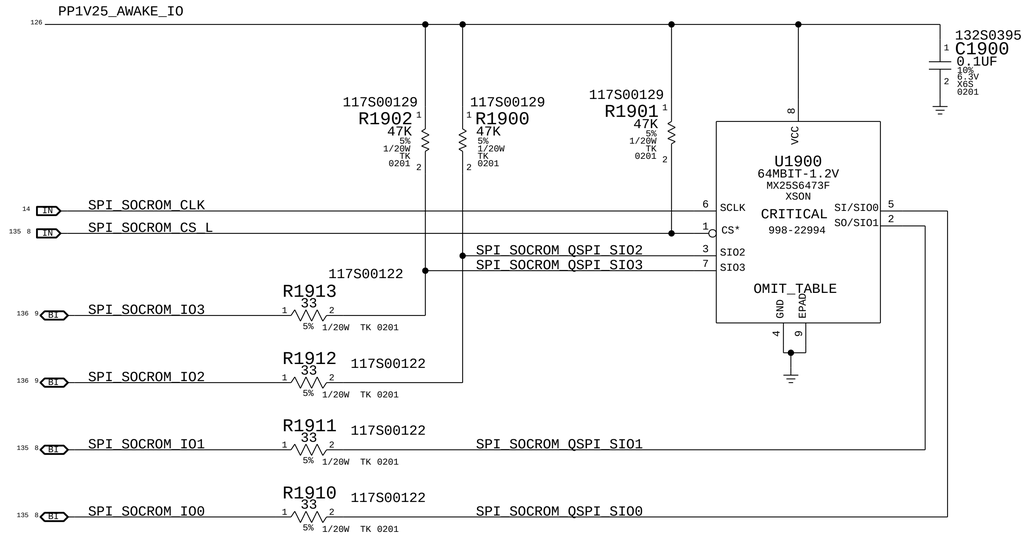
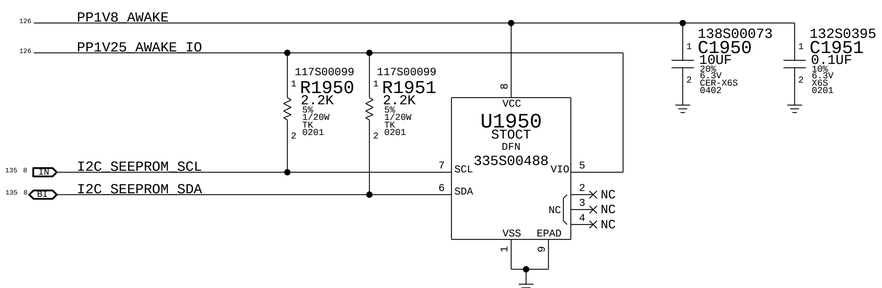
8	7	6	5	4	3	2	1

A SPI ROM



B SEP EEPROM



BOM_COST_GROUP=SOC

PAGE TITLE: SOC: SPI NOR, SEP ROM

Apple Inc.

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SOC ROM CLK SOURCE TERMINATION

R2002 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.P1:25MM
135 8 IN SPI_SOCROM_CLK_R 1 2 SPI_SOCROM_CLK OUT 33

TOUCHID SOURCE TERMINATIONS

R2004 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AR55:25MM
135 8 IN SPI_TOUCHID_MOSI_R 1 2 SPI_TOUCHID_MOSI OUT 111

R2005 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AT54:25MM
135 8 IN SPI_TOUCHID_CLK_R 1 2 SPI_TOUCHID_CLK OUT 111

IPD SOURCE TERMINATIONS

R2006 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AV4:25MM
134 7 IN SPI_IPD_MOSI_R 1 2 SPI_IPD_MOSI OUT 109 123

R2007 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AV1:25MM
134 7 IN SPI_IPD_CLK_R 1 2 SPI_IPD_CLK OUT 109 123

TCON SOURCE TERMINATIONS

R2090 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AR51:25MM
135 8 IN SPI_TCON_MOSI_R 1 2 SPI_TCON_MOSI OUT 94

R2091 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AR52:25MM
135 8 IN SPI_TCON_CLK_R 1 2 SPI_TCON_CLK OUT 94

IMU SOURCE TERMINATIONS

R2008 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.Y3:25MM
133 7 IN SPI_AOP_GYRO_MOSI_R 1 2 SPI_AOP_GYRO_MOSI OUT 64

R2009 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.W4:25MM
133 7 IN SPI_AOP_GYRO_CLK_R 1 2 SPI_AOP_GYRO_CLK OUT 64

SOC SPMI MPMU

DEVICE ADDRESS: 0X0F (SET IN OTP)

R2060 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AP1:25MM
133 7 IN SPMI_NUB_MPMU_CLK_R 1 2 SPMI_NUB_MPMU_CLK OUT 45

R2061 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AN2:25MM
133 7 BI SPMI_NUB_MPMU_DATA_R 1 2 SPMI_NUB_MPMU_DATA BI 45

SOC SPMI SPMU

DEVICE ADDRESS: 0X0F (SET IN OTP)

R2062 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AR4:25MM
133 7 IN SPMI_NUB_SPMU_CLK_R 1 2 SPMI_NUB_SPMU_CLK OUT 39

R2063 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AP3:25MM
133 7 BI SPMI_NUB_SPMU_DATA_R 1 2 SPMI_NUB_SPMU_DATA BI 39

SOC SWD SERIES R

R2080 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AT2:25MM
132 6 IN SWD_SOC_SWCLK_R 1 2 SWD_SOC_SWCLK OUT 70 113

R2081 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AT4:25MM
132 6 BI SWD_SOC_SWDIO_R 1 2 SWD_SOC_SWDIO BI 70 113

LAS SOURCE TERMINATIONS

R20B0 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.W3:25MM
133 7 IN SPI_AOP_SENSORS_MOSI_R 1 2 SPI_AOP_SENSORS_MOSI OUT 100

R20B1 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.Y1:25MM
133 7 IN SPI_AOP_SENSORS_CLK_R 1 2 SPI_AOP_SENSORS_CLK OUT 100

DMIC SOURCE TERMINATIONS

R20C0 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AB1:25MM
133 7 IN PDM_DMIC_CLK5_R 1 2 PDM_DMIC_CLK5 OUT 105

R20C1 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.AC4:25MM
133 7 IN PDM_DMIC_CLK6_R 1 2 PDM_DMIC_CLK6 OUT 105

DMIC SERIES R

R20C2 33 5% 1/20W TK 0201
PLACE_NEAR=UR970.7:25MM
133 7 OUT PDM_DMIC_DATA0 1 2 PDM_DMIC_DATA0_R IN 105

R20C3 33 5% 1/20W TK 0201
PLACE_NEAR=UR970.6:25MM
133 7 OUT PDM_DMIC_DATA1 1 2 PDM_DMIC_DATA1_R IN 105

TDM SOURCE TERMINATIONS

R2010 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.V7:25MM
135 8 IN TDM_SPKRAMP_L_BCLK_R 1 2 TDM_SPKRAMP_L_BCLK OUT 131

R2011 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.U5:25MM
135 8 IN TDM_SPKRAMP_L_R2D_R 1 2 TDM_SPKRAMP_L_R2D OUT 131

R2012 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.U7:25MM
135 8 IN TDM_SPKRAMP_L_FSYNC_R 1 2 TDM_SPKRAMP_L_FSYNC OUT 131

R2020 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.W7:25MM
135 8 IN TDM_SPKRAMP_R_BCLK_R 1 2 TDM_SPKRAMP_R_BCLK OUT 131

R2021 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.U3:25MM
135 8 IN TDM_SPKRAMP_R_R2D_R 1 2 TDM_SPKRAMP_R_R2D OUT 131

R2022 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.V5:25MM
135 8 IN TDM_SPKRAMP_R_FSYNC_R 1 2 TDM_SPKRAMP_R_FSYNC OUT 131

R2030 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.BC20:25MM
135 8 IN TDM_CODEC_BCLK_R 1 2 TDM_CODEC_BCLK OUT 101 115

R2031 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.BG20:25MM
135 8 IN TDM_CODEC_R2D_R 1 2 TDM_CODEC_R2D OUT 101 115

R2032 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.BE20:25MM
135 8 IN TDM_CODEC_FSYNC_R 1 2 TDM_CODEC_FSYNC OUT 101 115

DISP BKLT SPMI

R20E0 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.G2:25MM
137 10 IN SPMI_DISP_BKLT_CLK_R 1 2 SPMI_DISP_BKLT_CLK OUT 96

R20E1 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.G1:25MM
137 10 BI SPMI_DISP_BKLT_DATA_R 1 2 SPMI_DISP_BKLT_DATA BI 96

DISP BKLT SPI SOURCE TERMINATIONS

R20F1 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.F1:25MM
137 10 BI SPI_DISP_BKLT_MOSI_R 1 2 SPI_DISP_BKLT_MOSI BI 97

R20F0 33 5% 1/20W TK 0201
PLACE_NEAR=U0600.E1:25MM
137 10 IN SPI_DISP_BKLT_CLK_R 1 2 SPI_DISP_BKLT_CLK OUT 97

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: PROJECT SUPPORT (1/3)

Apple Inc.

DRAWING NUMBER: 051-07754
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
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UPC SWD

118S00465
R2110
15
1% 1/20W TK 0201
PLACE_NEAR=U0600.Y53:25MM

118S00309
R2111
49.9
1% 1/20W TK 0201
PLACE_NEAR=R2112.1:2MM

118S00309
R2112
49.9
1% 1/20W TK 0201
PLACE_NEAR=U5500.E16:40MM

117S00122
R2113
33
5% 1/20W TK 0201
PLACE_NEAR=U0600.W53:25MM

117S00122
R2114
33
5% 1/20W TK 0201
PLACE_NEAR=U0600.V52:25MM

134 7	IN	SWD_UPC_SWCLK_R	1	2 77 16	SWD_UPC_SWCLK_RR
1	2	SWD_UPC_SWCLK	OUT	69	
1	2	SWD_UPC_SWCLK1	OUT	32	
134 7	BI	SWD_UPC_SWDIO0_R	1	2	SWD_UPC_SWDIO0
BI	16 69 77				
134 7	BI	SWD_UPC_SWDIO1_R	1	2	SWD_UPC_SWDIO2
BI	131				

NAND SWD

118S00465
R2140
15
1% 1/20W TK 0201
PLACE_NEAR=U0600.AA49:25MM

118S00309
R2141
49.9
1% 1/20W TK 0201
PLACE_NEAR=R2142.1:2MM

118S00309
R2142
49.9
1% 1/20W TK 0201
PLACE_NEAR=UN100.F6:25MM

118S00465
R2143
15
1% 1/20W TK 0201
PLACE_NEAR=U0600.AB49:25MM

118S00309
R2144
49.9
1% 1/20W TK 0201
PLACE_NEAR=R2145.1:2MM

118S00309
R2145
49.9
1% 1/20W TK 0201
PLACE_NEAR=UN100.E6:25MM

132	IN	SWD_NAND0_SWCLK_R	1	2	SWD_NAND0_SWCLK_RR
1	2	SWD_NAND0_S5E0_SWCLK	OUT	89 91	
1	2	SWD_NAND0_S5E1_SWCLK	OUT	90 91	
132 6	BI	SWD_NAND0_SWDIO_R	1	2	SWD_NAND0_SWDIO_RR
1	2	SWD_NAND0_S5E0_SWDIO	BI	89 91	
1	2	SWD_NAND0_S5E1_SWDIO	BI	90 91	

PMU SWD

118S00465
R2100
15
1% 1/20W TK 0201
PLACE_NEAR=U0600.AR7:25MM

118S00309
R2101
49.9
1% 1/20W TK 0201
PLACE_NEAR=U7700.J9:25MM

118S00309
R2102
49.9
1% 1/20W TK 0201
PLACE_NEAR=U8100.J13:25MM

118S00465
R2103
15
1% 1/20W TK 0201
PLACE_NEAR=U0600.AN7:25MM

118S00309
R2104
49.9
1% 1/20W TK 0201
PLACE_NEAR=U7700.F8:25MM

118S00309
R2105
49.9
1% 1/20W TK 0201
PLACE_NEAR=U8100.K12:25MM

133 7	IN	SWD_NUB_PMU_SWCLK_R	1	2	SOC_NUB_SWD_TCK_OUT0_R
1	2	SWD_NUB_SWCLK_SPMU	OUT	130	
1	2	SWD_NUB_SWCLK_MPMU	OUT	130	
133 7	BI	SWD_NUB_PMU_SWDIO_R	1	2	SOC_NUB_SWD_TMS0_R
1	2	SWD_NUB_SWDIO_SPMU	BI	130	
1	2	SWD_NUB_SWDIO_MPMU	BI	130	

RT13 SWD

117S00122
R2120
33
5% 1/20W TK 0201
PLACE_NEAR=U0600.AR6:25MM

117S00122
R2121
33
5% 1/20W TK 0201
PLACE_NEAR=U0600.AP6:25MM

133 7	IN	SWD_NUB_ATCRTMR_SWCLK_R	1	2	SWD_NUB_ATCRTMR_SWCLK
OUT	130				
133 7	BI	SWD_NUB_ATCRTMR_SWDIO_R	1	2	SWD_NUB_ATCRTMR_SWDIO
BI	130				

IPD SWD

117S00122
R2123
33
5% 1/20W TK 0201
PLACE_NEAR=U0600.AP7:25MM

117S00122
R2124
33
5% 1/20W TK 0201
PLACE_NEAR=U0600.AM6:25MM

133 7	IN	SWD_IPD_SWCLK_R	1	2	SWD_IPD_CLK_R
OUT	109				
133 7	BI	SWD_IPD_SWDIO_R	1	2	SWD_IPD_DATA_R
BI	109				

AOP SPMI 0 - WLBT

117S00122
R2160
33
5% 1/20W TK 0201
PLACE_NEAR=U0600.AE6:25MM

117S00122
R2161
33
5% 1/20W TK 0201
PLACE_NEAR=U0600.AE7:25MM

133 7	IN	SPMI_AOP_WLBT_CLK_R	1	2	SPMI_WLBT_CLK
OUT	87				
133 7	BI	SPMI_AOP_WLBT_DATA_R	1	2	SPMI_WLBT_DATA
BI	87				

AOP SPMI 1 - SE

117S00122
R2170
33
5% 1/20W TK 0201
PLACE_NEAR=U0600.AD6:25MM

117S00122
R2171
33
5% 1/20W TK 0201
PLACE_NEAR=U0600.AF1:25MM

133 7	IN	SPMI_AOP_SE_CLK_R	1	2	SPMI_SE_CLK
OUT	27 117				
133 7	BI	SPMI_AOP_SE_DATA_R	1	2	SPMI_SE_DATA
BI	27 117				

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: PROJECT SUPPORT (2/3)

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DRAWING NUMBER: 051-07754 | SIZE: D
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BRANCH: dvt-1
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EUSB PROBE POINTS

(SOC SIDE) (RETIMER SIDE)

139 130 12 BI EUSB_ATC0_P BI

PP2200 P4MM SM PLACE_NEAR=U0600.BB52:14MM

PP2202 P4MM SM PLACE_NEAR=UF600.A1:7MM

139 130 12 BI EUSB_ATC0_N BI

PP2201 P4MM SM PLACE_NEAR=U0600.BB51:14MM

PP2203 P4MM SM PLACE_NEAR=UF600.B1:7MM

139 130 12 BI EUSB_ATC1_P BI

PP2210 P4MM SM PLACE_NEAR=U0600.BG47:14MM

PP2212 P4MM SM PLACE_NEAR=UF650.A1:7MM

139 130 12 BI EUSB_ATC1_N BI

PP2211 P4MM SM PLACE_NEAR=U0600.BF47:14MM

PP2213 P4MM SM PLACE_NEAR=UF650.B1:7MM

132 73 BI EUSB_DBG_P BI

PP2220 P4MM SM PLACE_NEAR=U0600.AY1:7MM

PP2222 P4MM SM PLACE_NEAR=UF600.A2:7MM

132 73 BI EUSB_DBG_N BI

PP2221 P4MM SM PLACE_NEAR=U0600.AY2:7MM

PP2223 P4MM SM PLACE_NEAR=UF600.A3:7MM

OPTION FOR SWD GLITCH MITIGATION <RDAR://88941330>

126 PP1V25_S2

R2290 10K 5% 1/20W TK 0201 117S00090

R2291 10K 5% 1/20W TK 0201 117S00090

R2292 10K 5% 1/20W TK 0201 117S00090

77 69 15 SWD_UPC_SWDIO0

131 32 SWD_UPC_SWDIO2

77 15 SWD_UPC_SWCLK_RR

BKLT BOOST THROTTLE OPTION TO SOC

<RDAR://70197433>

NOSTUFF R2200 0 0% 1/20W TK 0201

137 114 OUT BKLT_BOOST_THROTTLE_L BKLT_BOOST_THROTTLE_R_L IN 96 97

TOUCHID POWER ENABLE PULL UP

<RDAR://72888406>

PP1V25_S2 126

R2210 47K 5% 1/20W TK 0201 117S00129

TOUCHID_PWR_EN 7 112 114 134

INTERNAL DISPLAY HPD PULL DOWN

R2211 47K 5% 1/20W TK 0201 117S00129

LPDP_INT_HPD 10 94 113 137

HDMI HPD PULL DOWN OPTION

NOSTUFF R2212 47K 5% 1/20W TK 0201 117S00129

LPDP_DP2HDMI_HPD 10 117 130 137

998-4756 TP2200 TP-P5

6 BI TP_SOC_HOLD_RESET

998-4756 TP2201 TP-P5

133 7 IN TP_SOC_NUB_CLK_OUT_1

BOM_COST_GROUP=SOC

SYNC_MASTER=PATRICK_X2482_MLB SYNC_DATE=03/04/2022

PAGE TITLE: SOC: PROJECT SUPPORT (3/3)

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DRAWING NUMBER 051-07754 SIZE D

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BRANCH dvt-1

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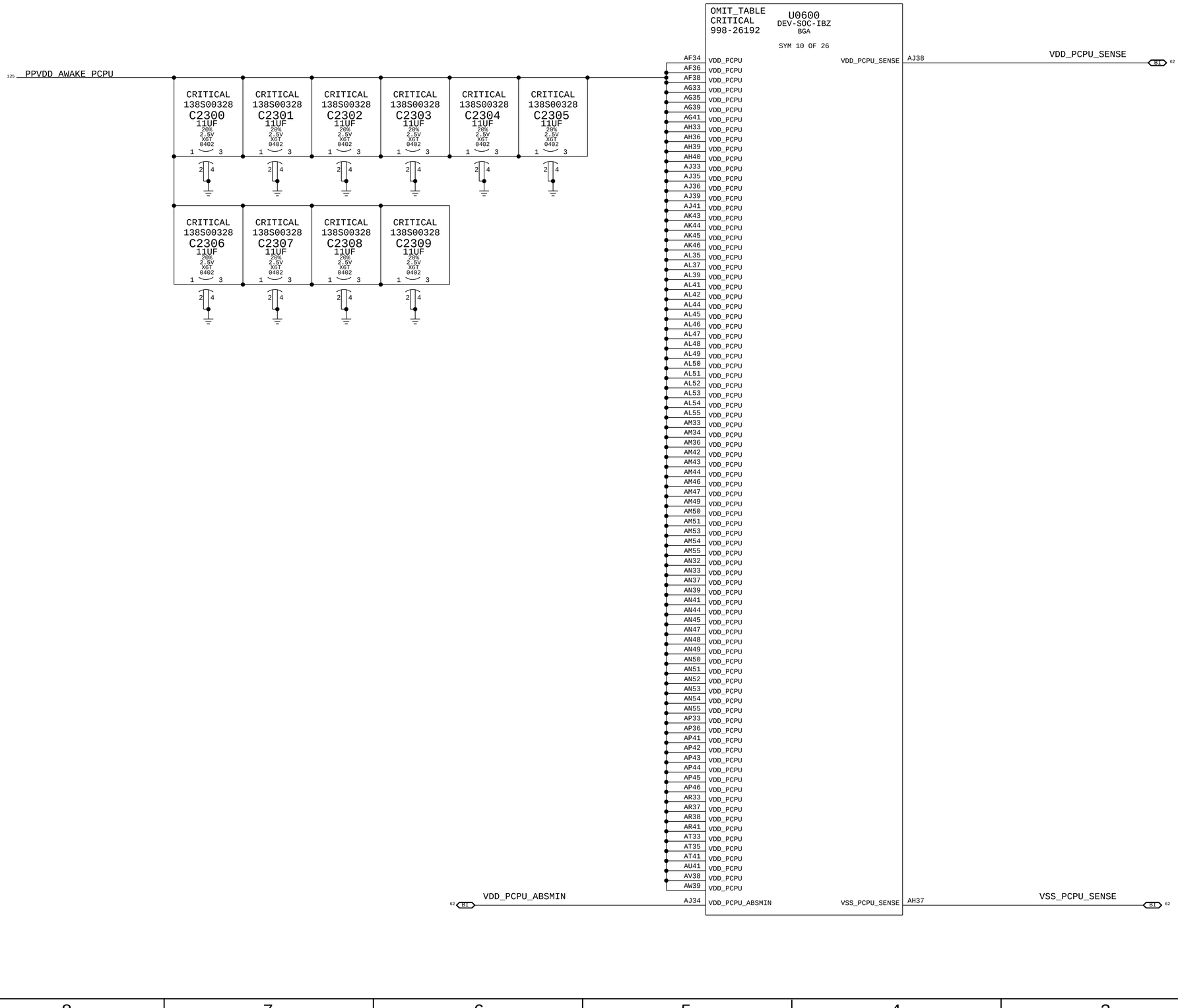

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER PCPU

Apple Inc.

DRAWING NUMBER 051-07754
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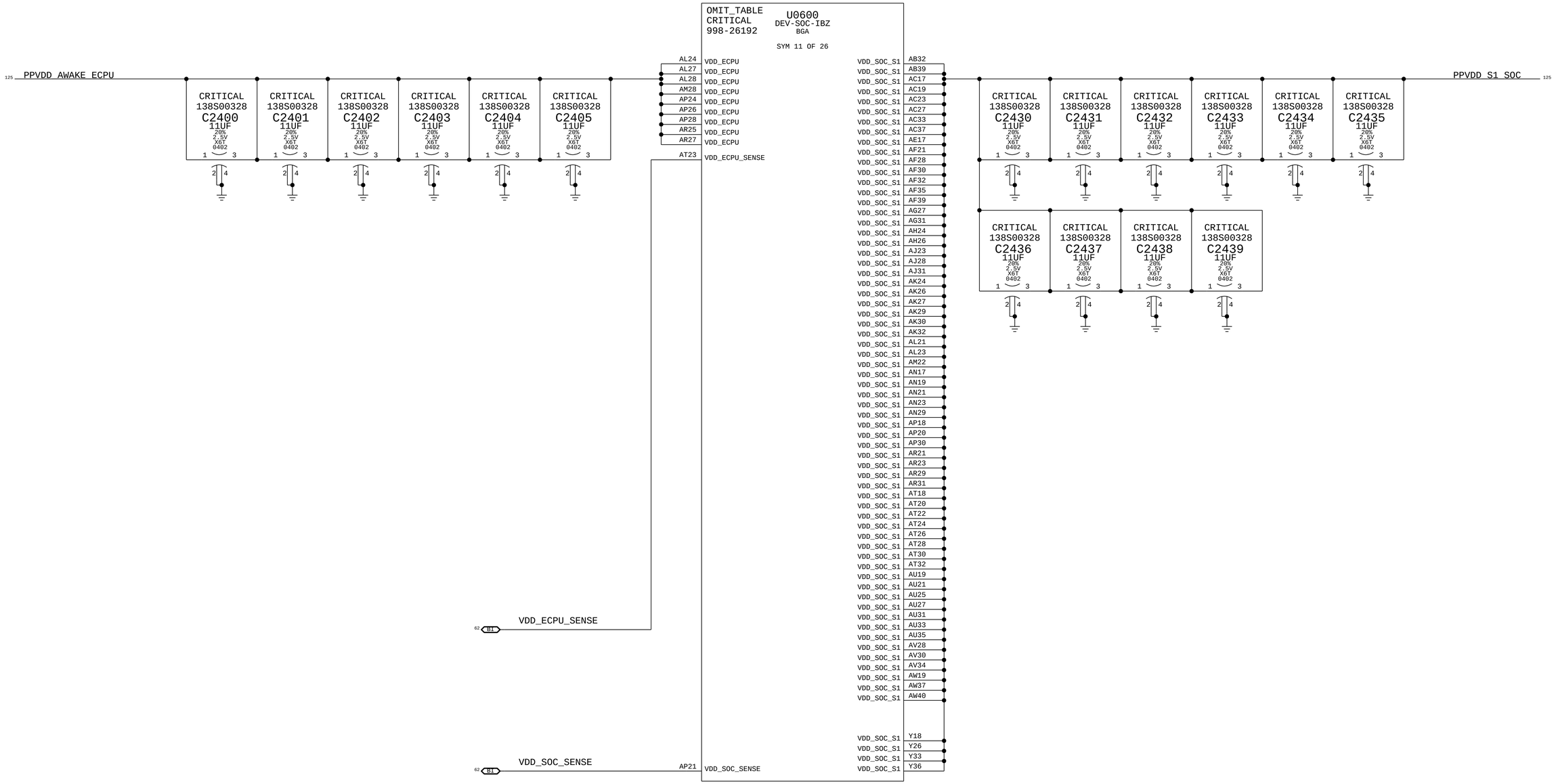

BOM_COST_GROUP=SOC

PAGE TITLE	SOC: POWER ECPU
	Apple Inc.
DRAWING NUMBER	051-07754
SIZE	D
REVISION	6.0.0
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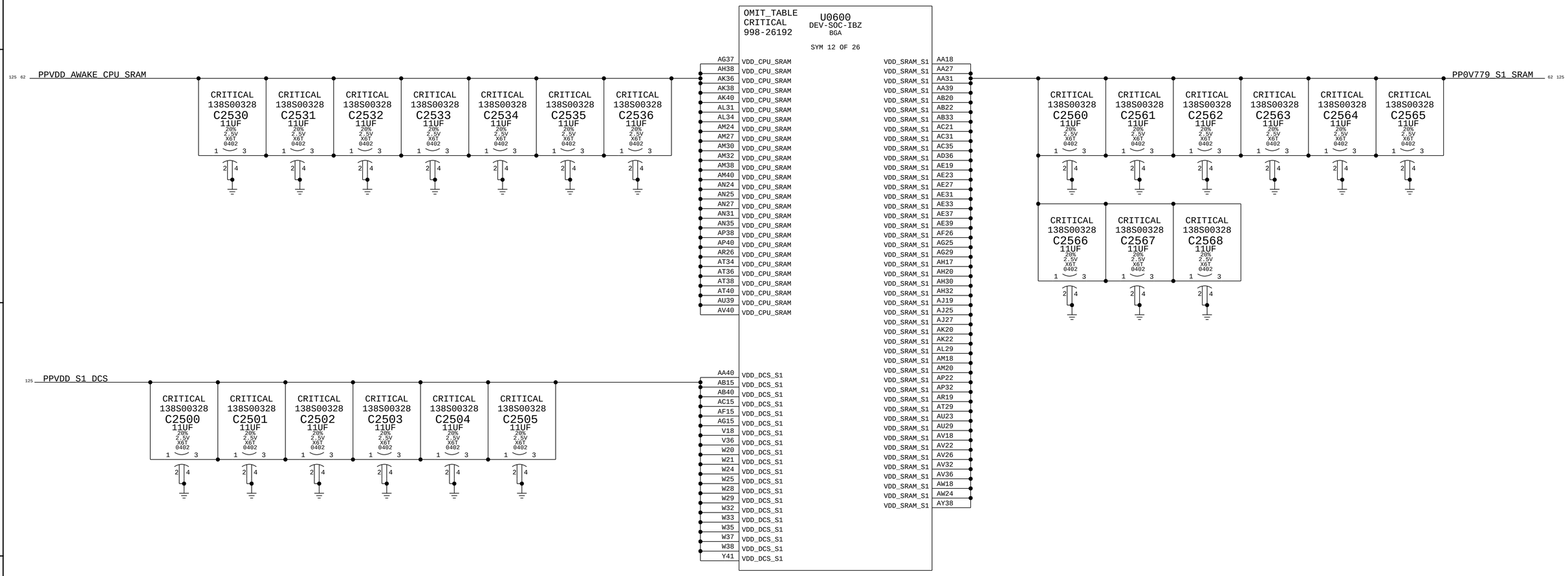

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PAGE TITLE	SOC: POWER SRAM
	Apple Inc.
DRAWING NUMBER	051-07754
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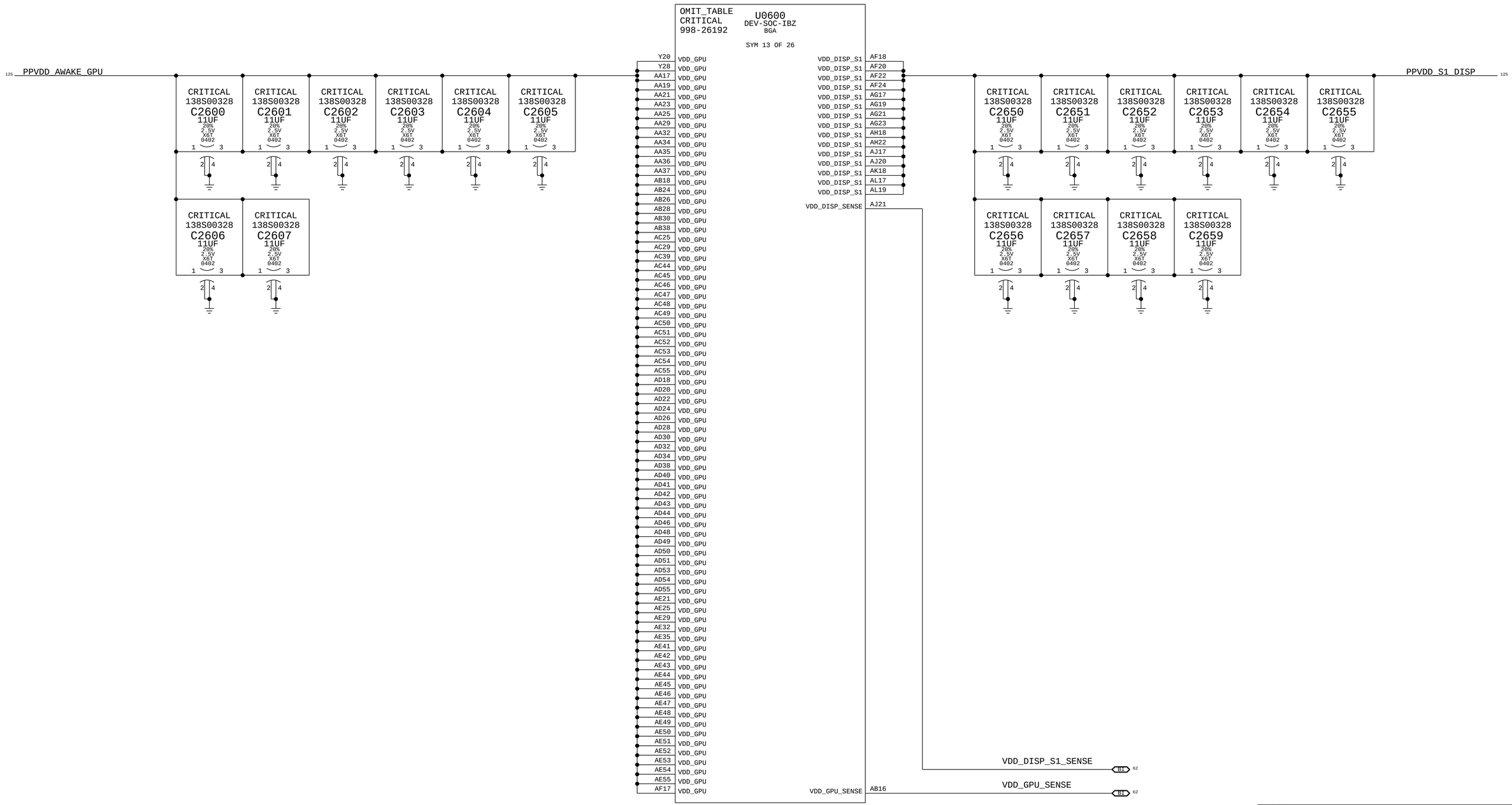

BOM_COST_GROUP=SOC

PAGE TITLE
SOC: POWER GRAPHICS

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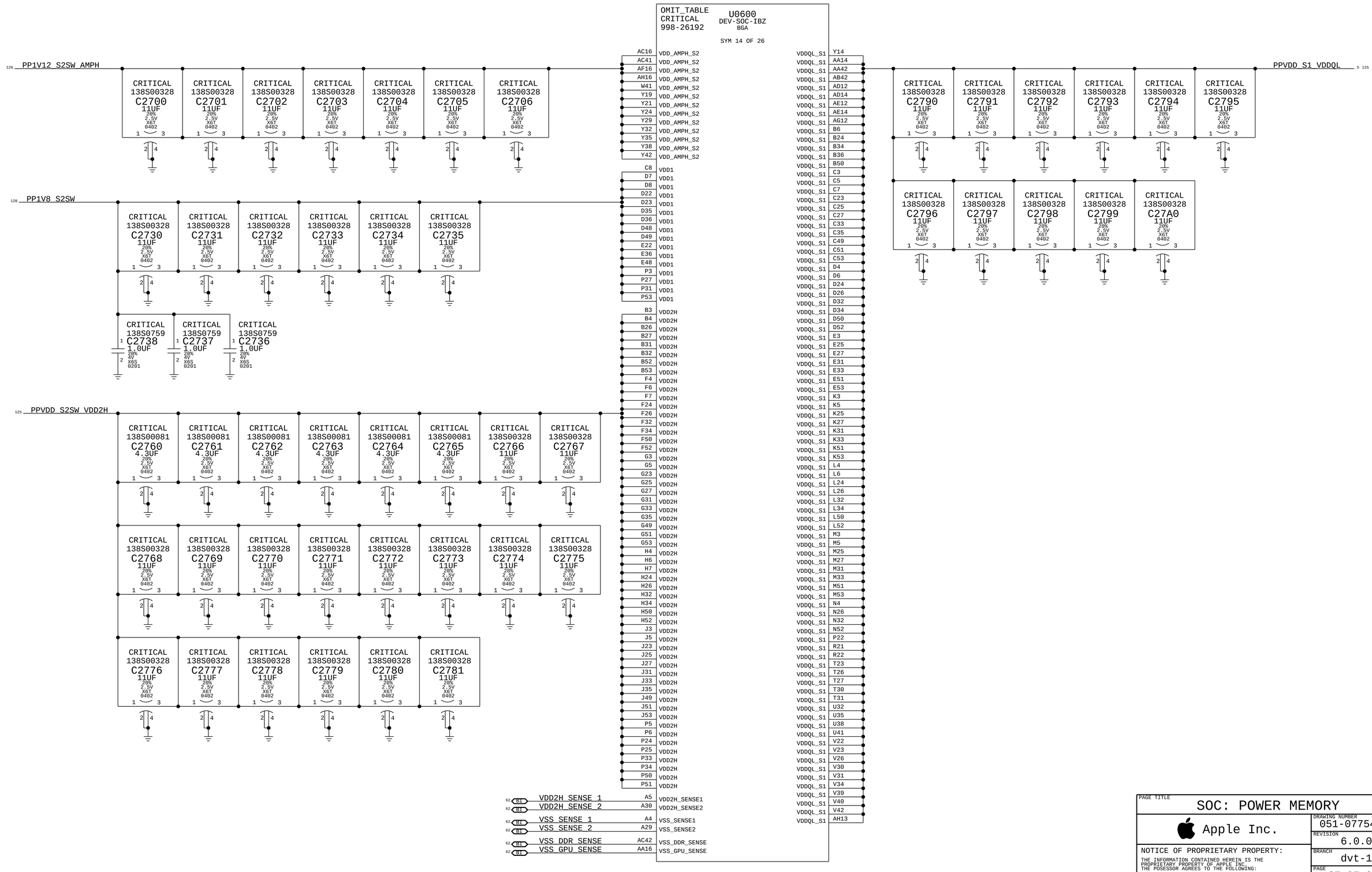

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: POWER MEMORY

Apple Inc.

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BRANCH: dvt-1
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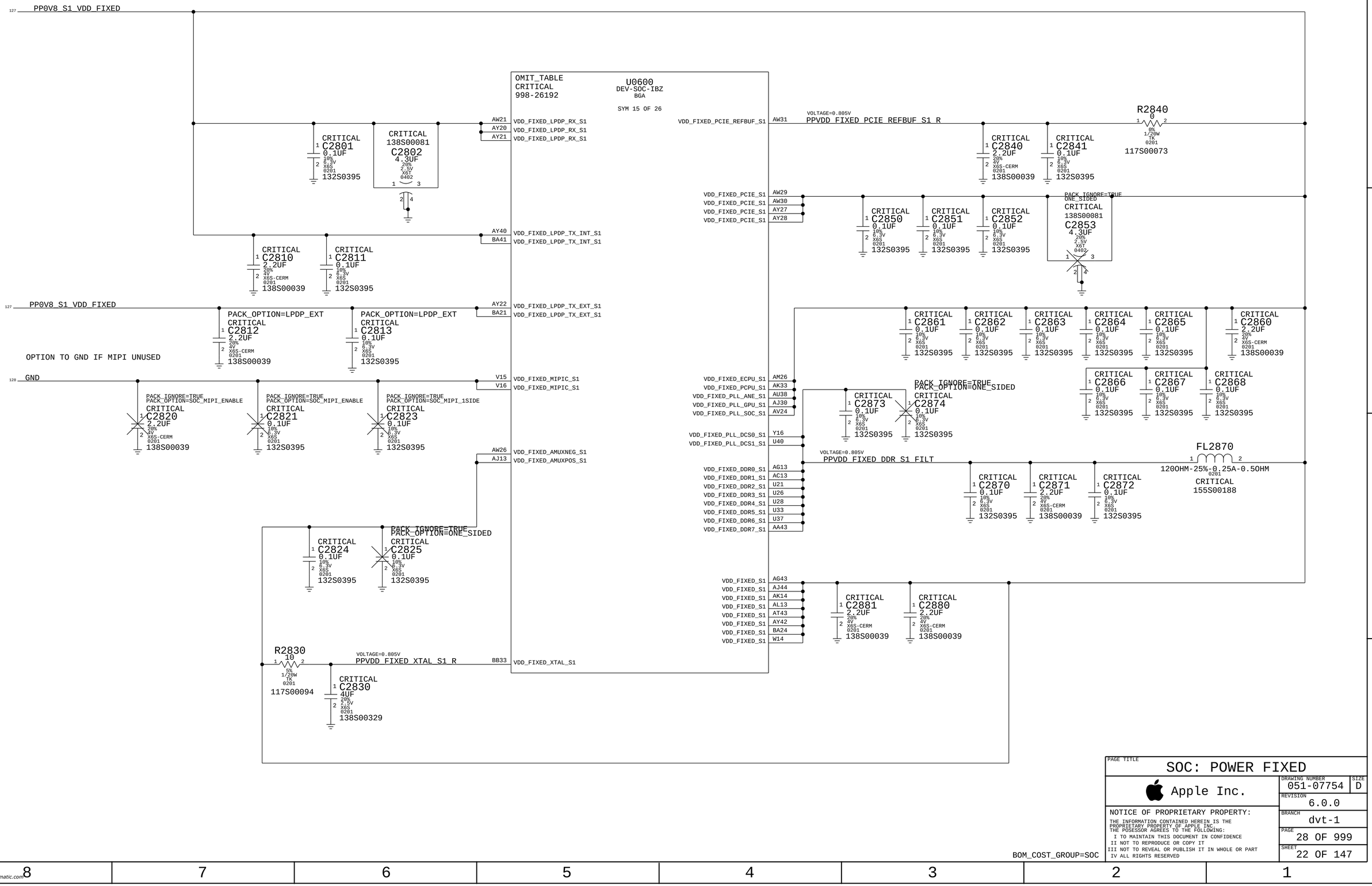

BOM_COST_GROUP=SOC

PAGE TITLE: SOC: POWER FIXED

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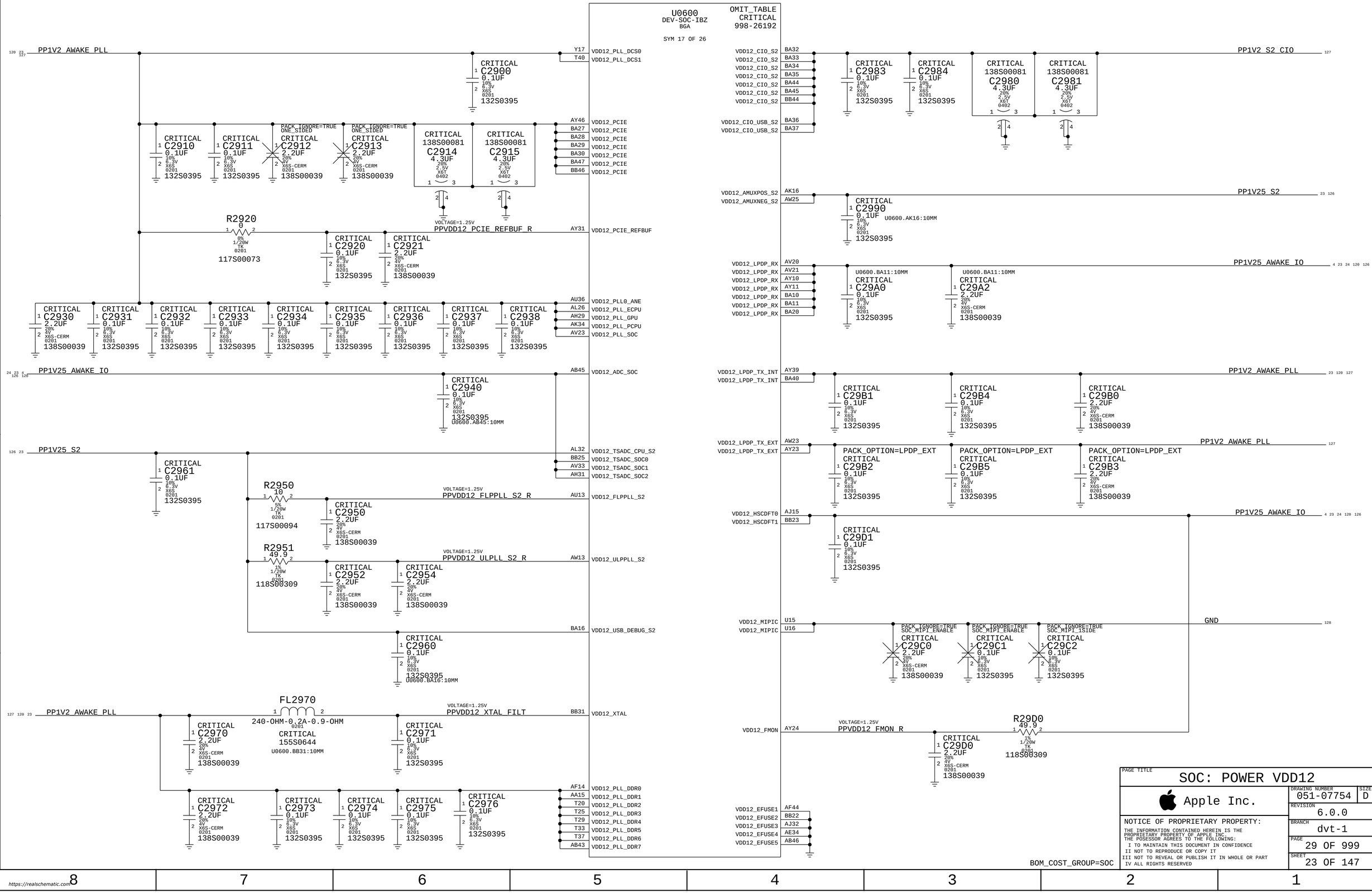
U0600
DEV-SOC-IBZ
BGA
SYM 17 OF 26
OMIT_TABLE
CRITICAL
998-26192
PP1V2 AWAKE PLL
PP1V25 AWAKE IO
PP1V25 S2
PP1V2 S2 CIO
PP1V25 S2
PP1V25 AWAKE IO
PP1V2 AWAKE PLL
PP1V2 AWAKE PLL
PP1V25 AWAKE IO
GND
VOLTAGE=1.25V
PPVDD12_PCIE_REFBUF_R
PPVDD12_FLPPLL_S2_R
PPVDD12_ULPLL_S2_R
PPVDD12_XTAL_FILT
PPVDD12_FMON_R
PACK_IGNORE=TRUE
ONE_SIDED
PACK_OPTION=LPDP_EXT
SOC_MIPI_ENABLE
SOC_MIPI_1SIDE
BOM_COST_GROUP=SOC
PAGE TITLE
SOC: POWER VDD12
Apple Inc.
DRAWING NUMBER 051-07754
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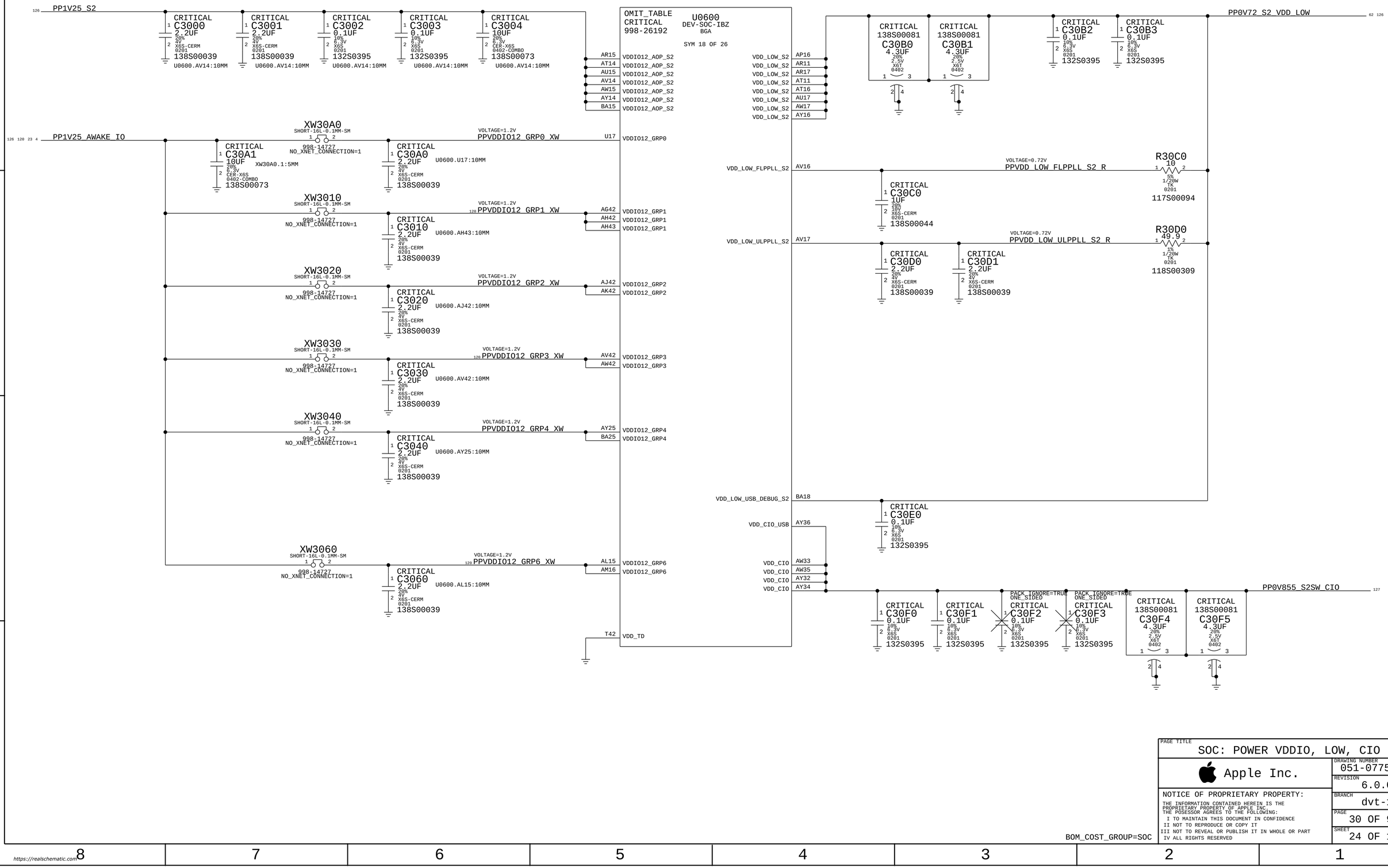

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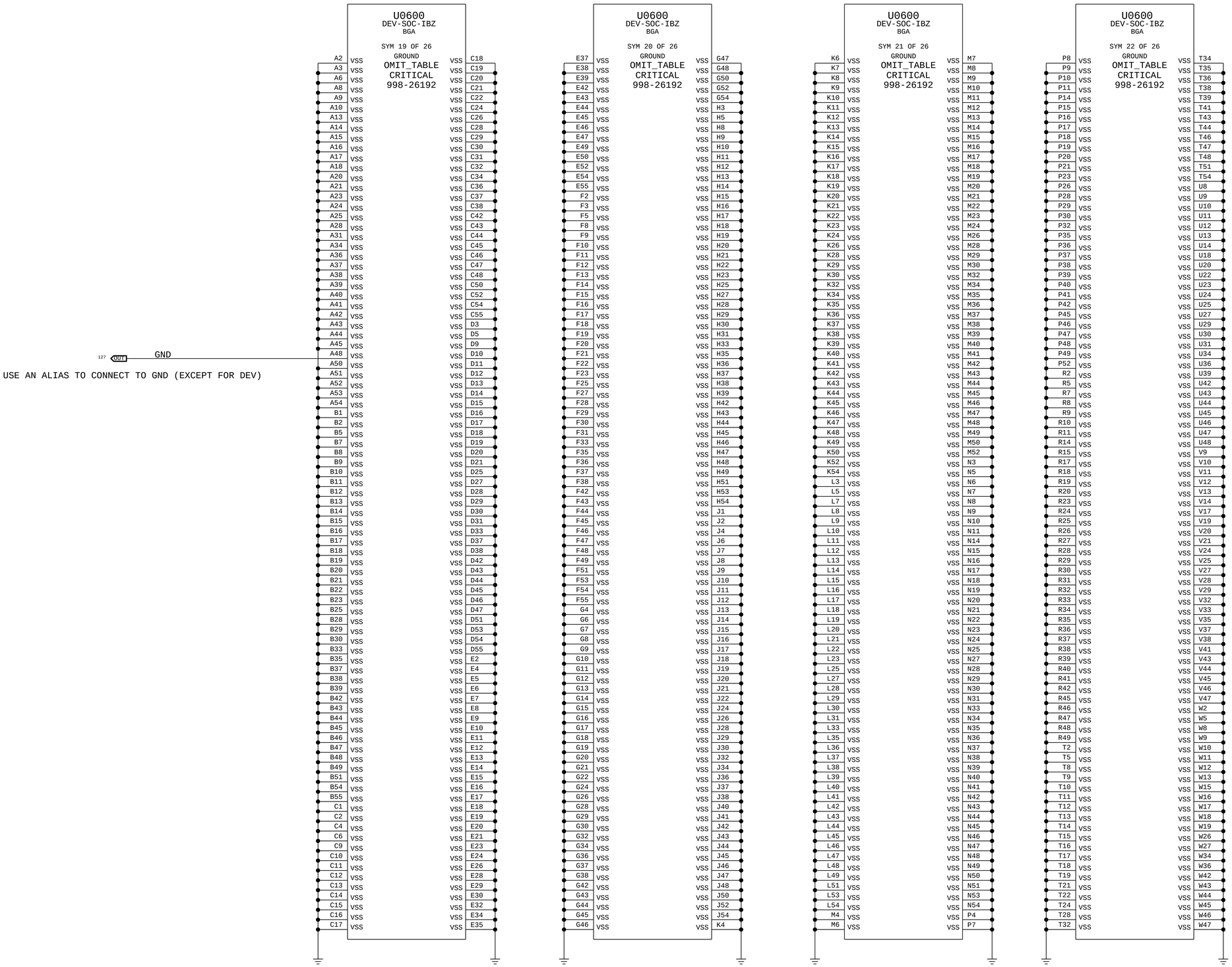

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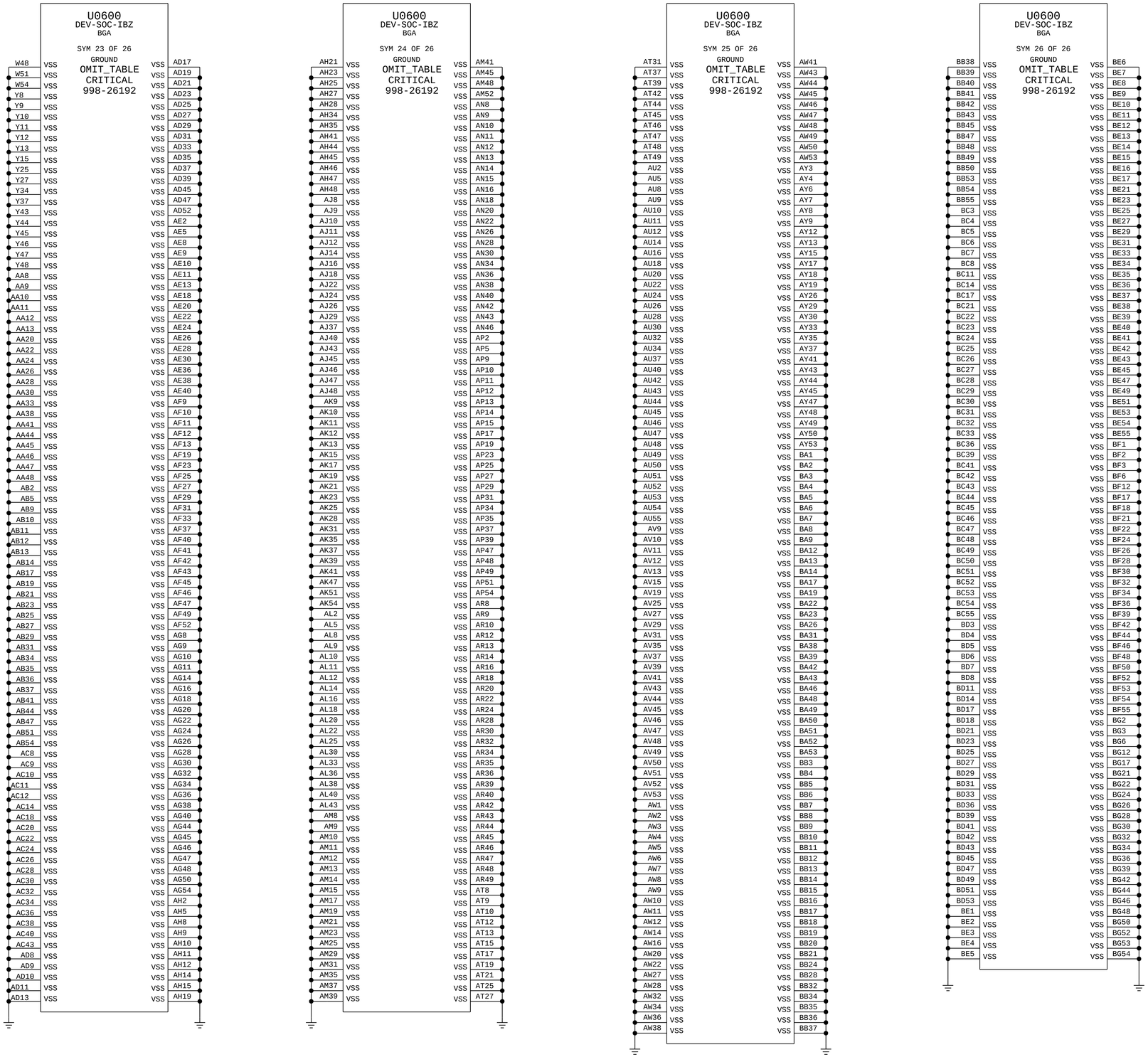

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Eos - Secure Element

If system power budget allows, alias to PP1V25_S2_SE
Otherwise, alias to PP1V8_S2
On B0 silicon, VDDIO_SE is driven by PPVDDCIN,
so choice of source will change SE domain IO voltage

126 PP1V25_S2
Imax 10mA

ROOM=SE_EOS U5000.G8:3mm C5011 0.22UF 20% 6.3V X5R 0201

126 PP1V25_S2
Imax 160mA

VDDC_SE VOLTAGE=3.8
VDDA0_SE VOLTAGE=3.8
VDDA_SE VOLTAGE=3.8
125 27 PP3V8_AON
NC_SE_K1 130
VDDNV_SE VOLTAGE=3.8
VDDRF_SE VOLTAGE=3.8

ROOM=SE_EOS U5000.A6:3mm C5014 1.0UF 20% 6.3V X5R 0201-1
ROOM=SE_EOS U5000.A7:3mm C5010 0.22UF 20% 6.3V X5R 0201
ROOM=SE_EOS U5000.A4:3mm C5009 0.22UF 20% 6.3V X5R 0201
ROOM=SE_EOS U5000.G1:3mm C5008 0.22UF 20% 6.3V X5R 0201
ROOM=SE_EOS U5000.J6:3mm C5051 1.0UF 20% 6.3V X5R 0201-1
ROOM=SE_EOS U5000.K2:3mm C5017 0.22UF 20% 6.3V X5R 0201
ROOM=SE_EOS U5000.C2:3mm C5018 0.1UF 10% 6.3V CERM-X5R 0201
ROOM=SE_EOS U5000.B8:3mm C5016 0.22UF 20% 6.3V X5R 0201

PP3V8_AON 27 125

U5000
SN300VUK/B017W0
WLCSP
OMIT_TABLE

B7	PMUVCC		
C8	SIMVCC		NC
C1	VDDBOOST		
G1	VDDA		
A4	VDDA0		
A7	VDDC		
A6	VDDCIN_IO_SE		
G8	VDDIO		
G2	VDDIO_AO		
D8	VDDIO_ISO		
B8	VDDNV		
J8	VDDPA		
K1	VDDPLL		
K2	VDDRF		
H8	VUP		
J6	VBAT		
A3	VBATPWR		
B3	VBATPWR		
B4	VBATLIN		
J4	AIO1		NC
H2	AIO2		NC
H5	AIO3		NC
J1	NFC_CLK_XTAL1		NC
G4	NFC_GPIO0	130 SE_NFC_GPIO0	
G5	NFC_GPIO1	130 SE_NFC_GPIO1	
G3	NFC_GPIO2_AO		NC
E1	NFC_GPIO3_AO	130 SE_IRQ_WAKE	
H6	NFC_GPIO4_AO		NC
F7	NFC_GPIO5		NC
F2	NFC_GPIO6		NC
G6	NFC_I3C_SCL	130 I3C_SE_NFC_SCL	
F3	NFC_I3C_SDA	130 I3C_SE_NFC_SDA	
B6	NFC_SIM_SWIO1		NC
C7	NFC_SIM_SWIO2		NC
G7	NFC_SPMI_SCLK	117 15 IN SPMI_SE_CLK	
F6	NFC_SPMI_SDATA	117 15 BI SPMI_SE_DATA	
H1	NFC_XTAL2		NC
K4	RXP		
K3	RXN		
H4	TM		NC
C2	SE_GPIO0	SE_GPIO0	130
D3	SE_GPIO1	SE_GPIO1	130
E2	SE_GPXC		NC
D1	SE_GPXI		NC
E8	SE_I2C_SCL	I2C_SE_SCL	130
C6	SE_I2C_SDA	I2C_SE_SDA	130
D5	SE_I3C_SCL	I3C_SE_SCL	130
D4	SE_I3C_SDA	I3C_SE_SDA	130
E3	SE_ISO_CLK		NC
D2	SE_ISO_IO		NC
C5	SE_ISO_RST		NC
E7	SE_SPI_CLK		NC
E4	SE_SPI_CS		NC
E6	SE_SPI_MISO		NC
E5	SE_SPI_MOSI		NC
D7	SE_SPMI_SCLK		NC
D6	SE_SPMI_SDATA		NC
K5	RXVMID		NC
J7	TXVMID		NC
K8	TX1	NC_SE_K8	130
K6	TX2		NC
A1	BOOST_LX		
B1	BOOST_LX	PP3V8_AON	27 125
F5	RSTN*	SE_PWR_EN	IN 46 117
J2	VREF	VREF_SE VOLTAGE=3.8	
F4	VSS_DIG		
A8	VSS_DIG		
C3	VSS_DIG		
C4	VSS_DIG		
F8	VSS_DIG		
F1	VSS_A		
K7	VSS_PA		
J3	VSS_RFPLL		
A5	VSS_PMU		
A2	VSS_PWR		
B2	VSS_PWR		
H7	VSS_SUB		
B5	VSS_SUB		
H3	VSS_SUB		

ROOM=SE_EOS U5000.J2:3mm C5013 0.1UF 10% 6.3V CERM-X5R 0201

Alias NFC_GPIO0 to a TP net for debug
Alias NFC_GPIO1 to a TP net for debug if space permits

Connect NFC_GPIO3 to an SoC AOP_FUNC GPIO

ROOM=SE_EOS R5050 1M 5% 1/20W TK 0201
ROOM=SE_EOS R5051 1M 5% 1/20W TK 0201

SE and NFC GPIO, I2C, and I3C are not used on the architectural roadmap as of 9/15/21 and should be NC'd on all form factor designs, with the exception of NFC_GPI01/2/3 per inline notes

Support for Eos A1 Silicon has been removed from the reference design following V0.1.0

<rdar://problem/59254645> [SN300V] Data Sheet
<rdar://problem/71610778> [SN300V] Wired Mode SE Only Reference Design Material

BOM_COST_GROUP=SECURE ELEMENT

PAGE TITLE: Secure Element

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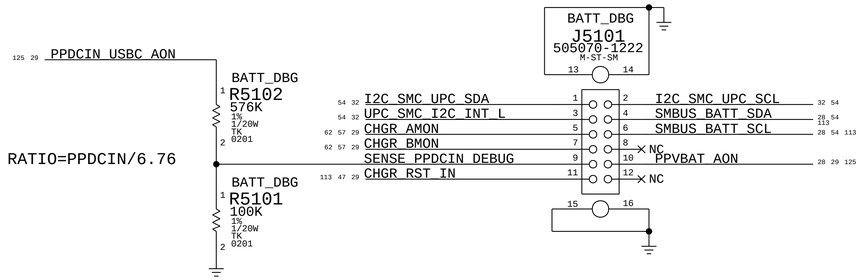
Battery Sub-System Debug Connector

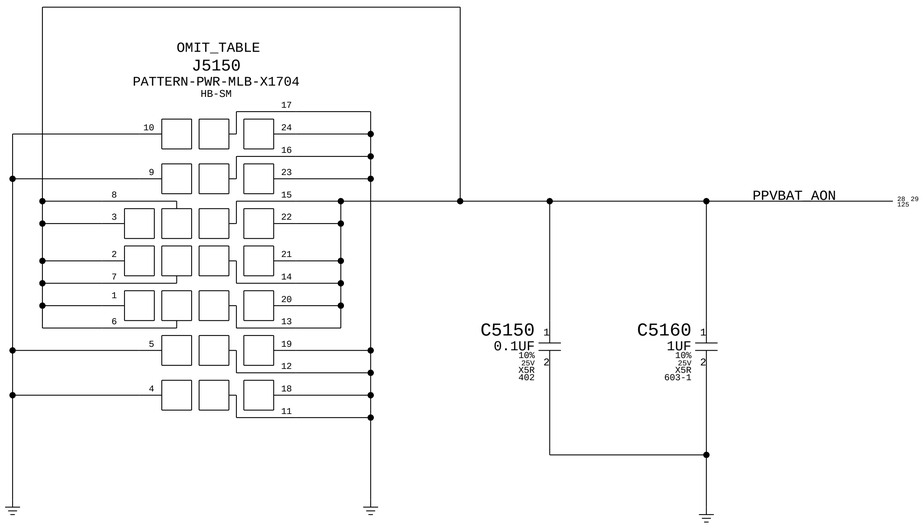
ARKANOID CONN

BMU POWER FLEX HOTBAR'd TO THE MLB:

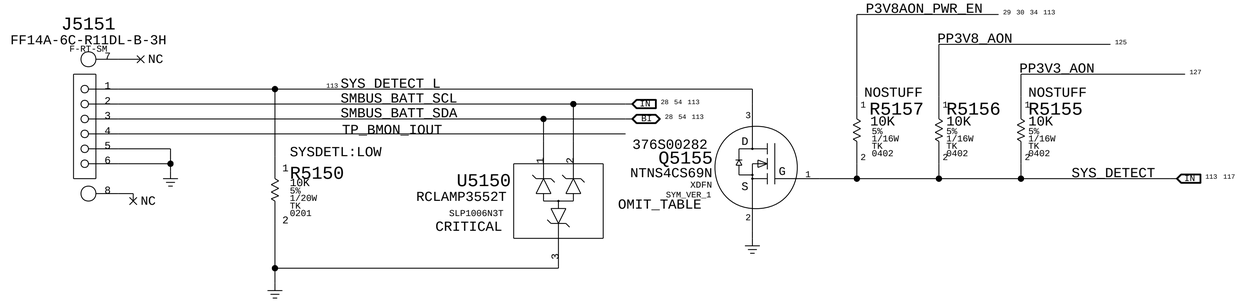
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-04146	1	PCBA,FLEX,BMU-POWER,X1703	J5150	CRITICAL	

ARKANOID	MLB Connector / Signals		Saleae
J0301 - 1	6	SMBUS_BATT_SCL (= I2C_SMC_PWR_SCL)	0
J0301 - 3	4	SMBUS_BATT_SDA (= I2C_SMC_PWR_SDA)	1
J0301 - 5	2	I2C_SMC_UPC_SCL	2
J0301 - 7	1	I2C_SMC_UPC_SDA	3
J0302 - 1	3	UPC_SMC_I2C_INT_L	4
J0302 - 3	5	CHGR_AMON	5
J0302 - 5	7	CHGR_BMON	6
J0302 - 7	9	1 / 6.76 * PPDCIN_AON	7
J0303 - 1	11	CHGR_RST_IN	8
J0303 - 3	12	—	9
J0303 - 5	10	PPVBAT_AON	10
J0303 - 7	8	—	11





APN:518S0818



BOM_COST_GROUP=BATTERY

PAGE TITLE	BATTERY CONN
	Apple Inc.
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*** OK2INTEGRATE ***

PPDCIN_AON_CHGR_R
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1800
VOLTAGE=20V

C520A 2.2UF 20% 35V X5R-CERM 0402-0.1MM 138S00030
C520B 2.2UF 20% 35V X5R-CERM 0402-0.1MM 138S00030
C520C 2.2UF 20% 35V X5R-CERM 0402-0.1MM 138S00030
C520D 2.2UF 20% 35V X5R-CERM 0402-0.1MM 138S00030
PACK_OPTION=CHGR_MLCC-STD

CRITICAL C5209 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT 128S00011
CRITICAL C5210 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT 128S00011
NOSTUFF
CRITICAL C520A 2.2UF 20% 35V X5R 0402-THICKSTNCL-COMBO 138S00409
CRITICAL C520B 2.2UF 20% 35V X5R 0402-THICKSTNCL-COMBO 138S00409
CRITICAL C520C 2.2UF 20% 35V X5R 0402-THICKSTNCL-COMBO 138S00409
CRITICAL C520D 2.2UF 20% 35V X5R 0402-THICKSTNCL-COMBO 138S00409
PACK_IGNORE=TRUE
PACK_OPTION=CHGR_MLCC-LN

CRITICAL C5202 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT 128S00011
CRITICAL C5203 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT 128S00011
CRITICAL C5204 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT 128S00011
CRITICAL C5205 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT 128S00011
CRITICAL C5206 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT 128S00011
CRITICAL C5207 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT 128S00011

CRITICAL R5220 0.01 0.5% 1W MF 0612-1-COMBO 107S00044

FROM USB-C SOURCE
PPDCIN_USBC_AON

CRITICAL C5201 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT 128S00011
CRITICAL C5208 6.8UF 20% 35V-0.090OHM POLY-TANT CASE-B1-B3-COMBO CAPMAT=POLY-TANT 128S00011

NO_XNET_CONNECTION=1
(AMON)
2-CELL: 0.02 OHM
3-CELL: 0.01 OHM

Consult DCDC DRI before removing PP

TP5201 CHGR_GATE_Q1 TP-P4 998-4704 PLACE_SIDE=TOP
TP5202 CHGR_GATE_Q2 TP-P4 998-4704 PLACE_SIDE=TOP
TP5203 CHGR_GATE_Q3 TP-P4 998-4704 PLACE_SIDE=TOP
TP5204 CHGR_GATE_Q4 TP-P4 998-4704 PLACE_SIDE=TOP
TP5207 P3V8AON_PWR_EN TP-P4 998-4704 PLACE_SIDE=BOTTOM
TP5208 CHGR_INT_1V8_L TP-P4 998-4704 PLACE_SIDE=BOTTOM

CHGR_CSI_P
PLACE_NEAR=U5200.D5:2MM
R5221 1 1% 1/20W TK 0201 118S00397
CHGR_CSI_FILT_P
132S00261
CRITICAL C5221 0.1UF 10% 25V X7R CERM-X7R 0402

CHGR_CSI_N
PLACE_NEAR=U5200.C5:2MM
R5222 1 1% 1/20W TK 0201 118S00397
CHGR_CSI_FILT_N
132S0640
CRITICAL C5222 0.047UF 10% 25V X7R CER-X7R 0402

132S0257
CRITICAL C5220 0.47UF 20% 4V CERM-X5R-1 201
NO_XNET_CONNECTION=1

PPVBAT_AON_CHGR_REG
CRITICAL C5278 2.2UF 20% 25V X6S-CERM 0402 138S00042
CRITICAL C5278 2.2UF 20% 25V X6S 0402-THICKSTNCL-COMBO 138S00410
PACK_IGNORE=TRUE
PACK_OPTION=CHGR_MLCC-LN

PACK_OPTION=CHGR_MLCC-STD
PPDCIN_USBC_AON
118S00393
R5215 787K 1% 1/20W TK 0201

CHGR_AUX_DET
NOSTUFF
CRITICAL C5216 0.01UF 10% 25V X5R-CERM 0201 132S0391
118S00358
R5216 158K 1% 1/20W TK 0201

<RDAR://68945820>
MAGSAFE: ACE GPIO6
USBC: ACE GPIO5
CRITICAL Q5216 SSM3K15AFS SOT523-3 376S00544
CHGR_AUX_DET_SHORT_3V3
R5217 10K 5% 1/20W TK 0201 117S00090

PP1V8_S2
C5280 1.0UF 20% 6.3V X5R 0201-1 138S0692

SMBUS_CHGR_1V8_SDA
SMBUS_CHGR_1V8_SCL
CHGR_RST_IN
CHGR_COMP
132S00180 CRITICAL C5270 0.12UF 10% 10V X5R 0402
132S00180 CRITICAL C5271 0.12UF 10% 10V X5R 0402
H:3-CELL
L:2-CELL

CHGR_PHASE1
NOSTUFF R5235 1.5 5% 0.1W 0603 TK 110S00153
CHGR_SNB1 DIDT=TRUE SWITCH_NODE=TRUE
NOSTUFF C5235 150PF 5% 50V C0G-CERM 0402 131S0514

CHGR_PHASE2
NOSTUFF R5245 1.5 5% 0.1W 0603 TK 110S00153
CHGR_SNB2 DIDT=TRUE SWITCH_NODE=TRUE
NOSTUFF C5245 150PF 5% 50V C0G-CERM 0402 131S0514

152S01218
CRITICAL L5230 2.7UH-20%-16A-0.0148OHM
BMCBEJ-SM-COMBO

CHGR_PHASE1 DIDT=TRUE SWITCH_NODE=TRUE
CHGR_PHASE2 DIDT=TRUE SWITCH_NODE=TRUE

Q5230 NTTFD4D1N03P1E WDFN8
CRITICAL
V+ V+ V+ GND GND HSG SW LSG
376S00519
Q5240 NTTFD4D1N03P1E WDFN8
CRITICAL
GND GND V+ V+ V+ LSG SW HSG
376S00519

CHGR_GATE_Q1_R DIDT=TRUE SWITCH_NODE=TRUE
R5251 0 5% 1/16W MF 0402-1 116S00044
CHGR_GATE_Q1 DIDT=TRUE SWITCH_NODE=TRUE

CHGR_GATE_Q2_R DIDT=TRUE GATE_NODE=TRUE
R5252 0 5% 1/16W MF 0402-1 116S00044
CHGR_GATE_Q2 DIDT=TRUE GATE_NODE=TRUE

CHGR_GATE_Q3_R DIDT=TRUE GATE_NODE=TRUE
R5253 0 5% 1/16W MF 0402-1 116S00044
CHGR_GATE_Q3 DIDT=TRUE GATE_NODE=TRUE

CHGR_GATE_Q4_R DIDT=TRUE SWITCH_NODE=TRUE
R5254 0 5% 1/16W MF 0402-1 116S00044
CHGR_GATE_Q4 DIDT=TRUE SWITCH_NODE=TRUE

SHORT-12L-0.25MM-SM
XW5230 998-2075
XW5240 998-2075

CHGR_LX1 DIDT=TRUE SWITCH_NODE=TRUE
CRITICAL C5230 0.1UF 10% 25V X7R-CERM-1 0402 132S0438
CHGR_BOOT1_RC DIDT=TRUE SWITCH_NODE=TRUE
R5230 0 5% 1/16W MF 0402-1 116S00044
CHGR_BOOT1 DIDT=TRUE SWITCH_NODE=TRUE

CHGR_LX2 DIDT=TRUE SWITCH_NODE=TRUE
CRITICAL C5240 0.1UF 10% 25V X7R-CERM-1 0402 132S0438
CHGR_BOOT2_RC DIDT=TRUE SWITCH_NODE=TRUE
R5240 0 5% 1/16W MF 0402-1 116S00044
CHGR_BOOT2 DIDT=TRUE SWITCH_NODE=TRUE

VOLTAGE=5V
PP5V_CHGR_SW
R5274 0 0% 1/20W TK 0201 117S00073
R5275 4.7 5% 1/20W 0201 117S00062
R5276 TK 1/20W 0201 117S00109

VOLTAGE=5V
PPCHGR_VDDA
CRITICAL C5275 2.2UF 20% 25V X5R-CERM 0402-1 138S0769
VOLTAGE=5V
PPCHGR_VDDP
CRITICAL C5277 10UF 20% 25V X5R-CERM 0603 138S0696

U5200
RAA489900-6
WLCSP
353S02990
CRITICAL
OMIT_TABLE

B5	P_IN	GATE_Q1	H1
C5	CSIN	BOOT1	F1
D5	CSIP	LX1	G1
A5	PBUS_PWR	GATE_Q2	E1
D3	AUX_DET	GATE_Q3	D1
		LX2	B1
		BOOT2	C1
		GATE_Q4	A1
A3	PBUS_Q4SNS		
A4	CSOP		
B4	CSON		
B3	BGATE		
C3	VBAT		
F2	EN_VR1		
H4	SMC_RST*		
H3	IRQ_L		
H2	CBC_ON		
F4	(5V) EN_MVR		
F3	(OD) AUX_OK		
D4	AMON		
C4	BMON		
F5	VDDIO1P8		
G5	SDA		
H5	SCL		
G2	SMC_RST_IN		
G3	HPWR_EN*		
E5	COMP		
G4	CELL		
B2	NC0		
C2	NC1		
E4	NC2		
E3	AGND		
E2	PGND		

CHGR_PBUS_SNS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
CHGR_BGATE
CHGR_VBAT
TP_CHGR_EN_VR1
TP_CHGR_SMC_RST_L
CHGR_INT_1V8_L
TP_CHGR_CBC_ON
CHGR_EN_MVR
CHGR_AUX_OK
CHGR_AMON
CHGR_BMON

ID REGISTER 0XFF => 0X000D

XW5260 SM
PLACE_NEAR=Q5240.3:2MM
998-0313

CHGR_CSO_P
PLACE_NEAR=U5200.A4:2MM
R5261 1 1% 1/20W TK 0201 118S00397
CHGR_CSO_FILT_P
132S0640
CRITICAL C5261 0.047UF 10% 16V X7R CER-X7R 0402

CHGR_CSO_N
PLACE_NEAR=U5200.B4:2MM
R5262 1 1% 1/20W TK 0201 118S00397
CHGR_CSO_FILT_N
132S0640
CRITICAL C5262 0.047UF 10% 16V X7R CER-X7R 0402

CRITICAL C5260 0.47UF 20% 4V CERM-X5R-1 201 132S0257
NO_XNET_CONNECTION=1

NO_XNET_CONNECTION=1
CRITICAL R5260 0.005 (BMON) 1% 1.5W MF 0612-4T 107S00232
3-CELL: 0.010 OHM
3-CELL: 0.005 OHM

CRITICAL C5256 2.2UF 20% 25V X6S-CERM 0402 138S00042
CRITICAL C5257 2.2UF 20% 25V X6S-CERM 0402 138S00042
CRITICAL C5256 2.2UF 20% 25V X6S 0402-THICKSTNCL-COMBO 138S00410
CRITICAL C5257 2.2UF 20% 25V X6S 0402-THICKSTNCL-COMBO 138S00410
CRITICAL C5258 1000PF 10% 25V X7R 0201 132S00052
PACK_OPTION=CHGR_MLCC-STD
PACK_IGNORE=TRUE
PACK_OPTION=CHGR_MLCC-LN

CAPDERATE CRITICAL C5252 33UF 20% 16V TANT CASE-T 128S00009
CAPDERATE CRITICAL C5253 33UF 20% 16V TANT CASE-T 128S00009
CAPDERATE CRITICAL C5254 33UF 20% 16V TANT CASE-T 128S00009
CAPDERATE CRITICAL C5255 33UF 20% 16V TANT CASE-T 128S00009
CAPDERATE CRITICAL C5282 33UF 20% 16V TANT CASE-T 128S00009
CAPDERATE CRITICAL C5283 33UF 20% 16V TANT CASE-T 128S00009
CAPDERATE CRITICAL C5284 33UF 20% 16V TANT CASE-T 128S00009
CAPDERATE CRITICAL C5285 33UF 20% 16V TANT CASE-T 128S00009
PACK_OPTION=CHGR_PBUS16V_33UF

CAPDERATE CRITICAL C5252 27UF 20% 16V TANT-POLY CASE-B12 128S00107
CAPDERATE CRITICAL C5253 27UF 20% 16V TANT-POLY CASE-B12 128S00107
CAPDERATE CRITICAL C5254 27UF 20% 16V TANT-POLY CASE-B12 128S00107
CAPDERATE CRITICAL C5255 27UF 20% 16V TANT-POLY CASE-B12 128S00107
CAPDERATE CRITICAL C5282 27UF 20% 16V TANT-POLY CASE-B12 128S00107
CAPDERATE CRITICAL C5283 27UF 20% 16V TANT-POLY CASE-B12 128S00107
CAPDERATE CRITICAL C5284 27UF 20% 16V TANT-POLY CASE-B12 128S00107
CAPDERATE CRITICAL C5285 27UF 20% 16V TANT-POLY CASE-B12 128S00107
PACK_IGNORE=TRUE
PACK_OPTION=CHGR_PBUS18V

CRITICAL F5200 12A-32V-0.0045OHM 1206
TO SYSTEM
PPBUS_AON
CRITICAL F5201 12A-32V-0.0045OHM 1206

CRITICAL C5250 68UF 20% 16V POLY-TANT CASE-D2E-SM-1 128S0364
CRITICAL C5251 68UF 20% 16V POLY-TANT CASE-D2E-SM-1 128S0364
CRITICAL C5252 68UF 20% 16V POLY-TANT CASE-D2E-SM-1 128S0364
CRITICAL C5253 68UF 20% 16V POLY-TANT CASE-D2E-SM-1 128S0364
PACK_IGNORE=TRUE CHGR_PBUS16V_68UF

PPVBAT_AON_CHGR_REG
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
VOLTAGE=13.05V

PPVBAT_AON_CHGR_R
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=13.05V

CRITICAL C5265 2.2UF 20% 25V X6S-CERM 0402 138S00042
CRITICAL C5266 2.2UF 20% 25V X6S-CERM 0402 138S00042
CRITICAL C5265 2.2UF 20% 25V X6S 0402-THICKSTNCL-COMBO 138S00410
CRITICAL C5266 2.2UF 20% 25V X6S 0402-THICKSTNCL-COMBO 138S00410
CRITICAL C5267 0.1UF 10% 25V X5R 0201 132S0534
CRITICAL C5268 0.01UF 10% 25V X5R-CERM 0201 132S0391
PACK_OPTION=CHGR_MLCC-STD
PACK_IGNORE=TRUE
PACK_OPTION=CHGR_MLCC-LN

376S0761
CRITICAL Q5265 SI7137DP SO-8-COMBO SYM-VER-2

TO/FROM BATTERY
PPVBAT_AON
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=13.05V

132S0534
CRITICAL C5269 0.1UF 10% 25V X5R 0201
C5264 1000PF 10% 25V X7R 0201 132S00052
132S00390
CRITICAL C5263 4700PF 10% 25V X5R-CERM 0201-1
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

XW5263 SM 998-0313

CHGR_VBAT_XW
CRITICAL Q5270 376S00282 NTNS4CS69N XDFN SYM_VER_1 OMIT_TABLE
<rdar://37259372&39763505>
SAVE_BAT_S
SAVE_BAT_G
R5270 24K 5% 1/20W TK 0201 117S00119
R5263 1K 5% 1/20W TK 0201-1 117S00077
PPDCIN_USBC_AON
118S00364
R5271 200K 1% 1/20W TK 0201
CRITICAL D5270 DFN0201 ALLOW_APPLE_PREFIX=D DZD5V6LP3-55 371S00307

BOM_COST_GROUP=BATTERY

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02633	1	RAA489900,PMIC,WHAMOLA,OTP-2,WCSP40	U5200	CRITICAL	WHAMOLA:0A5
353S02990	1	RAA489900,PMIC,WHAMOLA,OTP-6,WCSP40	U5200	CRITICAL	WHAMOLA:0A5-13V7

PAGE TITLE
PBUS SUPPLY & BATTERY CHARGER

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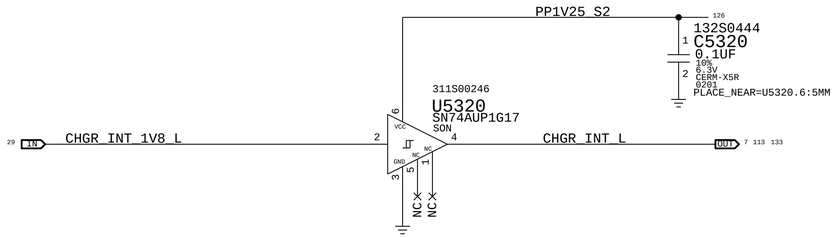
*** OK2INTEGRATE ***

CHGR I2C Level Translation

SMBUS_CHGR_1V8_[SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

CHGR_INT_L Level Translation

Stuff R5320 in case, glitch during power sequencing is a concern.



CHGR_AUX_OK Pull Up

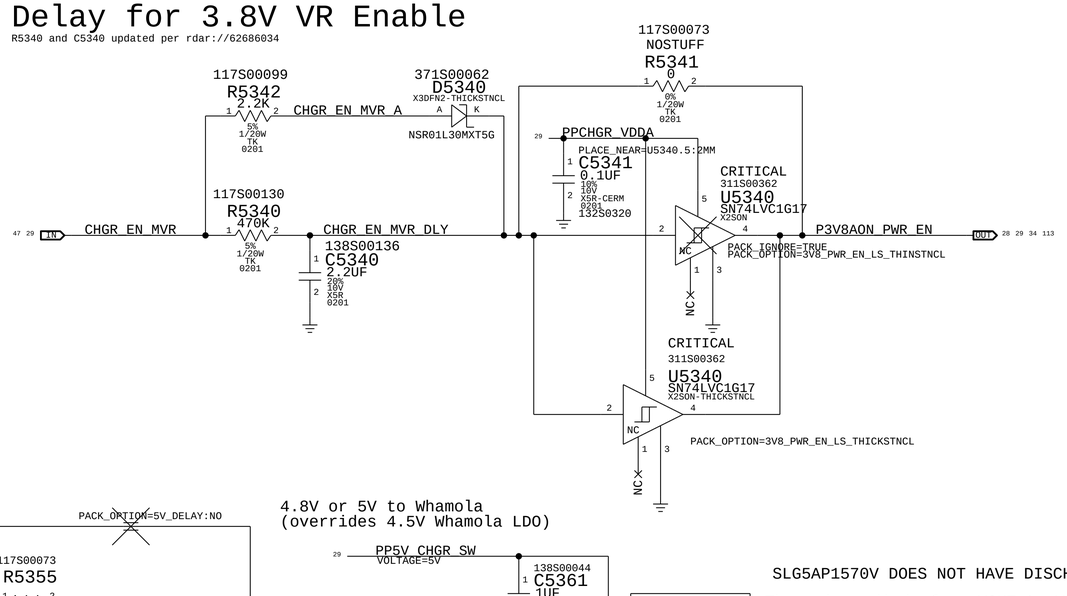
Pull up to MPMU LDO9, or rely on MPMU internal pull up.
OK, TO COMPLETELY REMOVE PULL UP , BUT CONSULT PMU ARCHITECTURE AND CHECK OTP BEFORE THAT.
DELETE PULL UP TO LDO9 PER RDAR://89302815

EE TO ADD ALIAS FOR CHGR_AUX_OK AND CHGR_AUX_OK_1V8.

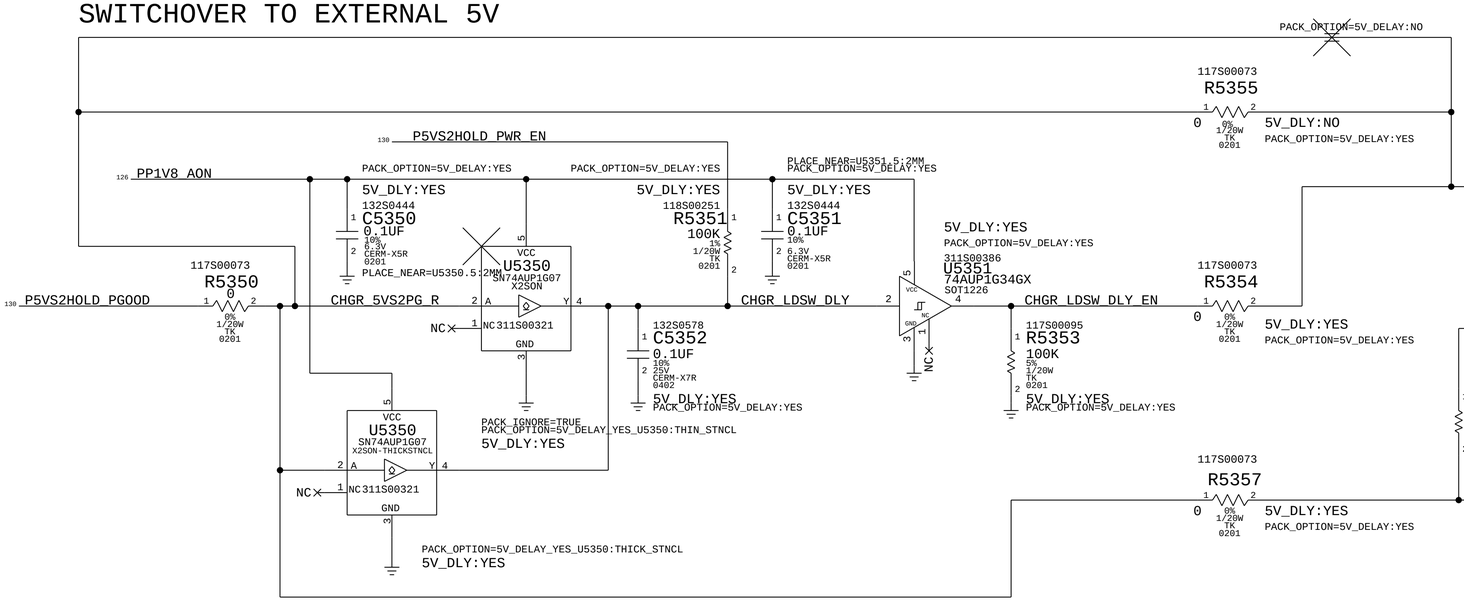
Probe points - bottom

Delay for 3.8V VR Enable

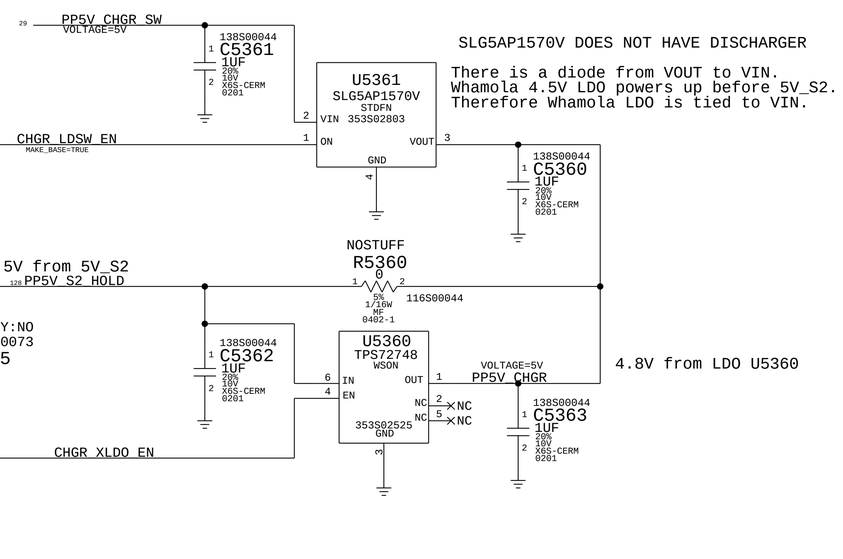
R5340 and C5340 updated per rdar://62686034



SWITCHOVER TO EXTERNAL 5V



4.8V or 5V to Whamola
(overrides 4.5V Whamola LDO)



Load switch enable rising edge is delayed.
Load switch enable falling edge is not delayed.

LDO is enabled before the load switch is enabled.
LDO disabled to prevent 5V_S2 discharge by Q5360.

BOM_COST_GROUP=BATTERY

PAGE TITLE
BATTERY CHARGER SUPPORT

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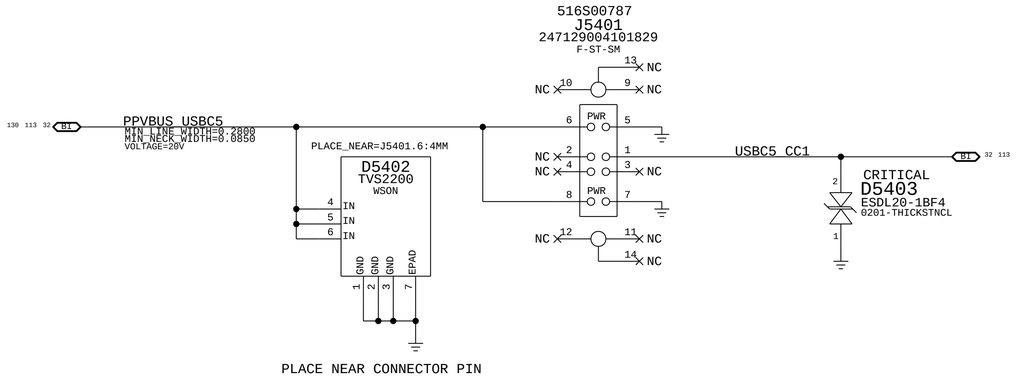
MLB:516S00787, FLEX:516S00788



BOM_COST_GROUP=MAGSAFE

PAGE TITLE: EXT PWR: CONNECTOR

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UPC5

MAX 100 UF TOTAL ON RAIL

PPHV_INT5_AONSW

PD_ACE5_VCONN

R5502 1K 5% 1/20W TK 0201-1 117S00077

PPVBUS_USBC5

PLACE_NEAR=U5500.G6:5MM PLACE_NEAR=U5500.H5:5MM PLACE_NEAR=U5500.J6:5MM PLACE_NEAR=U5500.K5:5MM PLACE_NEAR=U5500.L6:5MM PLACE_NEAR=U5500.M5:5MM PLACE_NEAR=U5500.H5:6MM

C5521 2200PF 10% 25V CER-X7R 0201 132S00057
C5522 2200PF 10% 25V CER-X7R 0201 132S00057
C5523 3300PF 10% 25V CER-X7R 0201 132S00343
C5524 3300PF 10% 25V CER-X7R 0201 132S00343
C5525 0.01UF 10% 25V X7R 0201 132S00070
C5526 0.01UF 10% 25V X7R 0201 132S00070
D5501 DSN2 NSR20F40NX_G 371S00085
C5501 1UF 10% 35V X5R 0402

PP_5V0 PP_CABLE PP_HV VBUS

CRITICAL
353S02158
U5500
CD3217B12BCE
FCBGA
OMIT_TABLE

DIGITAL CORE I/O & CONTROL

POWER

TYPE-C

PORT_MUX

GND

PD_UPC5_HRESET B13 HRESET
PD_UPC5_MRESET A14 MRESET
NC_UPC5_RESET_L B17 RESET*
TST_UPC5_SER_DBG A2 GPIO0
B1 GPIO0
UPC5_GPIO1 D1 GPIO1
UPC5_GPIO2 F1 GPIO2
UPC5_GPIO3 C2 GPIO3
UPC5_GPIO4 E2 GPIO4
UPC5_GPIO5 B3 GPIO5
UPC5_CHGR_AUX_DET_SHORT C4 GPIO6
UPC5_GPIO7 D3 GPIO7
UPC5_GPIO8 E4 GPIO8
UPC5_GPIO9 F3 GPIO9
UPC5_GPIO10 F7 GPIO10
A18 BUSPOWER
UPC5_I2C_ADDR M19 I2C_ADDR IPU-BOOT
UPC5_R_OSC M21 R_OSC
I2C_UPC5_SDA A16 I2CM_SDA_CNFG
I2C_UPC5_SCL B15 I2CM_SCL_CNFG
I2C_UPC_SDA B5 I2C_SDA1
I2C_UPC_SCL A4 I2C_SCL1
UPC_I2C_INT_L D7 I2C_IRQ1*
I2C_SMC_UPC_SDA B7 I2C_SDA2
I2C_SMC_UPC_SCL A6 I2C_SCL2
UPC_SMC_I2C_INT_L C8 I2C_IRQ2*
SPI_UPC5_R_CLK B9 SPI_CLK
SPI_UPC5_R_MOSI B11 SPI_MOSI
SPI_UPC5_R_MISO A10 SPI_MISO
SPI_UPC5_R_CS_L A8 SPI_SSZ
SWD_UPC_SWDIO2 E20 SWD_DATA IPU
SWD_UPC_SWCLK1 E16 SWD_CLK IPU
B19 UART_RX
UART_UPC5 A20 UART_TX
PD_UPC5_USB_RP H19 USB_RP1_P
H21 USB_RP1_N
G20 USB_RP2_P
G22 USB_RP2_N
F19 USB_RP3_P
F21 USB_RP3_N
J12 AUX_P
PD_UPC5_PORT_MUX H11 AUX_N
PD_UPC5_HPD C12 HPD
PD_UPC5_DBG_R G12 DEBUG0
F11 DEBUG1
E8 DEBUG2
E12 DEBUG3
G16 DEBUG4
F15 DEBUG5
D15 DEBUG6
D19 DEBUG7

VIN_3V3 C20 PP3V3_S2_LDO
VDDIO A12 PP1V25_S2
VDDIO_CFG D11
C22 PP3V3_UPC5_LDO
LDO_3V3 D21
VIN_LV L20 UPC5_LV
VOUT_LV L18
VRET C16
SS L22 UPC5_SS
LDO_CORE E22 PP1V5_UPC5_LDO_CORE
VBUS_OPT D5 PPVBUS_USBC5
PP_HV_OPT F5 PPHV_INT5_AONSW
C_CC1 M15 USBC5_CC1
N16
C_CC2 M17 USBC5_CC2
N18
RPD_G1 L14
RPD_G2 L16
C_USB_TP K19 PD_UPC5_USB2
C_USB_TN K21
C_USB_BP J20
C_USB_BN J22
C_SBU1 J16
C_SBU2 H15

R5511 0 0% 1/20W TK 0201
R5506 100K 5% 1/20W TK 0201
R5534 100K 5% 1/20W TK 0201
R5531 100K 5% 1/20W TK 0201
R5573 100K 5% 1/20W TK 0201
R5572 100K 5% 1/20W TK 0201
R5574 100K 5% 1/20W TK 0201
R5575 100K 5% 1/20W TK 0201
CRITICAL R5503 15K 0.1% 1/20W TK 0201 103S00582
R5505 1M 5% 1/20W TK 0201 117S00096
R5577 100K 5% 1/20W TK 0201 117S00095
R5578 100K 5% 1/20W TK 0201 117S00095
R5570 100K 5% 1/20W TK 0201 117S00095
R5576 100K 5% 1/20W TK 0201 117S00095

R5501 1K 5% 1/20W TK 0201-1 117S00077
C5508 10UF 20% 6.3V CERM 0402 138S0801
C5502 1.0UF 20% 6.3V X5R 0201-1
C5500 10UF 20% 6.3V CERM 0402 138S0801
C5509 0.68UF 5% 6.3V X6S 0402
C5505 10UF 20% 6.3V CERM 0402 138S0801
R5579 100K 5% 1/20W TK 0201 117S00095
NOSTUFF C5514 220PF 5% 50V C0G 0201-1 131S00464
C5513 220PF 5% 50V C0G 0201-1 131S00464

GND
A22 H9 N20 R21 K15 W22

SPI ROM

SPI_UPC5_R_CLK → R5568 15 5% 1/20W TK 0201 → SPI_UPC5_CLK
SPI_UPC5_R_CS_L → R5569 15 5% 1/20W TK 0201 → SPI_UPC5_CS_L

R5561 3.3K 5% 1/20W TK 0201
R5560 3.3K 5% 1/20W TK 0201
R5563 3.3K 5% 1/20W TK 0201
NOSTUFF R5564 3.3K 5% 1/20W TK 0201

U5560 8MBIT-3.0V W25Q80DVUXIE USON CRITICAL OMIT_TABLE
VCC CLK CS* WP*(IO2) HOLD*(IO3) DI(IO0) DO(IO1) GND EPAD

ROM_UPC5_WP_L
ROM_UPC5_HOLD_L

C5560 1UF 10% 6.3V CERM 402
R5562 3.3K 5% 1/20W TK 0201

PP3V3_UPC5_LDO

SPI_UPC5_MOSI
SPI_UPC5_MISO

R5565 15 5% 1/20W TK 0201 → SPI_UPC5_R_MOSI
R5566 15 5% 1/20W TK 0201 → SPI_UPC5_R_MISO
NOSTUFF R5567 47K 5% 1/20W TK 0201 117S00129

AARDVARKANOID CONN

APN 516S00115
USBC_DBG
J5502
505070-1222
PACK_TYPE=M-ST-SM

PP1V25_S2	1	2	SPI_UPC5_CS_L
SWD_UPC_SWDIO2	3	4	SPI_UPC5_CLK
SWD_UPC_SWCLK1	5	6	SPI_UPC5_MOSI
SPI_UPC5_MISO	7	8	TST_UPC5_SER_DBG
I2C_UPC01_3V3_SDA	9	10	NC_MAGSAFE_ACE_DEB_CON_10
I2C_UPC01_3V3_SCL	11	12	NC
	15	16	

PACK_OPTION=MAGSAFE_ACE_UPC_DBG:SMALL

BOM_COST_GROUP=MAGSAFE

PAGE TITLE: EXT PWR: PORT CONTROLLER

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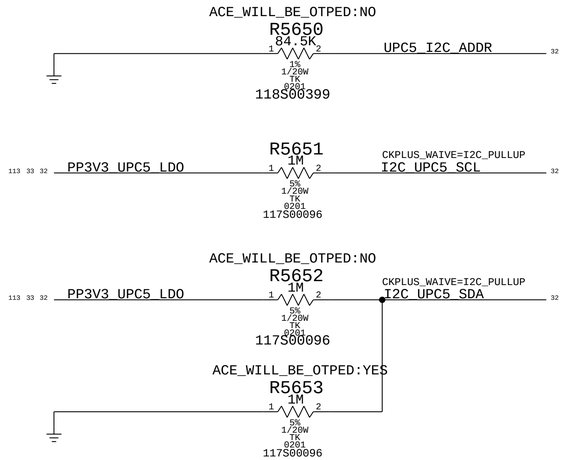
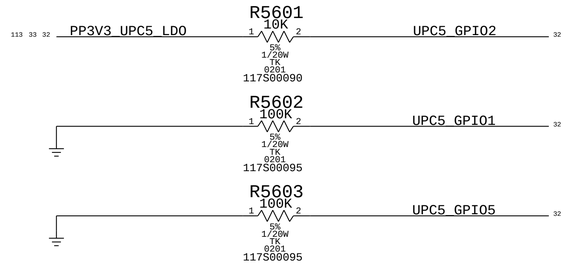
UPC5 I2C ADDRESS

IF FACTORY IS UPDATING OTP, THEN UPC5 STRAPS SHOULD BE:
I2C_ADDR: NOSTUFF PULL DOWN
I2CM_SCL_CNFG: 1M PULL UP
I2CM_SDA_CNFG: 1M PULL DOWN
IF FACTORY IS NOT UPDATING OTP (SUCH AS P0), THEN UPC5 STRAPS SHOULD BE:
I2C_ADDR: 84.5K PULL DOWN
I2CM_SCL_CNFG: 1M PULL UP
I2CM_SDA_CNFG: 1M PULL UP



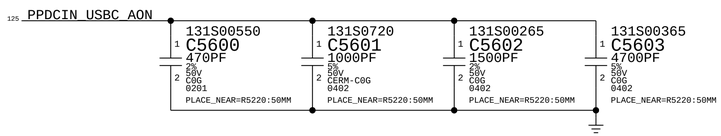
ADDITIONAL GPIO PULLS



POWER / FUSE FOR UPC

PPDCIN CAPS

TO REDUCE SPIKE ON PPDCIN AND REMOVE ACE LEAKAGE PER RDAR://88633531



BOM_COST_GROUP=MAGSAFE

PAGE TITLE
EXT PWR: CONTROLLER SUPPORT

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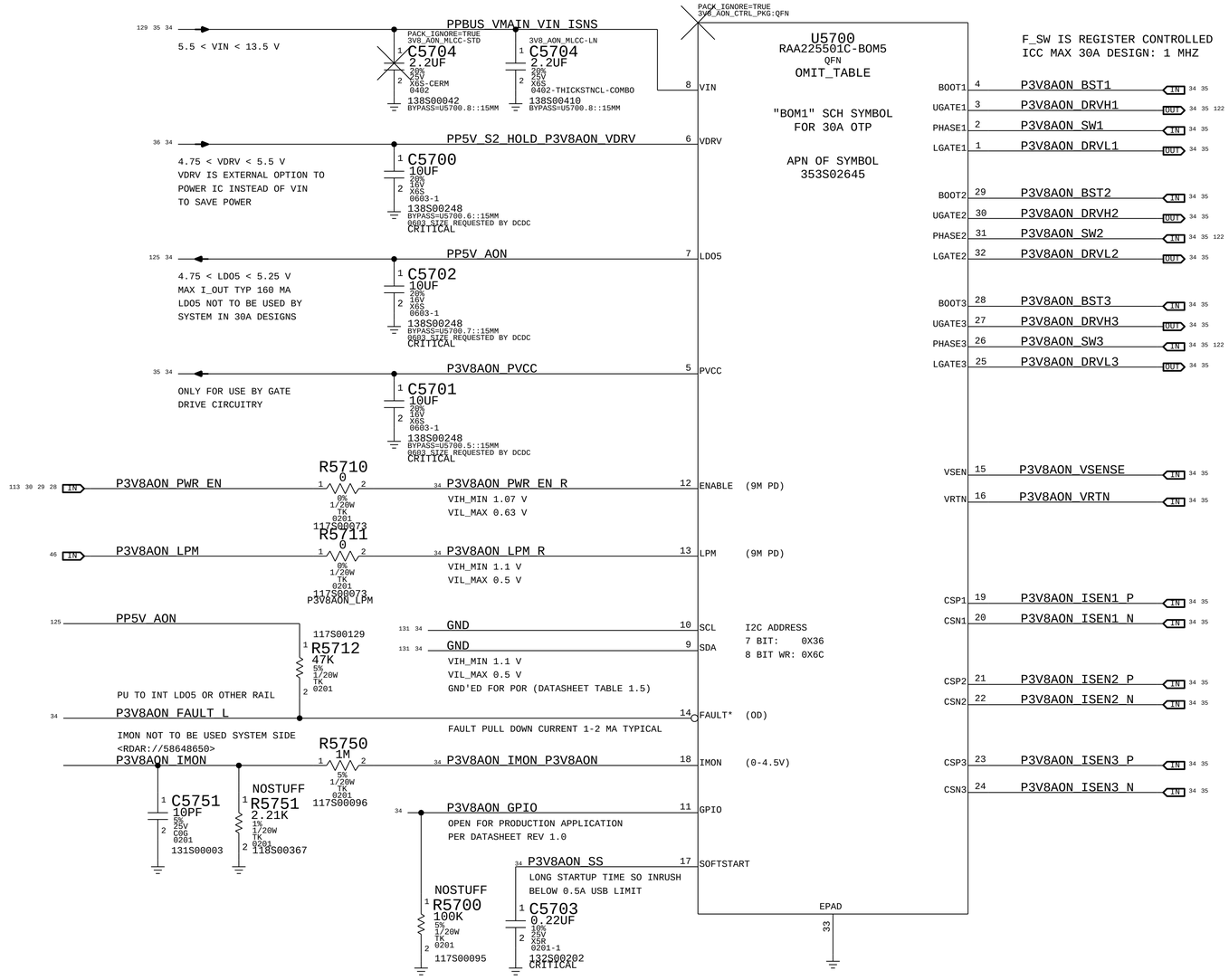
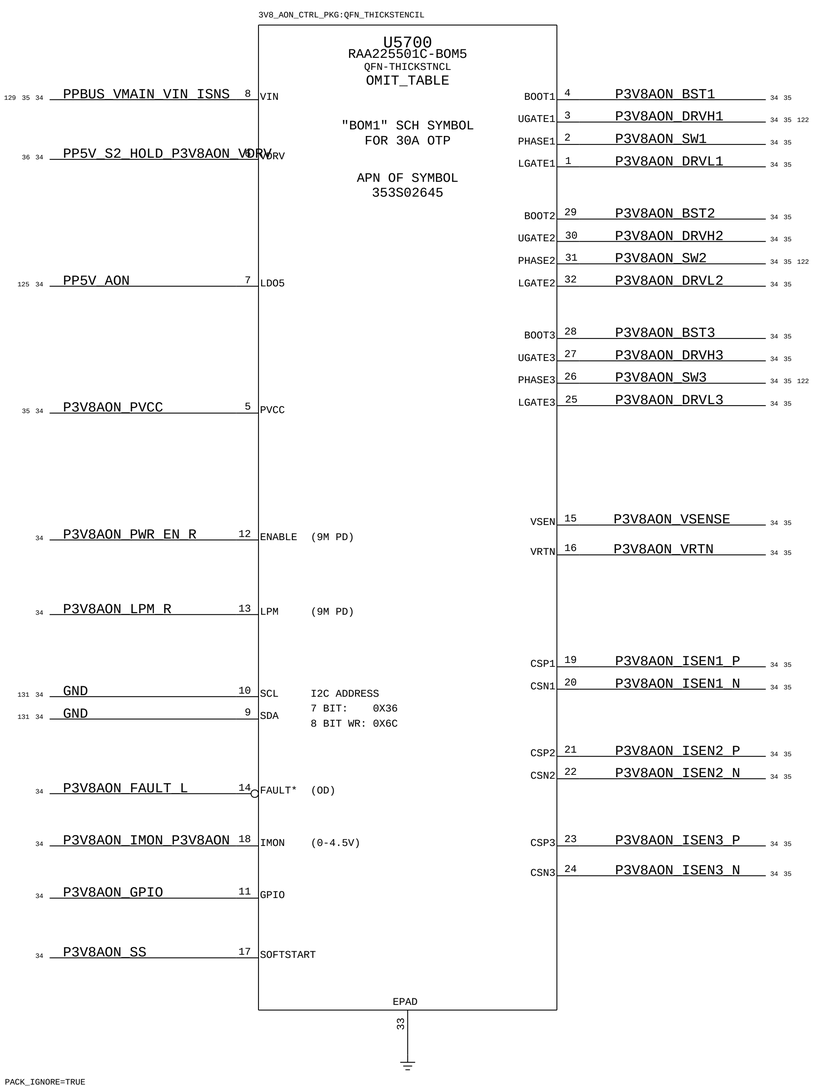
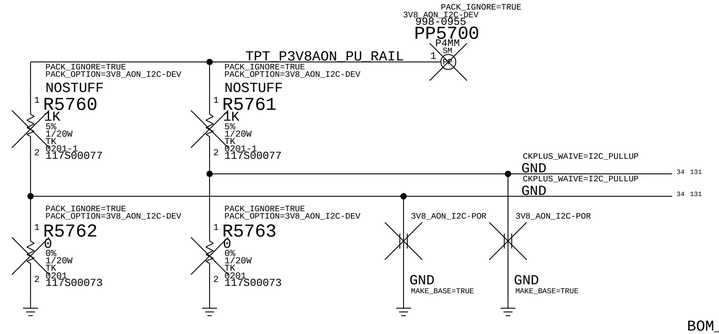
3V8 AON CONTROLLER
30A ICC MAX







30A OTP CHANGES DOCUMENTED IN <RDAR://61519509>

BOM5 IS A CONTINUATION OF BOM1 SINCE BOM1 IS FROZEN FOR TGA PROGRAMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
353S02326	1	IC,RAA225501,3-PH VOLT REG,TQFN32	U5700	CRITICAL	P3V8AON_IC:A0	
353S02472	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B0,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B0	
353S02544	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B1,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B1	
353S02560	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B2,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B2	
353S02576	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B3,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B3	
353S02592	1	IC,RAA225501B,ICE,BOM1,A2,OTP-R0B0,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_R0B0	<- 30A BOM1 OTP TGA PROGRAMS ARE GOING TO RAMP WITH
353S02645	1	IC,RAA225501C,ICE,BOM5,A2,OTP-R170,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_R170	<- NEW BOM5 OTP FOR FUTURE PROGRAMS

BOM_COST_GROUP=SOC POWER

PAGE TITLE: POWER: 3V8 AON (1/2)

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ICCMAX = 30 A

BOM_COST_GROUP=SOC POWER

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A PP3V8_AON Current Sense

Based on: rdar://problem/69466996

P3V8AON_ISNS3_P — R5924 5K 1/20W 0.1% TK 0201 — 103S00604 — NO_XNET_CONNECTION=1 — BOMOPTION=P3V8AON_ISNS
P3V8AON_ISNS2_P — R5922 5K 1/20W 0.1% TK 0201 — 103S00604 — NO_XNET_CONNECTION=1 — BOMOPTION=P3V8AON_ISNS
P3V8AON_ISNS1_P — R5920 20K 1/20W 0.1% TK 0201 — 103S00603 — NO_XNET_CONNECTION=1 — BOMOPTION=P3V8AON_ISNS
P3V8AON_ISNS1_N — R5921 20K 1/20W 0.1% TK 0201 — 103S00603 — NO_XNET_CONNECTION=1 — BOMOPTION=P3V8AON_ISNS
P3V8AON_ISNS2_N — R5923 5K 1/20W 0.1% TK 0201 — 103S00604 — NO_XNET_CONNECTION=1 — BOMOPTION=P3V8AON_ISNS
P3V8AON_ISNS3_N — R5925 5K 1/20W 0.1% TK 0201 — 103S00604 — NO_XNET_CONNECTION=1 — BOMOPTION=P3V8AON_ISNS

P3V8AON_ISNS_R_P — R5926 0 0% 1/20W TK 0201 — 117S00073 — BOMOPTION=P3V8AON_ISNS — P3V8AON_ISNS_P
P3V8AON_ISNS_R_N — R5927 0 0% 1/20W TK 0201 — 117S00073 — PLACE_NEAR=U5910.1:5MM — P3V8AON_ISNS_N — BOMOPTION=P3V8AON_ISNS — PLACE_NEAR=U5910.2:5MM

PP3V8_AON
BOMOPTION=P3V8AON_ISNS
BYPASS=U5910.A2::5MM — C5910 1UF 20% 10V X6S-CERM 0201 — 138S00044 — BOMOPTION=P3V8AON_ISNS
U5910 MAX9619 SC70 — 353S03250 — BOMOPTION=P3V8AON_ISNS
P3V8AON_ISUM_9P5X — R5917 0 0% 1/20W TK 0201 — 117S00073 — P3V8AON_ISUM_9P5X_R
R5910 100K 5% 1/20W TK 0201 — 117S00095 — BOMOPTION=P3V8AON_ISNS
R5914 200K 0.1% 1/20W TK 0201 — 103S00560
R5911 200K 0.1% 1/20W TK 0201 — 103S00560 — NO_XNET_CONNECTION=1 — BOMOPTION=P3V8AON_ISNS

BOMOPTION=P3V8AON_ISNS
BYPASS=U5911.A2::5MM — C5911 1UF 20% 10V X6S-CERM 0201 — 138S00044 — NOSTUFF
117S00073 — R5918 0 0% 1/20W TK 0201
NOSTUFF — U5911 MAX9619 SC70 — 353S03250
P3V8AON_ISUM_FB
R5913 324K 0.1% 1/20W TK 0201 — NOSTUFF — NO_XNET_CONNECTION=1 — 103S00607
R5912 38.3K 0.1% TK 1/20W 0201 — NOSTUFF — 103S00728

P3V8AON_ISUM_IOUT
R5915 100K 1% 1/20W TK 0201 — 118S00251 — PLACE_NEAR=U8100.E12:18MM — BOMOPTION=P3V8AON_ISNS
Rm = 0.02968 V/A
Fp = 74 Hz
P3V8AON_IMEAS (OUT)
R5916 261K 1% 1/20W TK 0201 — 118S00709
C5915 0.022UF 10% 6.3V X5R-CERM 0201 — 132S0330 — BOMOPTION=P3V8AON_ISNS
GND — BOMOPTION=P3V8AON_ISNS

P5VS2HOLD_PWR_EN (IN)

PP3V8_AON
NOSTUFF — U5912 MAX40100ANT+ BGA — 353S02125
NOSTUFF — U5913 MAX40100ANT+ BGA — 353S02125

PP3V8_AON
U5930 TPS7A0512 X2SON — 353S03149 — VOLTAGE=1.2V — BOMOPTION=P3V8AON_ISNS
BYPASS=U5930.4::5MM — C5930 1UF 20% 10V X6S-CERM 0201 — 138S00044 — BOMOPTION=P3V8AON_ISNS
BYPASS=U5930.1::5MM — C5931 1UF 20% 10V X6S-CERM 0201 — 138S00044 — BOMOPTION=P3V8AON_ISNS
PP1V2_VREF_P3V8AON_ILIMIT
117S00073 — R5932 0 0% 1/20W TK 0201 — NOSTUFF
BOMOPTION=P3V8AON_ISNS
BYPASS=U5940.2::5MM — C5940 1UF 20% 10V X6S-CERM 0201 — 138S00044

P3V8AON_ILIMIT_DIV_PULL_PWM (IN)
U5931 SN74AUP1G04 X2SON — 311S00323 — BOMOPTION=P3V8AON_ISNS
R5930 100K 5% 1/20W TK 0201 — 117S00095 — BOMOPTION=P3V8AON_ISNS
P3V8AON_ILIMIT_THRESH_RR
R5931 1K 1% 1/20W TK 0201 — 118S00282 — BOMOPTION=P3V8AON_ISNS
C5932 1UF 20% 10V X6S-CERM 0201 — 138S00044 — BOMOPTION=P3V8AON_ISNS
f = 240 kHz
V_ripple = Vdd/(4*f*R*C) = 1.25mV
P3V8AON_ILIMIT_THRESH
P3V8AON_ISUM_IOUT — R5933 0 0% 1/20W TK 0201 — 117S00073 — BOMOPTION=P3V8AON_ISNS — P3V8AON_ISUM_IOUT_R
C5933 1UF 20% 10V X6S-CERM 0201 — 138S00044 — NOSTUFF
BOMOPTION=P3V8AON_ISNS
353S02902
U5940 TLV7021 X2SON — OD Output
MPMU_VDDMAIN_UVWARN_L (OUT)

B PP5V_S2 to PP3V8_AON VDRV Connection

PP5V_S2_HOLD — R5900 0 0% 1/16W TK 0402 — 116S00022 — MAKE_BASE=TRUE — PP5V_S2_HOLD_P3V8AON_VDRV = PP5V_S2_HOLD_P3V8AON_VDRV
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: POWER: 3V8 AON SUPPORT

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DRAWING NUMBER: 051-07754 — SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 59 OF 999
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PP3V8_AON_SPMU_ISNS_VIN

CRITICAL 138S00073 C77F0 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C77F1 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C77F2 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C77F3 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C77F4 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C77F5 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C77F6 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C77F7 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00377 C77G0 2.2UF 20% 6.3V X6S 0201
CRITICAL 138S00044 C77G1 1UF 20% 10V X6S-CERM 0201
CRITICAL 138S00377 C77G2 2.2UF 20% 6.3V X6S 0201
CRITICAL 138S00044 C77G3 1UF 20% 10V X6S-CERM 0201
CRITICAL 138S00377 C77G4 2.2UF 20% 6.3V X6S 0201
CRITICAL 138S00044 C77G5 1UF 20% 10V X6S-CERM 0201
CRITICAL 138S00377 C77G6 2.2UF 20% 6.3V X6S 0201
CRITICAL 138S00044 C77G7 1UF 20% 10V X6S-CERM 0201
CRITICAL 138S00377 C77G8 2.2UF 20% 6.3V X6S 0201
CRITICAL 138S00044 C77G9 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C77H0 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C77H1 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C77H2 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C77H3 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C77H4 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C77H5 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C77H6 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C77H7 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C77H8 2.2UF 20% 6.3V X6S 0201
PACK_IGNORE=TRUE PMU_VDDMAIN_EXTRA_CAPS
138S00044 CRITICAL C77H9 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C77J0 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C77J1 1UF 20% 10V X6S-CERM 0201
PACK_IGNORE=TRUE PMU_VDDMAIN_EXTRA_CAPS
PACK_IGNORE=TRUE PMU_VDDMAIN_EXTRA_CAPS
PACK_IGNORE=TRUE PMU_VDDMAIN_EXTRA_CAPS

OMIT_TABLE 998-23585

U7700 VALE CSP SYM 1 OF 4

VOLTAGE INPUTS
A7 VDD_BUCK10_8
B7 VDD_BUCK10_8
A11 VDD_BUCK10_8
B11 VDD_BUCK10_8
G13 VDD_BUCK14_5
G14 VDD_BUCK14_5
L12 VDD_BUCK14_5
L13 VDD_BUCK14_5
L14 VDD_BUCK14_5
L1 VDD_MAIN_BUCK6
M2 VDD_BUCK6
N2 VDD_BUCK6
P2 VDD_BUCK6
N6 VDD_BUCK12
P6 VDD_BUCK12
H5 VDD_MAIN
C11 VDD_MAIN_NORTH
N10 VDD_MAIN_SOUTH

SENSE
40 PPVDD_SPMU_VDD_MAIN_SNS → E4 VDD_MAIN_SNS
40 PPVDD_SPMU_VDD_BOOST_SNS → F6 VDD_BOOST_SNS

BUCK OUTPUTS
127 PP1V5_LDOINT_SPMU
132S00030 C7720 0.1UF 10% 16V X6S-CERM 0201
132S00030 C7721 0.1UF 10% 16V X6S-CERM 0201
C7 VDD_ANA
D4 VDD_ANA
D10 VDD_ANA
G5 VDD_ANA
G12 VDD_ANA
K3 VDD_ANA
M6 VDD_ANA
N12 VDD_ANA
127 PP1V5_LDOINT_SPMU
132S00030 C7722 0.1UF 10% 16V X6S-CERM 0201
132S00030 C7723 0.1UF 10% 16V X6S-CERM 0201
D11 VDD_DIG
E8 VDD_DIG
K5 VDD_DIG
L11 VDD_DIG
C14 BSTLQ_LX
D14 BSTLQ_VOUT
40 37 SPMU_BSTLQ_LX
37 PP5V_SPMU_BSTLQ_XW
127 PP5V_SPMU_BSTLQ
D5 VDD_HI_INT1
E5 VDD_HI_INT2
L4 VDD_HI_INT3
N11 VDD_HI_INT4
E11 VDD_HI_INT5
126 PP1V25_S2 → J10 VDDIO_1V2
125 PP1V8_S2 → H10 VDDIO_1V8
127 PP1V2_AON_SPMU → G10 VDDIO_1V2_1V8
PPVREF_SPMU VOLTAGE=1.0 → G4 VREF
138S00041 CRITICAL C7711 2.2UF 10% 10V X6S-CERM 0402
PP1V5_SPMU_VREFADC VOLTAGE=1.5 → H4 VREF_ADC
132S0406 CRITICAL C7710 0.22UF 20% 6.3V X6S-CERM 0201
40 39 GND_VREF_RTN_SPMU VOLTAGE=0V
40 GND_VREF_RTN_SPMU VOLTAGE=0V

152S00874 L7700 0.47UH-20%-1.7A-0.175OHM PIJT1005FE-SM-COMBO
40 37 SPMU_BSTLQ_LX SWITCH_NODE=TRUE DIDT=TRUE
PP3V8_AON_SPMU_ISNS_VIN 37 40 129
XW7700 SHORT-12L-0.25MM-SM
37 PP5V_SPMU_BSTLQ_XW VOLTAGE=5 MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000
PP5V_SPMU_BSTLQ 127
138S00078 C7700 22UF 20% 10V X5R 0402
138S00078 C7701 22UF 20% 10V X5R 0402
132S00030 C7702 0.1UF 10% 16V X6S-CERM 0201
132S00030 C7770 0.1UF 10% 16V X6S-CERM 0201
132S00030 C7771 0.1UF 10% 16V X6S-CERM 0201
132S00030 C7772 0.1UF 10% 16V X6S-CERM 0201
132S00030 C7773 0.1UF 10% 16V X6S-CERM 0201

BUCK5_LX0 H14
BUCK5_LX1 K12
BUCK5_LX1 K13
BUCK5_LX1 K14
BUCK5_FB H11
BUCK5_VSS_FB H12
BUCK6_VOUT M1
BUCK6_VOUT N1
BUCK6_VOUT P1
BUCK6_LX M3
BUCK6_LX N3
BUCK6_LX P3
BUCK6_FB L3
BUCK6_VSS_FB K2
BUCK8_LX0 A12
BUCK8_LX1 A10
BUCK8_LX1 B10
BUCK8_LX2 A8
BUCK8_LX2 B8
BUCK8_FB D12
BUCK8_VSS_FB C12
BUCK10_LX A6
BUCK10_LX B6
BUCK10_FB D6
BUCK10_VSS_FB C6
BUCK12_LX N5
BUCK12_LX P5
BUCK12_FB L5
BUCK12_VSS_FB M5
BUCK14_LX F13
BUCK14_LX F14
BUCK14_FB F11
BUCK14_VSS_FB F12

CRITICAL L7750 1.0UH-20%-4A-0.034OHM PIKD20161B-SM 152S01283
BUCK5_LX0 SWITCH_NODE=TRUE DIDT=TRUE
PP0V779_S1_SRAM
CRITICAL L7751 0.22UH-20%-6.7A-0.023OHM PINA201217-SM 152S00204
BUCK5_LX1 SWITCH_NODE=TRUE DIDT=TRUE
R7750 0 0% 1/20W TK 0201
998-14727 XW7750 SHORT-16L-0.1MM-SM
BUCK5_FB BUCK5_FB_R NO_XNET_CONNECTION=1
BOMOPTION=PMU_FB:FF

CRITICAL L7760 0.47UH-20%-6.9A-0.022OHM MEMK2520-SM 152S01325
BUCK6_LX SWITCH_NODE=TRUE DIDT=TRUE
R7760 0 0% 1/20W TK 0201
998-0313 XW7760 SHORT-16L-0.1MM-SM
40 BUCK6_FB BUCK6_FB_R NO_XNET_CONNECTION=1
BOMOPTION=BUCK6_BULK_REG

CRITICAL L7780 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283
BUCK8_LX0 SWITCH_NODE=TRUE DIDT=TRUE
CRITICAL L7781 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM 152S01268
BUCK8_LX1 BUCK8_LX2 SWITCH_NODE=TRUE DIDT=TRUE
R7780 0 0% 1/20W TK 0201
998-0313 XW7780 SHORT-16L-0.1MM-SM
BUCK8_FB BUCK8_FB_R NO_XNET_CONNECTION=1
BOMOPTION=PMU_FB:FF

CRITICAL L77A0 0.47UH-20%-4A-0.024OHM PIKD20121B-SM 152S01263
BUCK10_LX SWITCH_NODE=TRUE DIDT=TRUE
R77A0 0 0% 1/20W TK 0201
998-0313 XW77A0 SHORT-16L-0.1MM-SM
BUCK10_FB BUCK10_FB_R NO_XNET_CONNECTION=1
BOMOPTION=PMU_FB:FF

CRITICAL L77C0 0.47UH-20%-4A-0.024OHM PIKD20121B-SM 152S01263
BUCK12_LX SWITCH_NODE=TRUE DIDT=TRUE
R77C0 0 0% 1/20W TK 0201
998-0313 XW77C0 SHORT-16L-0.1MM-SM
BUCK12_FB BUCK12_FB_R NO_XNET_CONNECTION=1
BOMOPTION=PMU_FB:FF

CRITICAL L77E0 0.47UH-20%-4A-0.024OHM PIKD20121B-SM 152S01263
BUCK14_LX SWITCH_NODE=TRUE DIDT=TRUE
R77E0 0 0% 1/20W TK 0201
998-0313 XW77E0 SHORT-16L-0.1MM-SM
BUCK14_FB BUCK14_FB_R NO_XNET_CONNECTION=1
BOMOPTION=PMU_FB:FF

PP0V779_S1_SRAM
CRITICAL 138S1058 C7750 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7751 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7752 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7753 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7754 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7755 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7756 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7757 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7758 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7759 15UF 20% 2V X6S 0402-2
CRITICAL 138S00039 C775A 2.2UF 20% 4V X6S-CERM 0201
CRITICAL 138S00039 C775B 2.2UF 20% 4V X6S-CERM 0201
PACK_OPTION=BUCK5_LOCAL_CAPS
PACK_OPTION=BUCK5_LOCAL_CAPS

PP2V58_AWAKE_NAND_VCC
CRITICAL 138S00073 C7760 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7761 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7762 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7763 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7764 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7765 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7768 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7769 10UF 20% 6.3V CER-X6S 0402-COMBO
BOMOPTION=BUCK6_BULK_REG
CRITICAL 138S00073 C776A 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C776B 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7766 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C7767 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C776C 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C776D 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C776E 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C776F 10UF 20% 6.3V CER-X6S 0402-COMBO
BOMOPTION=BUCK6_BULK_REG

PPVDD_S1_DISP
CRITICAL 138S1058 C7780 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7781 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7782 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7783 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7784 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7785 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7786 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7787 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7788 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C7789 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C778A 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C778B 15UF 20% 2V X6S 0402-2
CRITICAL 138S00039 C778C 2.2UF 20% 4V X6S-CERM 0201
CRITICAL 138S00039 C778D 2.2UF 20% 4V X6S-CERM 0201
NOSTUFF
NOSTUFF
PACK_OPTION=BUCK8_LOCAL_CAPS
PACK_OPTION=BUCK8_LOCAL_CAPS

PPVDD_S1_VDDQL
CRITICAL 138S1058 C77A0 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77A1 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77A2 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77A3 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77A4 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77A5 15UF 20% 2V X6S 0402-2
CRITICAL 138S00039 C77A6 2.2UF 20% 4V X6S-CERM 0201
CRITICAL 138S00039 C77A7 2.2UF 20% 4V X6S-CERM 0201
BOMOPTION=PMU_BULK_VDDQL
BOMOPTION=PMU_BULK_VDDQL

PP0V88_S1
CRITICAL 138S1058 C77C0 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77C1 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77C2 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77C3 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77C4 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77C5 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77C6 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77C7 15UF 20% 2V X6S 0402-2
NOSTUFF
NOSTUFF

PP1V12_S2SW_AMPH
CRITICAL 138S1058 C77E0 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77E1 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77E2 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77E3 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77E4 15UF 20% 2V X6S 0402-2
CRITICAL 138S1058 C77E5 15UF 20% 2V X6S 0402-2
CRITICAL 138S00039 C77E6 2.2UF 20% 4V X6S-CERM 0201
CRITICAL 138S00039 C77E7 2.2UF 20% 4V X6S-CERM 0201
PACK_OPTION=BUCK14_LOCAL_CAPS
PACK_OPTION=BUCK14_LOCAL_CAPS

BOM_COST_GROUP=SOC POWER

PAGE TITLE: SPMU: INPUT PWR, BULK, BSTLQ

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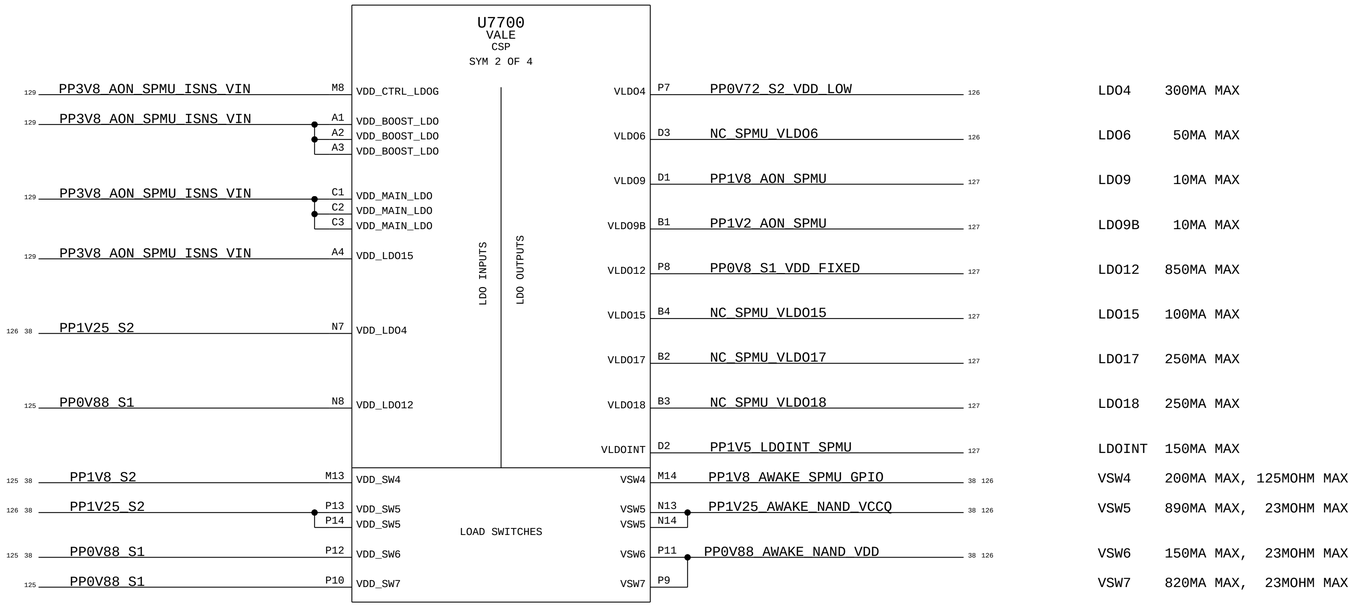
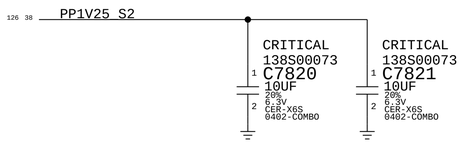
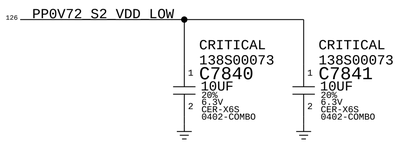
OMIT_TABLE
998-23585

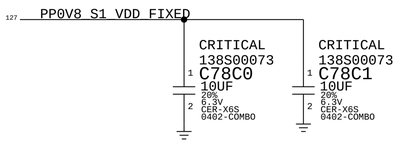


LDO4	300MA MAX	
LDO6	50MA MAX	
LDO9	10MA MAX	
LDO9B	10MA MAX	
LDO12	850MA MAX	
LDO15	100MA MAX	
LDO17	250MA MAX	
LDO18	250MA MAX	
LDOINT	150MA MAX	
VSW4	200MA MAX,	125MOHM MAX
VSW5	890MA MAX,	23MOHM MAX
VSW6	150MA MAX,	23MOHM MAX
VSW7	820MA MAX,	23MOHM MAX

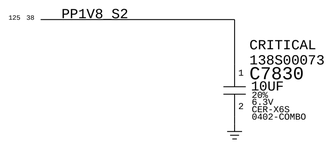
VDD_LDO4
DECOUPLNIG SHARED WITH J10 (VDDIO_1V2)

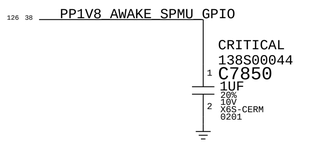


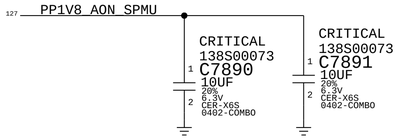
VLDO4


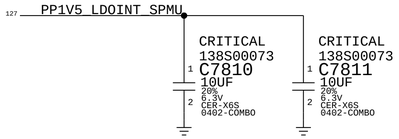
VLDO12


VDD_SW4
DECOUPLNIG SHARED WITH H10 (VDDIO_1V8)

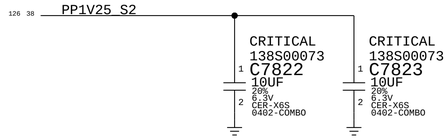


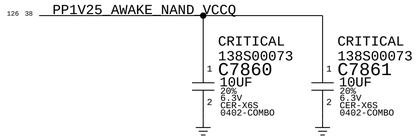
VSW4


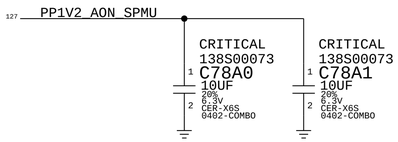
VLDO9


VLDOINT


VDD_SW5
DECOUPLNIG SHARED WITH J10 (VDDIO_1V2)

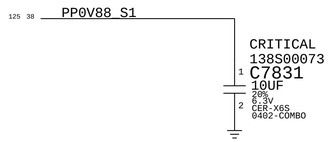


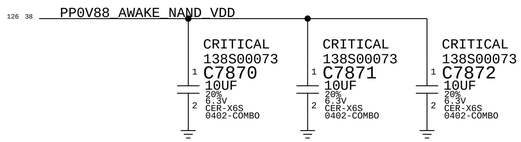
VSW5


VLDO9B


UN-UNUSED LDOS
LDO 6, 15, 17, 18

VDD_SW6/7
DECOUPLNIG SHARED VDD_LDO12



VSW6/7


BOM_COST_GROUP=SOC POWER

PAGE TITLE
SPMU: LDO, SW

Apple Inc.

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REVISION 6.0.0
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*** OK2INTEGRATE ***

OMIT_TABLE
998-23585

U7700
VALE
CSP
SYM 3 OF 4

63	IN	SPMU_THMSNS	H1	TDEV1	GPIO0	D8	NC_SPMU_GPIO_0
63	IN	AMBLR_THMSNS	J1	TDEV2	GPIO1	J7	NC_SPMU_GPIO_1
63	IN	NAND0_THMSNS	H2	TDEV3	GPIO2	K7	NC_SPMU_GPIO_2
63	IN	NAND1_THMSNS	G2	TDEV4	GPIO3	J8	NC_SPMU_GPIO_3
63	IN	AMBLL_THMSNS	J2	TDEV5	GPIO4	G9	NC_SPMU_GPIO_4
		SPMU_TCAL	G1	TCAL	GPIO5	D9	NC_SPMU_GPIO_5
40	IN	SPMU_ADC_IN	G3	ADC_IN	GPIO6	K8	NC_SPMU_GPIO_6
62	IN	MPMU_HS_ISENSE	E2	AMUX_A<0>	GPIO7	H7	NC_SPMU_GPIO_7
62	IN	SPMU_HS_ISENSE	F2	AMUX_A<1>	GPIO8	L10	NC_SPMU_GPIO_8
62	IN	P3V8AON_HS_ISENSE	F1	AMUX_A<2>	GPIO9	K9	NC_SPMU_GPIO_9
62	IN	WLBT_3V8_ISENSE	E1	AMUX_A<3>	GPIO10	H9	NC_SPMU_GPIO_10
40	BI	SPMU_AMUX_AY	H3	AMUX_AY	GPIO11	E10	NC_SPMU_GPIO_11
62	IN	P5VS2_HS_ISENSE	F3	AMUX_B<0>	GPIO12	K6	NC_SPMU_GPIO_12
62	IN	PORT5V_HS_ISENSE	F4	AMUX_B<1>	GPIO13	K10	NC_SPMU_GPIO_13
62	IN	TCON_3V8_ISENSE	F5	AMUX_B<2>	GPIO14	H6	NC_SPMU_GPIO_14
62	IN	LCDBKLT_HS_ISENSE	E3	AMUX_B<3>	GPIO15	E9	NC_SPMU_GPIO_15
40	BI	SPMU_AMUX_BY	J3	AMUX_BY	UVWARN*	G7	SPMU_VDDMAIN_UVWARN_L
14	IN	SPMI_NUB_SPMU_CLK	L9	SPMI_SCLK			
14	BI	SPMI_NUB_SPMU_DATA	L8	SPMI_SDATA	SCRASH*	F7	SPMU_SCRASH_L
45	IN	SGPIO_SCLK	L7	SGPIO_SCLK	SGPIO_READY_REQ	G8	PMU_SGPIO_READY_REQ
45	BI	SGPIO_SDATA	M7	SGPIO_SDATA			
40	IN	SPMU_RESET_IN	G6	RESET_IN			
40	IN	SPMU_FORCE_SYNC	F9	FORCE_SYNC			
130	BI	SWD_NUB_SWDIO_SPMU	F8	SWD_TMS			
40	IN	GND	H8	DFT_CTRL0			
130	IN	SWD_NUB_SWCLK_SPMU	J9	DFT_CTRL1			
40	IN	GND	J5	DFT_CTRL2			
48		GND	M10	VPP			

ADC | GPIO | THROTTLE | INTERFACE

63 40 GND_TCAL_SPMU
VOLTAGE=0V

103S00584
R7950
3.92K
0.1%
1/20W
TF
0201

131S0805
C7950
100PF
5%
25V
C0G
0201

OMIT_TABLE
998-23585

U7700
VALE
CSP
SYM 4 OF 4

J12	VSS_BUCK5		VSS	B12	
J13	VSS_BUCK5		VSS	C4	
J14	VSS_BUCK5		VSS	C5	
			VSS	C8	
A9	VSS_BUCK8		VSS	C9	
B9	VSS_BUCK8		VSS	C10	
A13	VSS_BUCK8		VSS	C13	
B13	VSS_BUCK8		VSS	D7	
			VSS	D13	
A5	VSS_BUCK10		VSS	E6	
B5	VSS_BUCK10		VSS	E7	
			VSS	E12	
N4	VSS_BUCK12_6		VSS	F10	
P4	VSS_BUCK12_6		VSS	G11	
			VSS	H13	
E13	VSS_BUCK14		VSS	J6	
E14	VSS_BUCK14		VSS	J11	
			VSS	K1	
A14	VSS_BSTLQ		VSS	K4	
B14	VSS_BSTLQ		VSS	K11	
			VSS	L2	
J4	VSS_REF		VSS	L6	
			VSS	M4	
			VSS	M9	
			VSS	M11	
			VSS	M12	
			VSS	N9	

40 37 GND_VREF_RTN_SPMU

998-14727
XW7910
SHORT-16L-0.1MM-SM
1 2

PLACEMENT NOTES

CONNECT VSS_REF THROUGH ALL GND LAYERS
PLACE XW AT VSS_REF PIN, ROUTE RTN SIGNAL BACK TO PASSIVES

BOM_COST_GROUP=SOC POWER

PAGE TITLE
SPMU: GPIO, VSS

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*** PROJECT SPECIFIC (USE AS TEMPLATE) ***

SPMU GPIO

NC_SPMU_GPIO_0 — NC_SPMU_GPIO_0 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_1 — NC_SPMU_GPIO_1 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_2 — NC_SPMU_GPIO_2 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_3 — NC_SPMU_GPIO_3 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_4 — NC_SPMU_GPIO_4 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_5 — NC_SPMU_GPIO_5 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_6 — NC_SPMU_GPIO_6 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_7 — NC_SPMU_GPIO_7 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_8 — NC_SPMU_GPIO_8 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_9 — NC_SPMU_GPIO_9 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_10 — NC_SPMU_GPIO_10 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_11 — NC_SPMU_GPIO_11 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_12 — NC_SPMU_GPIO_12 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_13 — NC_SPMU_GPIO_13 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_14 — NC_SPMU_GPIO_14 (MAKE_BASE=TRUE, NO_TEST=1)
NC_SPMU_GPIO_15 — NC_SPMU_GPIO_15 (MAKE_BASE=TRUE, NO_TEST=1)

GND
GND — MAKE_BASE=TRUE

PROBE POINTS

SPMU_AMUX_AY (BI) — PP8000 P4MM SM (NO_TEST=1)
SPMU_AMUX_BY (BI) — PP8001 P4MM SM (NO_TEST=1)
BUCK5_LX0 (IN) — PP8050 P4MM SM (NO_TEST=1)
BUCK5_LX1 (IN) — PP8051 P4MM SM (NO_TEST=1)
BUCK6_LX (IN) — PP8060 P4MM SM (NO_TEST=1)
BUCK8_LX0 (IN) — PP8080 P4MM SM (NO_TEST=1)
BUCK8_LX1 (IN) — PP8081 P4MM SM (NO_TEST=1)
BUCK8_LX2 (IN) — PP8082 P4MM SM (NO_TEST=1)
BUCK10_LX (IN) — PP80A0 P4MM SM (NO_TEST=1)
BUCK12_LX (IN) — PP80C0 P4MM SM (NO_TEST=1)
BUCK14_LX (IN) — PP80E0 P4MM SM (NO_TEST=1)
SPMU_BSTLQ_LX (IN) — PP80F0 P4MM SM (NO_TEST=1)

ALIAS AMUX NEGATIVE REFERENCE TO GND

GND — MAKE_BASE=TRUE

TCAL/TDEV NEGATIVE XW CONNECTION TO GND

XW8030 998-14727 SHORT-16L-0.1MM-SM
GND_TCAL_SPMU — XW8030 — GND

ALIAS VREF AND ADC GND

GND_VREF_RTN_SPMU — GND_VREF_RTN_SPMU (MAKE_BASE=TRUE)

SPMU_ADC_IN — R8010 117S00096 1M 5% 1/20W TK 0201
SPMU_RESET_IN — R8011 117S00095 100K 5% 1/20W TK 0201
SPMU_FORCE_SYNC — R8012 117S00095 100K 5% 1/20W TK 0201

PP1V25_AWAKE_IO — R8020 117S00090 10K 5% 1/20W TK 0201 — SPMU_VDDMAIN_UVWARN_L
NOSTUFF

VDD MAIN/BOOST SENSE

XW8020 998-14727 SHORT-16L-0.1MM-SM
PPVDD_SPMU_VDD_MAIN_SNS — XW8020 — PP3V8_AON_SPMU_ISNS_VIN (OUT)
PPVDD_SPMU_VDD_MAIN_SNS (MAKE_BASE=TRUE)
NO_XNET_CONNECTION=1

XW8021 998-14727 SHORT-16L-0.1MM-SM
PPVDD_SPMU_VDD_BOOST_SNS — XW8021 — PP3V8_AON_SPMU_ISNS_VIN (OUT)
PPVDD_SPMU_VDD_BOOST_SNS (MAKE_BASE=TRUE)
NO_XNET_CONNECTION=1

BUCK6 REMOTE BULK DECOUPLING OPTIONS (FOR X2211)

PP2V58_AWAKE_NAND_VCC

CRITICAL 138S00073 C8060 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8061 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8062 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8063 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8064 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8065 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8068 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8069 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C806A 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C806B 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8066 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C8067 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C806C 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C806D 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C806E 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL 138S00073 C806F 10UF 20% 6.3V CER-X6S 0402-COMBO

PACK_OPTION=BUCK6_RMT

ADD 2X 2.2UF AT REGULATOR

PP2V58_AWAKE_NAND_VCC
CRITICAL 138S00039 C806G 2.2UF 20% 4V X6S-CERM 0201
CRITICAL 138S00039 C806H 2.2UF 20% 4V X6S-CERM 0201
PACK_OPTION=BUCK6_RMT

ADD OPTION FOR REMOTE SENSING

BUCK6_FB — R8060 0 0% 1/20W TK 0201 — BUCK6_FB_RMT — XW8060 998-14727 SHORT-16L-0.1MM-SM NO_XNET_CONNECTION=1 — PP2V58_AWAKE_NAND_VCC
PACK_OPTION=BUCK6_RMT

BOM_COST_GROUP=SOC POWER

PAGE TITLE: SPMU: ALIASES, SUPPORT

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*** OK2INTEGRATE ***

PP3V8_AON_MPMU_ISNS_VIN

129 46 44 43

138S00073 CRITICAL C81A0 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81A1 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81A2 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81A3 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81A4 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81A5 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81A6 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81A7 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81A8 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81A9 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81AA 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81AB 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81AC 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81AD 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81AE 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81AF 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81AG 10UF 20% 6.3V X6S 0402-COMBO
138S00073 CRITICAL C81AH 10UF 20% 6.3V X6S 0402-COMBO
138S00377 CRITICAL C8140 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8141 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8142 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8143 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8144 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8145 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8146 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8147 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8148 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8149 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8150 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8151 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8152 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8153 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8154 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8155 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8156 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8157 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8158 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8159 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8160 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8161 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8162 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8163 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8164 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8165 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8166 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8167 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8168 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8169 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8170 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8171 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8172 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8173 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8174 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8175 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8176 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8177 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8178 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8179 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8180 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8181 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8182 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8183 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8184 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8185 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8186 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8187 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8188 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8189 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8190 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8191 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8192 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8193 1UF 20% 10V X6S-CERM 0201
138S00377 CRITICAL C8194 2.2UF 20% 6.3V X6S 0201
138S00044 CRITICAL C8195 1UF 20% 10V X6S-CERM 0201

PACK_IGNORE=TRUE PMU_VDDMAIN_EXTRA_CAPS

OMIT_TABLE
998-23524

U8100
STOWE_00
CSP
SYM 1 OF 5

VOLTAGE INPUTS

B1 VDD_BUCK_MP
B2 VDD_BUCK_MP
B3 VDD_BUCK_MP
B4 VDD_BUCK_MP
F1 VDD_BUCK_MP
F2 VDD_BUCK_MP
F3 VDD_BUCK_MP
F4 VDD_BUCK_MP
K1 VDD_BUCK_MP
K2 VDD_BUCK_MP
K3 VDD_BUCK_MP
K4 VDD_BUCK_MP
P1 VDD_BUCK_MP
P2 VDD_BUCK_MP
P20 VDD_BUCK_MP
P21 VDD_BUCK_MP
V20 VDD_BUCK_MP
V21 VDD_BUCK_MP
A7 VDD_BUCK_MP
B7 VDD_BUCK_MP
A11 VDD_BUCK_MP
B11 VDD_BUCK_MP
C11 VDD_BUCK_MP
A15 VDD_BUCK_MP
B15 VDD_BUCK_MP
U2 VDD_BUCK_MP
V2 VDD_BUCK_MP
W2 VDD_BUCK_MP
Y2 VDD_BUCK_MP
U6 VDD_BUCK_MP
V6 VDD_BUCK_MP
W6 VDD_BUCK_MP
Y6 VDD_BUCK_MP
U10 VDD_BUCK_MP
V10 VDD_BUCK_MP
W10 VDD_BUCK_MP
Y10 VDD_BUCK_MP
W14 VDD_BUCK_MP
Y14 VDD_BUCK_MP
W18 VDD_BUCK_MP
Y18 VDD_BUCK_MP
A19 VDD_BUCK13_3
B19 VDD_BUCK13_3
C19 VDD_BUCK13_3
J9 VDD_MAIN
C15 VDD_MAIN1
V16 VDD_MAIN2
M16 VDD_MAIN3

BUCK OUTPUTS

SENSE

46 PPVDD_MPMU_VDD_MAIN_SNS J8 VDD_MAIN_SNS
47 PBUS_DIV_SNS_R J6 VDD_BOOST_SNS

127 PP1V5_LDOINT_MPMU
132S00030 C8130 0.1UF 10% 10V X6S-CERM 0201
132S00030 C8131 0.1UF 10% 10V X6S-CERM 0201
C7 VDD_ANA
D14 VDD_ANA
D19 VDD_ANA
H5 VDD_ANA
J10 VDD_ANA
M18 VDD_ANA
P3 VDD_ANA
T8 VDD_ANA
V14 VDD_ANA
V19 VDD_ANA

127 PP1V5_LDOINT_MPMU
132S00030 C8132 0.1UF 10% 10V X6S-CERM 0201
132S00030 C8133 0.1UF 10% 10V X6S-CERM 0201
E18 VDD_DIG
G12 VDD_DIG
H6 VDD_DIG
L15 VDD_DIG
N6 VDD_DIG

PACK_IGNORE=TRUE PMU_VDDMAIN_EXTRA_CAPS

PACK_IGNORE=TRUE PMU_VDDMAIN_EXTRA_CAPS

BUCK0_LX0 R1
BUCK0_LX0 R2
BUCK0_LX1 U3
BUCK0_LX1 V3
BUCK0_LX1 W3
BUCK0_LX1 Y3
BUCK0_LX3 U5
BUCK0_LX3 V5
BUCK0_LX3 W5
BUCK0_LX3 Y5
BUCK0_LX2 U7
BUCK0_LX2 V7
BUCK0_LX2 W7
BUCK0_LX2 Y7
BUCK0_LX4 U9
BUCK0_LX4 V9
BUCK0_LX4 W9
BUCK0_LX4 Y9
BUCK0_FB R4
BUCK0_VSS_FB R5

CRITICAL L8100 1.0UH-20%-4A-0.034OHM PPVDD_AWAKE_PCPU
BUCK0_LX0 SWITCH_NODE=TRUE DIDT=TRUE
PIKD20161B 152S01283
CRITICAL L8101 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM
BUCK0_LX1 SWITCH_NODE=TRUE DIDT=TRUE
CRITICAL L8102 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM
BUCK0_LX2 SWITCH_NODE=TRUE DIDT=TRUE
BUCK0_LX4 SWITCH_NODE=TRUE DIDT=TRUE
152S01268
R8100 0 0% 1/20W TK 0201
BUCK0_FB BUCK0_FB_R
XW8100 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1
BOMOPTION=PMU_FB:FF

PPVDD_AWAKE_PCPU
CRITICAL 138S1058 C8100 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8101 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8102 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8103 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8104 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8105 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8106 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8107 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8108 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8109 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C810A 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C810B 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S00039 C810C 2.2UF 20% 6.3V X6S-CERM 0201
CRITICAL 138S00039 C810D 2.2UF 20% 6.3V X6S-CERM 0201

BUCK1_LX0 A6
BUCK1_LX0 B6
BUCK1_LX1 C1
BUCK1_LX1 C2
BUCK1_LX1 C3
BUCK1_LX1 C4
BUCK1_LX3 E1
BUCK1_LX3 E2
BUCK1_LX3 E3
BUCK1_LX3 E4
BUCK1_LX2 G1
BUCK1_LX2 G2
BUCK1_LX2 G3
BUCK1_LX2 G4
BUCK1_LX4 J1
BUCK1_LX4 J2
BUCK1_LX4 J3
BUCK1_LX4 J4
BUCK1_FB D6
BUCK1_VSS_FB E6

CRITICAL L8110 1.0UH-20%-4A-0.034OHM PPVDD_AWAKE_GPU
BUCK1_LX0 SWITCH_NODE=TRUE DIDT=TRUE
PIKD20161B 152S01283
CRITICAL L8111 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM
BUCK1_LX1 SWITCH_NODE=TRUE DIDT=TRUE
CRITICAL L8112 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM
BUCK1_LX2 SWITCH_NODE=TRUE DIDT=TRUE
BUCK1_LX4 SWITCH_NODE=TRUE DIDT=TRUE
152S01268
R8110 0 0% 1/20W TK 0201
BUCK1_FB BUCK1_FB_R
XW8110 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1
BOMOPTION=PMU_FB:FF

PPVDD_AWAKE_GPU
CRITICAL 138S1058 C8110 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8111 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8112 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8113 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8114 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8115 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8116 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8117 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8118 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8119 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C811A 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C811B 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C811C 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C811D 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S00039 C811E 2.2UF 20% 6.3V X6S-CERM 0201
CRITICAL 138S00039 C811F 2.2UF 20% 6.3V X6S-CERM 0201

BUCK2_LX0 Y19
BUCK2_LX1 U20
BUCK2_LX1 U21
BUCK2_LX3 R20
BUCK2_LX3 R21
BUCK2_LX2 W17
BUCK2_LX2 Y17
BUCK2_LX4 W15
BUCK2_LX4 Y15
BUCK2_FB U18
BUCK2_VSS_FB T18

CRITICAL L8120 1.0UH-20%-4A-0.034OHM PPVDD_S1_SOC
BUCK2_LX0 SWITCH_NODE=TRUE DIDT=TRUE
PIKD20161B 152S01283
CRITICAL L8121 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM
BUCK2_LX1 SWITCH_NODE=TRUE DIDT=TRUE
CRITICAL L8122 0.1UH-20%-10.3A-0.01OHM PCCE20161B-SM
BUCK2_LX2 SWITCH_NODE=TRUE DIDT=TRUE
BUCK2_LX4 SWITCH_NODE=TRUE DIDT=TRUE
152S01268
R8120 0 0% 1/20W TK 0201
BUCK2_FB BUCK2_FB_R
XW8120 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1
BOMOPTION=PMU_FB:FF

PPVDD_S1_SOC
CRITICAL 138S1058 C8120 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8121 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8122 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8123 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8124 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8125 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8126 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8127 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8128 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C8129 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S00039 C812A 2.2UF 20% 6.3V X6S-CERM 0201
CRITICAL 138S00039 C812B 2.2UF 20% 6.3V X6S-CERM 0201
CRITICAL 138S1058 C812C 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S1058 C812D 15UF 20% 6.3V X6S 0402-2
CRITICAL 138S00039 C812E 2.2UF 20% 6.3V X6S-CERM 0201
CRITICAL 138S00039 C812F 2.2UF 20% 6.3V X6S-CERM 0201

BOM_COST_GROUP=SOC POWER

PAGE TITLE
MPMU: INPUT PWR, BUCK 0, 1, 2

Apple Inc.

DRAWING NUMBER 051-07754
SIZE D
REVISION 6.0.0
BRANCH dvt-1
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OMIT_TABLE
998-23524

U8100
STOWE_00
CSP
SYM 2 OF 5

MPMU_BSTLQ_LX — T15 BSTLQ_LX
PP5V_MPMU_BSTLQ_XW — T16 BSTLQ_VOUT
PP5V_MPMU_BSTLQ — D17 VDD_HI_INT1, G7 VDD_HI_INT2, E21 VDD_HI_INT3, M19 VDD_HI_INT4, J15 VDD_HI_INT5
PP1V25_S2 — N13 VDDIO_1V2
PP1V8_S2 — P15 VDDIO_1V8
PP1V2_AON_MPMU — M13 VDDIO_1V2_1V8
PPVREF_MPMU — H11 VREF
PP1V5_MPMU_VREFADC — H7 VREF_ADC
GND_VREF_RTN_MPMU — H9 VBAT
GND_VREF_RTN_MPMU — H8 IBAT
MPMU_VBAT — XIN
MPMU_IBAT — XOUT
NC_MPMU_XIN — M21 XIN
MPMU_XOUT — L21 XOUT
PMU_CLK32K_SOC_R — M7 SLEEP_32K
PMU_CLK32K_WLBT_R — M8 OUT_32K
PP1V8_S2 — N20 VDD_SW1
PP1V8_S2 — N16 VDD_SW2
PP1V25_S2 — N18 VDD_SW3

BUCK OUTPUTS
CLOCK
LOAD SWITCHES

BUCK3_LX — A18, B18
BUCK3_FB — D18
BUCK3_VSS_FB — C18
BUCK4_LX0 — A16
BUCK4_LX1 — A14, B14
BUCK4_LX2 — A12, B12
BUCK4_FB — D16
BUCK4_VSS_FB — C16
BUCK7_LX0 — N1
BUCK7_LX1 — L1, L2, L3
BUCK7_FB — N4
BUCK7_VSS_FB — N3
BUCK9_LX0 — A8
BUCK9_LX1 — A10, B10, C10
BUCK9_FB — D8
BUCK9_VSS_FB — C8
BUCK11_LX0 — Y13
BUCK11_LX1 — V11, W11, Y11
BUCK11_FB — U13
BUCK11_VSS_FB — V13
BUCK13_LX — A20, B20, C20
BUCK13_FB — E20
BUCK13_VSS_FB — D20
VSW1 — N21
VSW2 — N17
VSW3 — N19

BUCK3_LX: CRITICAL L8230 0.47UH-20%-4A-0.024OHM, PIKD20121B-SM, 152S01263, SWITCH_NODE=TRUE, DIDT=TRUE
BUCK3_FB: R8230 0 0% 1/20W TK 0201 — BUCK3_FB_R — XW8230 SHORT-16L-0.1MM-SM, 998-14727, NO_XNET_CONNECTION=1 — PP1V8_S2
BUCK4_LX0: CRITICAL L8240 1.0UH-20%-4A-0.034OHM, PIKD20161B, 152S01283, SWITCH_NODE=TRUE, DIDT=TRUE
BUCK4_LX1/LX2: CRITICAL L8241 0.1UH-20%-10.3A-0.01OHM, PCCE201618-SM, 152S01268, SWITCH_NODE=TRUE, DIDT=TRUE
BUCK4_FB: R8240 0 0% 1/20W TK 0201 — BUCK4_FB_R — XW8240 SHORT-16L-0.1MM-SM, 998-14727, NO_XNET_CONNECTION=1 — PPVDD_S2SW_VDD2H
BOMOPTION=PMU_FB:FF
BUCK7_LX0: CRITICAL L8270 1.0UH-20%-4A-0.034OHM, PIKD20161B, 152S01283, SWITCH_NODE=TRUE, DIDT=TRUE
BUCK7_LX1: CRITICAL L8271 0.22UH-20%-6.7A-0.023OHM, PINA20121T-SM, 152S00204, SWITCH_NODE=TRUE, DIDT=TRUE
BUCK7_FB: R8270 0 0% 1/20W TK 0201 — BUCK7_FB_R — XW8270 SHORT-16L-0.1MM-SM, 998-14727, NO_XNET_CONNECTION=1 — PPVDD_AWAKE_CPU_SRAM
BOMOPTION=PMU_FB:FF
BUCK9_LX0: CRITICAL L8290 1.0UH-20%-4A-0.034OHM, PIKD20161B, 152S01283, SWITCH_NODE=TRUE, DIDT=TRUE — PPVDD_S1_DCS
BUCK9_LX1: CRITICAL L8291 0.22UH-20%-6.7A-0.023OHM, PINA20121T-SM, 152S00204, SWITCH_NODE=TRUE, DIDT=TRUE
BUCK9_FB: R8290 0 0% 1/20W TK 0201 — BUCK9_FB_R — XW8290 SHORT-16L-0.1MM-SM, 998-14727, NO_XNET_CONNECTION=1
BOMOPTION=PMU_FB:FF
BUCK11_LX0: CRITICAL L82B0 1.0UH-20%-4A-0.034OHM, PIKD20161B, 152S01283, SWITCH_NODE=TRUE, DIDT=TRUE
BUCK11_LX1: CRITICAL L82B1 0.22UH-20%-6.7A-0.023OHM, PINA20121T-SM, 152S00204, SWITCH_NODE=TRUE, DIDT=TRUE
BUCK11_FB: R82B0 0 0% 1/20W TK 0201 — BUCK11_FB_R — XW82B0 SHORT-16L-0.1MM-SM, 998-14727, NO_XNET_CONNECTION=1 — PPVDD_AWAKE_ECPU
BOMOPTION=PMU_FB:FF
BUCK13_LX: CRITICAL L82D0 0.47UH-20%-6.9A-0.022OHM, MEMK2520-SM, 152S01325, SWITCH_NODE=TRUE, DIDT=TRUE — PP1V25_S2
BUCK13_FB: R82D0 0 0% 1/20W TK 0201 — BUCK13_FB_R — XW82D0 SHORT-16L-0.1MM-SM, 998-14727, NO_XNET_CONNECTION=1

PP1V8_AWAKE
NC_PPVOUT_MPMU_SW2_REG
PP1V25_AWAKE_IO

VSW1 700MA MAX, 23MOHM MAX
VSW2 350MA MAX, 125MOHM MAX
VSW3 200MA MAX, 23MOHM MAX

PP1V8_S2: CRITICAL 138S00073 C8230–C8239, C823A, C823B 10UF 20% 6.3V CER-X6S 0402-COMBO
PPVDD_S2SW_VDD2H: CRITICAL 138S1058 C8240–C8249, C824A, C824B 15UF 20% 2V X6S 0402-2; CRITICAL 138S00039 C824C, C824D 2.2UF 20% 4V X6S-CERM 0201
PPVDD_AWAKE_CPU_SRAM: CRITICAL 138S1058 C8270–C8276 15UF 20% 2V X6S 0402-2; CRITICAL 138S00039 C8277–C8279 2.2UF 20% 4V X6S-CERM 0201
PPVDD_S1_DCS: CRITICAL 138S00039 C8298, C8299 2.2UF 20% 4V X6S-CERM 0201; CRITICAL 138S1058 C8290–C8296 15UF 20% 2V X6S 0402-2; CRITICAL 138S00073 C8297 15UF 20% 2V X6S 0402-2; NOSTUFF, NOSTUFF
PPVDD_AWAKE_ECPU: CRITICAL 138S1058 C82B0–C82B6 15UF 20% 2V X6S 0402-2; CRITICAL 138S00039 C82B8, C82B9 2.2UF 20% 4V X6S-CERM 0201
PP1V25_S2: CRITICAL 138S1058 C82D0–C82D5 15UF 20% 2V X6S 0402-2

VDD_SW1: PP1V8_S2 — PLACE_NEAR=U8100.N20:5MM — CRITICAL 138S00073 C8200 10UF 20% 6.3V CER-X6S 0402-COMBO
VDD_SW3: PP1V25_S2 — PLACE_NEAR=U8100.N18:5MM — CRITICAL 138S00073 C8201 10UF 20% 6.3V CER-X6S 0402-COMBO
VDD_SW2: PP1V8_S2 — PLACE_NEAR=U8100.N16:5MM — CRITICAL 138S00073 C8220 10UF 20% 6.3V CER-X6S 0402-COMBO — DNI=TRUE, PACK_IGNORE=TRUE, PACK_OPTION=MPMD_VSW2

VSW1: PP1V8_AWAKE — CRITICAL 138S00073 C8202, C8203 10UF 20% 6.3V CER-X6S 0402-COMBO
VSW2: NC_PPVOUT_MPMU_SW2_REG — CRITICAL 138S00073 C8221 10UF 20% 6.3V CER-X6S 0402-COMBO — DNI=TRUE, PACK_IGNORE=TRUE, PACK_OPTION=MPMD_VSW2; CRITICAL 138S00073 C8222 10UF 20% 6.3V CER-X6S 0402-COMBO — PACK_IGNORE=TRUE, PACK_OPTION=MPMD_VSW2
VSW3: PP1V25_AWAKE_IO — CRITICAL 138S00073 C8204, C8205 10UF 20% 6.3V CER-X6S 0402-COMBO

BOM_COST_GROUP=SOC POWER

PAGE TITLE	MPMU: BUCK 3, 4, 7, 9, 11, 13, SW
	Apple Inc.
DRAWING NUMBER	051-07754
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BRANCH	dvt-1
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OMIT_TABLE
998-23524

U8100
STOWE_00
CSP
SYM 3 OF 5

VDDMAIN>>
129 PP3V8_AON_MPMU_ISNS_VIN — F15 VDD_CTRL_LDOG

129 46 44 43 41 PP3V8_AON_MPMU_ISNS_VIN — G17 VDD_BOOST_LDO; G18 VDD_BOOST_LDO; H17 VDD_BOOST_LDO; H18 VDD_BOOST_LDO; J18 VDD_BOOST_LDO

129 46 44 43 41 PP3V8_AON_MPMU_ISNS_VIN — J17 VDD_MAIN_LDO; K17 VDD_MAIN_LDO; K19 VDD_MAIN_LDO

PORTABLES: SHORT TO VDD_MAIN >>
DESKTOPS: CONNECT TO CON CELL >>
129 PP3V8_AON_MPMU_ISNS_VIN — L18 VDD_RTC_ALT

BUCK3 OR BUCK13>>
47 43 PPVDD_LDO20_14_8_3 — F19 VDD_LDO20_14_8_3; F20 VDD_LDO20_14_8_3; G20 VDD_LDO20_14_8_3; H20 VDD_LDO20_14_8_3

BUCK4>>
125 43 PPVDD_S2SW_VDD2H — J20 VDD_LDO11

BUCK4>>
125 PPVDD_S2SW_VDD2H — F16 VDD_LDO16

46 IN NC_MPMU_LDO1_EN — R13 LDO1_EN

LDO INPUTS

LDO OUTPUTS

VLDO1 G19 NC_MPMU_VLDO1 — 126
VLDO2 J16 PP1V8_AON — 126
VLDO3 F18 NC_MPMU_VLDO3 — 126
VLDO5 G16 NC_MPMU_VLDO5 — 126
VLDO7 H19 PP3V3_S2_LDO — 126
VLDO8 H21 PP1V2_AWAKE_PLL — 127
VLDO9 K16 PP1V8_AON_MPMU — 127
VLDO9B K18 PP1V2_AON_MPMU — 127
VLDO10 H16 PP3V3_AON — 127
VLDO11 J21 PP0V855_S2SW_CIO — 127
VLDO13 J19 PP3V3_S2SW_SNS — 127
VLDO14 F21 NC_MPMU_VLDO14 — 127
VLDO16 F17 NC_MPMU_VLDO16 — 127
VLDO20 G21 PP1V2_S2_CIO — 127
VLDOINT K20 PP1V5_LDOINT_MPMU — 127
VLDORTC L19 PP1V5_LDOINT_MPMU — 43 127
VLDORTC2 L20 GND — 43 46

LDO1	300MA MAX	
LDO2	50MA MAX	
LDO3	600MA MAX	
LDO5	250MA MAX	
LDO7	250MA MAX	
LDO8	730MA MAX	
LDO9	10MA MAX	
LDO9B	10MA MAX	
LDO10	250MA MAX	
LDO11	1000MA MAX	
LDO13	250MA MAX	
LDO14	300MA MAX	
LDO16	1500MA MAX	
LDO20	400MA MAX	
LDOINT	150MA MAX	

VLDORTC: SHORT TO LDO_INT FOR PORTABLES
VLDORTC: CONNECT TO DECOUPLING CAP (ENABLE PACK_OPTION: PMU_DESKTOPS)

VLDORTC2: SHORT TO GND ONLY IF LDORTC2 IS DISABLED PER OTP (PORTABLES)
VLDORTC2: DEV/DESKTOP HAVE OPTIONS TO USE LDORTC2

UN-UNUSED LDOS

LDO 3, 5, 14, 16

VDD LDO 3/8/14/20

47 43 PPVDD_LDO20_14_8_3
C8300 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
C8301 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDO2 DECOUPLING

126 PP1V8_AON
C8320 CRITICAL 138S0750 4.7UF 20% 6.3V X6S 0402
PACK_OPTION=PMU_LDO2

VLDO9 DECOUPLING

127 45 PP1V8_AON_MPMU
C8310 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
C8311 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDO11 DECOUPLING

127 PP0V855_S2SW_CIO
C83B5 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
C83B6 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDOINT DECOUPLING

127 PP1V5_LDOINT_MPMU
C8380 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
C8381 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO

VDD_LDO11

125 43 PPVDD_S2SW_VDD2H
C83B0 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
C83B1 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDO7 DECOUPLING

126 PP3V3_S2_LDO
C8330 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
C8331 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDO9B DECOUPLING

127 PP1V2_AON_MPMU
C8340 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
C8341 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDO13 DECOUPLING

127 PP3V3_S2SW_SNS
C83D0 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDORTC DECOUPLING

PP1V5_LDOINT_MPMU 43 127
C8370 CRITICAL 138S0750 4.7UF 20% 6.3V X6S 0402
PACK_IGNORE=TRUE
PACK_OPTION=PMU_DESKTOPS

VLDO1 DECOUPLING

=PPVOUT_MPMU_VLDO1
C8390 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
C8391 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
PACK_IGNORE=TRUE
PACK_OPTION=PMU_LDO1
PACK_IGNORE=TRUE
PACK_OPTION=PMU_LDO1

VLDO8 DECOUPLING

127 PP1V2_AWAKE_PLL
C8360 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
C8361 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
C8362 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
NOSTUFF

VLDO10 DECOUPLING

127 PP3V3_AON
C83A0 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
PACK_OPTION=PMU_LDO10

VLDO20 DECOUPLING

127 PP1V2_S2_CIO
C8350 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO
C8351 CRITICAL 138S00073 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDORTC2 DECOUPLING

GND 43 46
C8371 138S00040 1UF 20% 6.3V X5S-CERM 0201
PMU_RTC_LDO:INT2
PACK_IGNORE=TRUE
PMU_DESKTOPS

BOM_COST_GROUP=SOC POWER

PAGE TITLE: MPMU: LDO

Apple Inc.

DRAWING NUMBER: 051-07754
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
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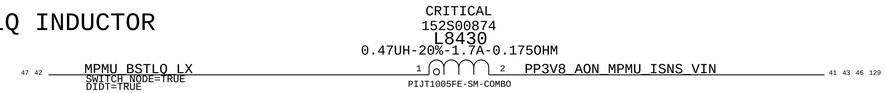
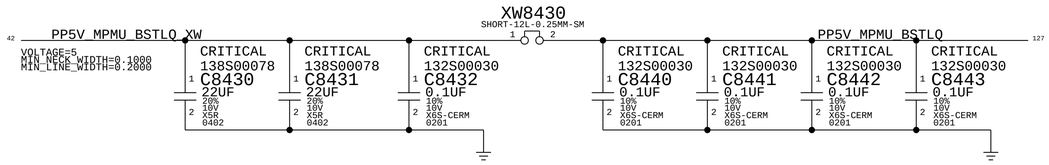
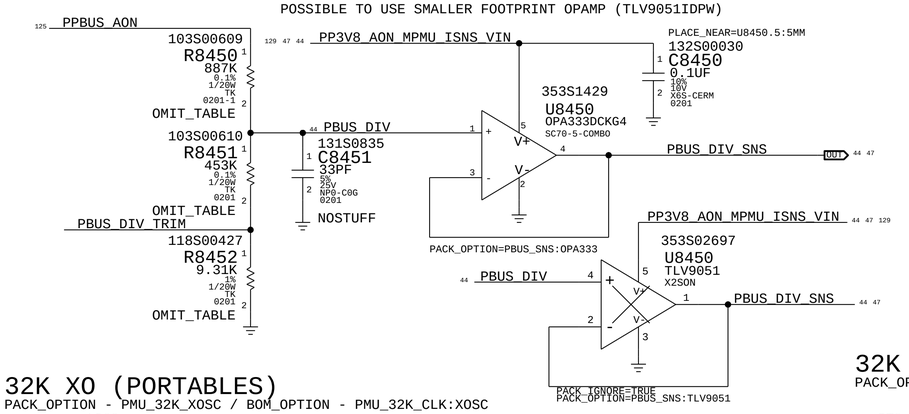
BSTLQ INDUCTOR





PBUS SENSE



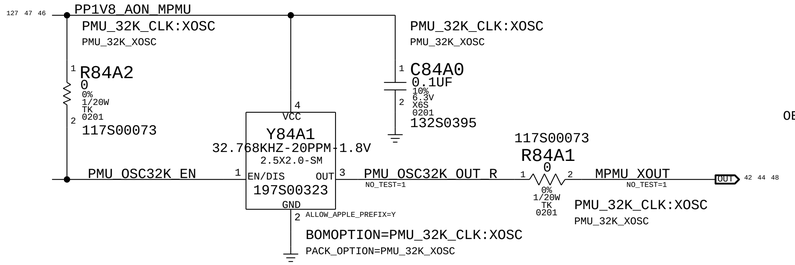
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
103S00609	1	RES,TK,887KOHM,0.1%,50PPM,1/20W,0201	R8450	PMU_PBUS:BATT3S
103S00610	1	RES,TK,453KOHM,0.1%,50PPM,1/20W,0201	R8451	PMU_PBUS:BATT3S
117S00073	1	RES,TK,0OHM,1A MAX,1/20W,0201	R8452	PMU_PBUS:BATT3S
103S00669	1	RES,TK,910 KOHM,0.1%,1/20W,0201	R8450	PMU_PBUS:12V
103S00661	1	RES,TK,280K OHM,0.1%,50PPM,1/20W,0201	R8451	PMU_PBUS:12V
117S00073	1	RES,TK,0OHM,1A MAX,1/20W,0201	R8452	PMU_PBUS:12V
103S00609	1	RES,TK,887KOHM,0.1%,50PPM,1/20W,0201	R8450	PMU_PBUS:15V8
103S00658	1	RES,TK,205K OHM,0.1%,50PPM,1/20W,0201	R8451	PMU_PBUS:15V8
117S00073	1	RES,TK,0OHM,1A MAX,1/20W,0201	R8452	PMU_PBUS:15V8
103S00669	1	RES,TK,910 KOHM,0.1%,1/20W,0201	R8450	PMU_PBUS:DEV_DUAL
103S00661	1	RES,TK,280K OHM,0.1%,50PPM,1/20W,0201	R8451	PMU_PBUS:DEV_DUAL
117S00073	1	RES,TK,0OHM,1A MAX,1/20W,0201	R8452	PMU_PBUS:DEV_DUAL

PMU_PBUS:DEV_DUAL IS POTENTIALLY USED IN DEV BOARD ON OTHER PAGES.
R8452 SHOULD BE 118S00427 (9.31K) IF ENABLING BOOST_SNS PULL DOWN CIRCUIT (NON POR)

32K XO (PORTABLES)

PACK_OPTION - PMU_32K_XOSC / BOM_OPTION - PMU_32K_CLK:XOSC

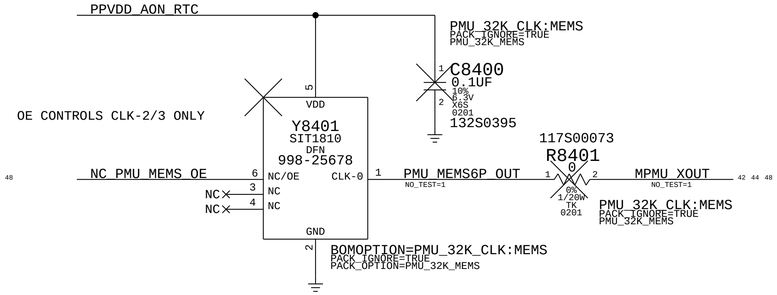
>> LDO9



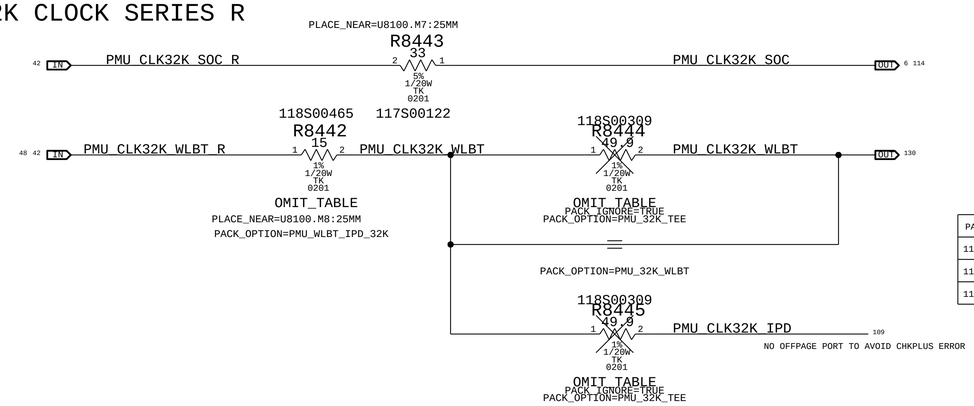
32K MEMS CLOCK (DESKTOPS)

PACK_OPTION - PMU_32K_MEMS / BOM_OPTION - PMU_32K_CLK:MEMS

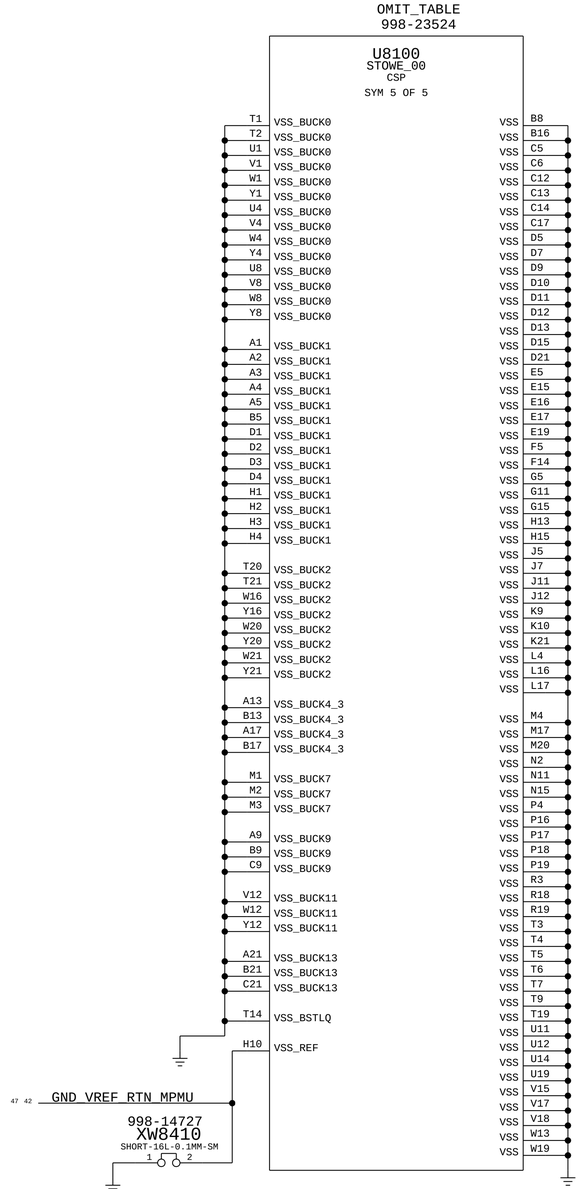
>> RTC SUPPLY (DISCRETE, VLDORTC, OR VLDORTC2)



32K CLOCK SERIES R



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S00465	1	RES,TK,15 OHM,1%,1/20W,0201	R8442		PMU_OUT32K:TEE
117S00122	1	RES,TK,33 OHM,5%,1/20W,0201	R8442		PMU_OUT32K:WLBT
118S00309	2	RES,TK,49.9 OHM,1%,1/20W,0201	R8444,R8445		PMU_OUT32K:TEE



PLACEMENT NOTES

CONNECT VSS_REF THROUGH ALL GND LAYERS
PLACE XW AT VSS_REF PIN, ROUTE RTN SIGNAL BACK TO PASSIVES

BOM_COST_GROUP=SOC POWER

PAGE TITLE: MPMU: MISC CKT, VSS

Apple Inc.

DRAWING NUMBER: 051-07754 | SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
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*** OK2INTEGRATE ***

OMIT_TABLE
998-23524

U8100
STOWE_00
CSP
SYM 4 OF 5

63	IN	P3V8AONVR_THMSNS	F8	TDEV1			
63	IN	SOC_THMSNS	F13	TDEV2			
63	IN	WLBT_THMSNS	F9	TDEV3			
63	IN	MPMU_AMUXTDEV_TERM	F10	TDEV4			
63	IN	MPMU_AMUXTDEV_TERM	F11	TDEV5			
63	IN	IOPORT_THMSNS	F12	TDEV6			
63	IN	MPMU_THMSNS	G9	TDEV7			
63	IN	CHGR_THMSNS	G8	TDEV8			
		MPMU_TCAL	E14	TCAL			
46	IN	GND	E13	BRICK_ID1			
46	IN	GND	E9	BRICK_ID2			
46	IN	MPMU_ADC_IN	G14	ADC_IN			
62	IN	DCIN_VSENSE	E11	AMUX_A<0>			
62	IN	DCIN_ISENSE	E10	AMUX_A<1>			
62	IN	PBUS_VSENSE	E8	AMUX_A<2>			
62	IN	BMON_ISENSE	E7	AMUX_A<3>			
47	BI	MPMU_AMUX_AY	G13	AMUX_AY			
62	IN	P3V8AON_IMEAS	E12	AMUX_B<0>			
62	IN	MESA_HS_ISENSE	F6	AMUX_B<1>			
62	IN	MPMU_AMUXTDEV_TERM	F7	AMUX_B<2>			
62	IN	MPMU_AMUXTDEV_TERM	G6	AMUX_B<3>			
47	BI	MPMU_AMUX_BY	G10	AMUX_BY			
46	IN	PMU_ONOFF_L	N12	BUTTON1			
48	IN	PMU_RSLOC_RST_L	L13	BUTTON2			
46	IN	NC_MPMU_BUTTON3	K15	BUTTON3			
46	IN	NC_MPMU_BUTTON4	K13	BUTTON4			
46	IN	NC_MPMU_RESET_IN0	K7	RESET_IN0			
48	IN	SOC_WDOG	L9	RESET_IN1			
46	IN	UPC_PMU_RESET_1V2	K5	RESET_IN2			
48	IN	SOC_SOCHOT_L	M9	RESET_IN3			
116 113 46	IN	MPMU_SHDN	K11	SHDN			
46	IN	MPMU_REQUEST_DFU	L12	REQUEST_DFU			
48	IN	NC_MPMU_VBUS_DET	L11	VBUS_DETECT			
14	IN	SPMI_NUB_MPMU_CLK	M14	SPMI_SCLK			
14	BI	SPMI_NUB_MPMU_DATA	M15	SPMI_SDATA			
39	OUT	SGPIO_SCLK	P14	SGPIO_SCLK			
39	BI	SGPIO_SDATA	N14	SGPIO_SDATA			
117 39	OUT	PMU_SGPIO_READY_REQ	P13	SGPIO_READY_REQ			
130	BI	SWD_NUB_SWDIO_MPMU	K12	SWD_TMS			
46	IN	GND	J14	DFT_CTRL0			
130	IN	SWD_NUB_SWCLK_MPMU	J13	DFT_CTRL1			
46	IN	GND	H12	DFT_CTRL2			
46	IN	MPMU_OTP_SEL	N5	OTP_SEL			
48		GND	K8	VPP			

ADC / GPIO

	GPIO0	R12	IPD_LID_OPEN_1V8	BI	46
	GPIO1	R6	CODEC_WAKE_L	BI	46
	GPIO2	M11	NC_SENSOR_PWR_EN	BI	46
	GPIO3	P9	SDCONN_STATE_CHANGE	BI	46
HLD	GPIO4	M10	CHGR_AUX_OK	BI	46
	GPIO5	N9	WLBT_WAKE	BI	46
HLD	GPIO6	T10	IPD_PWR_EN	BI	46
	GPIO7	N10	NC_MPMU_GPIO_7	BI	46
SEQ	GPIO8	T11	IPD_TOUCH_RESET_L	BI	46
SEQ	GPIO9	U15	DP2HDMI_RESET_L	BI	46 117
SEQ	GPIO10	U16	LCD_PWR_EN	BI	46
SEQ	GPIO11	P11	NC_P3V3S2_PWR_EN	BI	46
SEQ	GPIO12	P12	PVDD1_PWR_EN	BI	46
SEQ	GPIO13	R15	WLBT_PWR_EN	BI	46
SEQ	GPIO14	P7	IPD_WAKE_L	BI	46
SEQ	GPIO15	P6	SE_PWR_EN	BI	46
SEQ	GPIO16	P5	HDMI_CECFET_EN	BI	46
SEQ	GPIO17	R8	NAND0_LPB_L	BI	46
SEQ	GPIO18	R9	BL_PWR_EN	BI	46
SEQ,HLD	GPIO19	R7	P3V8AON_LPM	BI	46
SEQ,HLD	GPIO20	R10	P5VS2HOLD_PWR_EN	BI	46
SEQ	GPIO21	P10	DP2HDMI_PWR_EN_PMU	BI	46
SEQ	GPIO22	R11	HDMI_PWR_EN	BI	46
SEQ	GPIO23	T12	SD_PWR_EN	BI	46
SEQ	GPIO24	T13	IPD_MCU_RESET_L	BI	46
SEQ	GPIO25	R16	NC_P2V5_NAND0_DISCHARGE_EN	BI	46
SEQ,HV	GPIO26	R17	BL_PMIC_PWR_EN	BI	46

BUTTONS

BUTTON1	BUTTONO1	L14	NC_MPMU_BUTTONO1	OUT 46
BUTTON2	BUTTONO2	K14	NC_MPMU_BUTTONO2	OUT 46
BUTTON3	BUTTONO3	M12	NC_MPMU_BUTTONO3	OUT 46
	DBLCLICK_DET	T17	DBL_CLICK_DET	OUT 48
	RESET*	L6	PMU_RESET_L	OUT 48

STATE MACHINE

	FORCE_DFU	H14	MPMU_SOC_FORCE_DFU_R	
	WAKE2MS	R14	NC_MPMU_WAKE2MS	OUT 46
	OFF_REQ	U17	NC_MPMU_OFF_REQ	OUT 46
	SYS_ALIVE	K6	PMU_SYS_ALIVE	OUT 46 47 91 113
	ACTIVE_READY	L10	PMU_ACTIVE_READY	OUT 48
	CRASH*	L8	PMU_CRASH_L	BI 46 47 114
	FAULT_OUT*	L7	MPMU_FAULT_OUT_L	OUT 46
	SCRASH*	M6	MPMU_SCRASH_L	BI 39 114

INTERFACE / THROTTLE

	THROTTLE0*	L5	BUCK0_THERMAL_THROTTLE_L	OUT 46 48
	THROTTLE1*	N7	BUCK1_THERMAL_THROTTLE_L	OUT 46 48
	THROTTLE2*	P8	TPT_MPMU_THROTTLE2_L	OUT 46 48
	THROTTLE3*	N8	MPMU_VDDHI_UVWARN_L	OUT 46 48
	UVWARN*	M5	MPMU_VDDMAIN_UVWARN_L	OUT 46 48

103S00584
R8550
3.92K
0.1% 1/20W TK 0201

131S0805
C8550
100PF
5% 25V C0G 0201

63 47 GND_TCAL_MPMU
VOLTAGE=0V

117S00113
R8540
20
5% 1/20W TK 0201

117S00113
R8541
20
5% 1/20W TK 0201

OTP: PMOS OD

117S00129
R8563
47K
5% 1/20W TK 0201

117S00099
R8562
2.2K
5% 1/20W TK 0201

SOC_FORCE_DFU OUT 48

NOSTUFF
117S00090
R8561
10K
5% 1/20W TK 0201

PP1V8_AON_MPMU 43 127

>> IPU: LDO9

117S00077
R8560
1K
5% 1/20W TK 0201-1

BOM_COST_GROUP=SOC POWER

PAGE TITLE	MPMU: GPIO
Apple Inc.	DRAWING NUMBER 051-07754
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*** PROJECT SPECIFIC ***

IO OTP SETTINGS, ">iBoot" SUGGESTS IT WILL BE RECONFIGURED AS IBOOT OVERRIDE..
SUPPLY:LDO9 (1.8V AON), BUCK13 (1.25V S2), BUCK3 (1.8V S2), SLDO9B (1.2V AON)
IO TYPE: INPUT, OUTPUT OPEN DRAIN, OR OUTPUT PUSH PULL
PULLS: IPU, IPD, NONE

```
GPIO0:  LDO9   IN  IPD
GPIO1:  BUCK13 IN  IPU
GPIO2:  LDO9   IN  IPD
GPIO3:  BUCK13 IN  IPU
GPIO4:  LDO9   IN  IPU
GPIO5:  BUCK13 IN  IPD
GPIO6:  LDO9   PP  NONE
GPIO7:  LDO9   IN  IPD
>iBoot: BUCK13 IN  IPD
GPIO8:  LDO9   PP  NONE
GPIO9:  LDO9   IN  IPD
GPIO10: LDO9   IN  IPD
>iBoot: LDO9   PP  NONE
GPIO11: LDO9   PP  NONE
>iBoot: LDO9   IN  IPD
GPIO12: LDO9   PP  NONE
GPIO13: LDO9   PP  NONE
GPIO14: LDO9   IN  NONE
GPIO15: LDO9   PP  NONE
>iBoot: BUCK13 PP  NONE
GPIO16: LDO9   IN  IPD
>iBoot: LDO9   PP  NONE
GPIO17: BUCK13 PP  NONE
GPIO18: BUCK13 IN  IPD
>iBoot: BUCK13 PP  NONE
GPIO19: LDO9   PP  NONE
GPIO20: LDO9   PP  NONE
GPIO21: LDO9   IN  IPD
>iBoot: LDO9   PP  NONE
GPIO22: LDO9   IN  IPD
>iBoot: LDO9   PP  NONE
GPIO23: LDO9   IN  IPD
>iBoot: LDO9   PP  NONE
GPIO24: LDO9   PP  NONE
GPIO25: LDO9   PP  NONE
>iBoot: LDO9   IN  IPD
GPIO26: LDO9   IN  IPD
>iBoot: BUCK13 PP  NONE
```

45 BI IPD_LID_OPEN_1V8 = IPD_LID_OPEN_1V8 MAKE_BASE=TRUE — 99 110 114
45 BI CODEC_WAKE_L = CODEC_WAKE_L MAKE_BASE=TRUE — 101
45 BI NC_SENSOR_PWR_EN = NC_SENSOR_PWR_EN MAKE_BASE=TRUE NO_TEST=1
45 BI SDCONN_STATE_CHANGE = SDCONN_STATE_CHANGE MAKE_BASE=TRUE — 85
45 BI CHGR_AUX_OK = CHGR_AUX_OK MAKE_BASE=TRUE — 113 130
45 BI WLBT_WAKE = WLBT_WAKE MAKE_BASE=TRUE — 87 88
45 BI IPD_PWR_EN = IPD_PWR_EN MAKE_BASE=TRUE — 107 110
45 BI NC_MPMU_GPIO_7 = NC_MPMU_GPIO_7 MAKE_BASE=TRUE
45 BI IPD_TOUCH_RESET_L = IPD_TOUCH_RESET_L MAKE_BASE=TRUE — 46 109
117 45 BI DP2HDMI_RESET_L = DP2HDMI_RESET_L MAKE_BASE=TRUE — 81
45 BI LCD_PWR_EN = LCD_PWR_EN MAKE_BASE=TRUE — 95
45 BI NC_P3V3S2_PWR_EN = NC_P3V3S2_PWR_EN MAKE_BASE=TRUE — 48
45 BI PVDD1_PWR_EN = PVDD1_PWR_EN MAKE_BASE=TRUE — 50
45 BI WLBT_PWR_EN = WLBT_PWR_EN MAKE_BASE=TRUE — 46 87 88
45 BI IPD_WAKE_L = IPD_WAKE_L MAKE_BASE=TRUE — 109 114
45 BI SE_PWR_EN = SE_PWR_EN MAKE_BASE=TRUE — 27 46 117
45 BI HDMI_CECFET_EN = HDMI_CECFET_EN MAKE_BASE=TRUE — 78
45 BI NAND0_LPB_L = NAND0_LPB_L MAKE_BASE=TRUE — 89 90 91
45 BI BL_PWR_EN = BL_PWR_EN MAKE_BASE=TRUE — 96
45 BI P3V8AON_LPM = P3V8AON_LPM MAKE_BASE=TRUE — 34 46
45 BI P5VS2HOLD_PWR_EN = P5VS2HOLD_PWR_EN MAKE_BASE=TRUE — 36 46 130 131
45 BI DP2HDMI_PWR_EN_PMU = DP2HDMI_PWR_EN_PMU MAKE_BASE=TRUE — 130
45 BI HDMI_PWR_EN = HDMI_PWR_EN MAKE_BASE=TRUE — 78
45 BI SD_PWR_EN = SD_PWR_EN MAKE_BASE=TRUE — 86
45 BI IPD_MCU_RESET_L = IPD_MCU_RESET_L MAKE_BASE=TRUE — 46 109
45 BI NC_P2V5_NAND0_DISCHARGE_EN = NC_P2V5_NAND0_DISCHARGE_EN MAKE_BASE=TRUE NO_TEST=1
45 BI BL_PMIC_PWR_EN = BL_PMIC_PWR_EN MAKE_BASE=TRUE — 97 113

45 OUT PMU_ONOFF_L = PMU_ONOFF_L MAKE_BASE=TRUE — 46 47 111 113 116

BUTTON2 DIFFERENT BETWEEN FF AND DEV >> ALIAS IN OTHER PAGE

45 NC_MPMU_BUTTON3 = NC_MPMU_BUTTON3 MAKE_BASE=TRUE NO_TEST=1
45 NC_MPMU_BUTTON4 = NC_MPMU_BUTTON4 MAKE_BASE=TRUE NO_TEST=1
45 NC_MPMU_BUTTONO1 = NC_MPMU_BUTTONO1 MAKE_BASE=TRUE NO_TEST=1
45 NC_MPMU_BUTTONO2 = NC_MPMU_BUTTONO2 MAKE_BASE=TRUE NO_TEST=1
45 NC_MPMU_BUTTONO3 = NC_MPMU_BUTTONO3 MAKE_BASE=TRUE NO_TEST=1
45 NC_MPMU_RESET_IN0 = NC_MPMU_RESET_IN0 MAKE_BASE=TRUE NO_TEST=1
45 UPC_PMU_RESET_1V2 = UPC_PMU_RESET_1V2 MAKE_BASE=TRUE — 47 114
45 GND =
45 GND =
45 GND =
45 GND = MAKE_BASE=TRUE

43 NC_MPMU_LDO1_EN = NC_MPMU_LDO1_EN MAKE_BASE=TRUE NO_TEST=1
45 NC_MPMU_OFF_REQ = NC_MPMU_OFF_REQ MAKE_BASE=TRUE NO_TEST=1
46 45 MPMU_OTP_SEL = MPMU_OTP_SEL MAKE_BASE=TRUE — 45 46
45 NC_MPMU_WAKE2MS = NC_MPMU_WAKE2MS MAKE_BASE=TRUE NO_TEST=1

VLDORTC2 SHORTED TO GND ON PORTABLES (REMOVE BELOW FOR DEV/DESKTOPS)

43 GND = MAKE_BASE=TRUE

VDD_MAIN SENSE

XW8661
SHORT-16L-0.1MM-SM
998-14727
NO_XNET_CONNECTION=1

41 PPVDD_MPMU_VDD_MAIN_SNS — 1 — 2 — PP3V8_AON_MPMU_ISNS_VIN OUT 41 43 44 129
PPVDD_MPMU_VDD_MAIN_SNS = MAKE_BASE=TRUE

46 34 P3V8AON_LPM — R8630 100K 5% 1/20W TK 0201 — 117S00095
131 130 46 36 P5VS2HOLD_PWR_EN — R8631 NOSTUFF 100K 5% 1/20W TK 0201 — 117S00095
88 87 46 WLBT_PWR_EN — R8632 NOSTUFF 100K 5% 1/20W TK 0201 — 117S00095
46 IN MPMU_ADC_IN — R8610 1M 5% 1/20W TK 0201 — 117S00096
42 IN MPMU_IBAT — R8611 1M 5% 1/20W TK 0201 — 117S00096
45 IN MPMU_REQUEST_DFU — R8612 100K 5% 1/20W TK 0201 — 117S00095
116 113 45 IN MPMU_SHDN — R8613 100K 5% 1/20W TK 0201 — 117S00095
42 IN MPMU_VBAT — R8614 1M 5% 1/20W TK 0201 — 117S00096
117 46 27 IN SE_PWR_EN — R8618 47K 5% 1/20W TK 0201 — 117S00129

RECOMMENDED NOT TO LEAVE AMUX/TDEV FLOATING.

63 62 IN MPMU_AMUXTDEV_TERM — R8616 100K 5% 1/20W TK 0201 — 117S00095

OTP_SEL (PU: DESKTOPS, PD: PORTABLES)

127 47 46 44 PP1V8_AON_MPMU
R8617 10K 5% 1/20W TK 0201 — 117S00090
BOMOPTION=PMU_OTP_SEL:PU
PACK_IGNORE=TRUE
PACK_OPTION=PMU_DESKTOPS
46 45 IN MPMU_OTP_SEL
117S00073
R8622 0 0% 1/20W TK 0201
BOMOPTION=PMU_OTP_SEL:PD
PACK_OPTION=PMU_PORTABLES

127 47 46 44 PP1V8_AON_MPMU

114 47 45 BI PMU_CRASH_L — R8620 10K 0201 TK 1/20W 5% — 117S00090

CRASH_L SET AT BIDIR <RDAR://85478086>

45 IN MPMU_FAULT_OUT_L — R8621 100K 0201 TK 1/20W 5% — 117S00095
116 113 111 47 46 IN PMU_ONOFF_L — R8623 10K 0201 TK 1/20W 5% — 117S00090
116 113 107 48 47 IN PMU_RSLOC_RST_L — R8624 10K 0201 TK 1/20W 5% — 117S00090
109 46 IN IPD_TOUCH_RESET_L — R8625 NOSTUFF 100K 0201 TK 1/20W 5% — 117S00095
109 46 IN IPD_MCU_RESET_L — R8626 NOSTUFF 100K 0201 TK 1/20W 5% — 117S00095

126 116 47 PP1V25_S2
113 91 47 45 IN PMU_SYS_ALIVE — R8640 NOSTUFF 10K 0201 TK 1/20W 5% — 117S00090

126 40 PP1V25_AWAKE_IO
48 45 IN BUCK0_THERMAL_THROTTLE_L — R8651 NOSTUFF 10K 0201 TK 1/20W 5% — 117S00090
48 45 IN BUCK1_THERMAL_THROTTLE_L — R8652 NOSTUFF 10K 0201 TK 1/20W 5% — 117S00090
48 45 IN TPT_MPMU_THROTTLE2_L — R8653 NOSTUFF 10K 0201 TK 1/20W 5% — 117S00090
48 45 IN MPMU_VDDHI_UVWARN_L — R8654 NOSTUFF 10K 0201 TK 1/20W 5% — 117S00090
48 45 IN MPMU_VDDMAIN_UVWARN_L — R8650 NOSTUFF 10K 0201 TK 1/20W 5% — 117S00090

BOM_COST_GROUP=SOC POWER

PAGE TITLE: MPMU: SUPPORT

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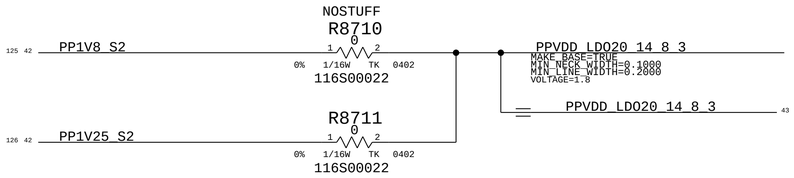
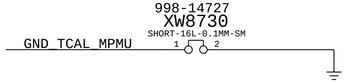
*** PROJECT SPECIFIC ***

BUCK3/BUCK13 OPTION FOR LDO3/8/14/20 VDDIN



ALIAS AMUX NEGATIVE REFERENCE TO GND

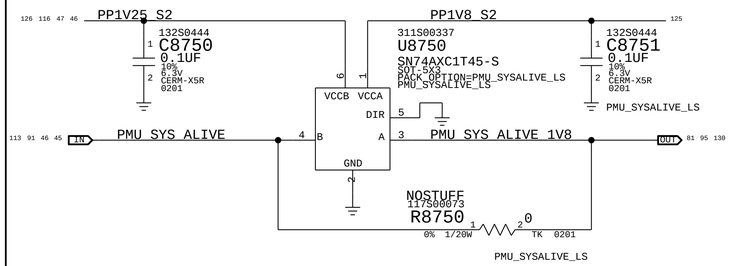
TCAL/TDEV NEGATIVE XW CONNECTION TO GND



ALIAS VREF AND ADC GND

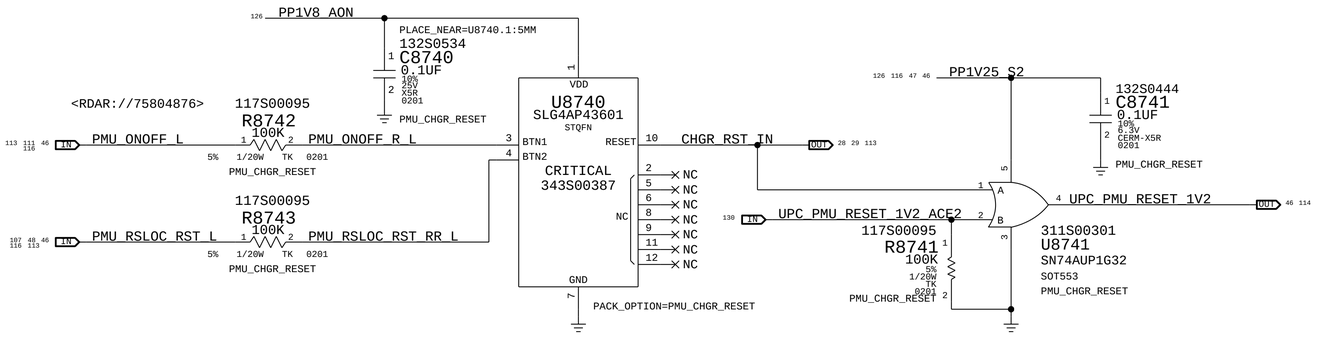
PMU_SYS_ALIVE LEVEL SHIFTER

PACK_OPTION - PMU_SYS_ALIVE_LS
DIR PIN PULLED DOWN, DOUBLE CHECK WHEN ADDING ALT PART
SOME ALTS MIGHT REQUIRE PINS TO BE PULLED UP.



CHARGER RESET CIRCUIT

PACK_OPTION - PMU_CHGR_RESET (PMU NOW TAKES 1.2V)



ANALOG PROBE POINTS

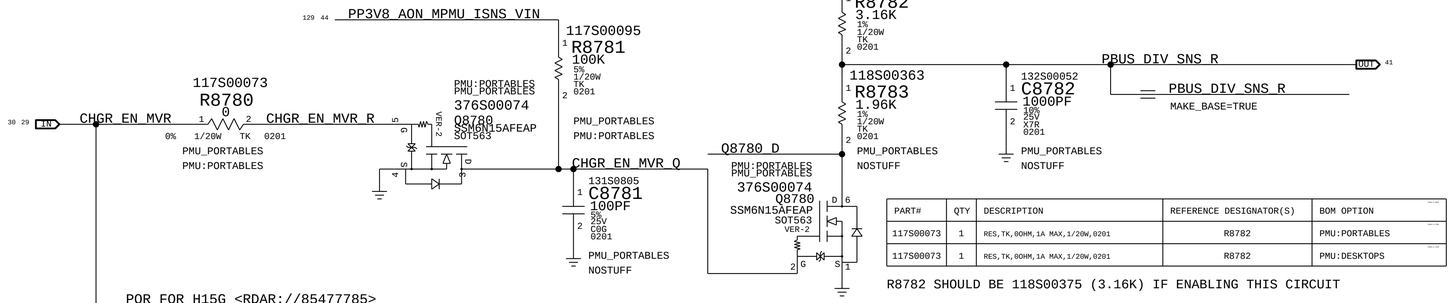
BUCK0_LX0	PP8700	BUCK2_LX0	PP8720	BUCK7_LX0	PP8770	MPMU_BSTLQ_LX	PP87F0
BUCK0_LX1	PP8701	BUCK2_LX1	PP8721	BUCK7_LX1	PP8771	MPMU_AMUX_AY	PP8750
BUCK0_LX2	PP8702	BUCK2_LX2	PP8722	BUCK9_LX0	PP8790	MPMU_AMUX_BY	PP8751
BUCK0_LX3	PP8703	BUCK2_LX3	PP8723	BUCK9_LX1	PP8791		
BUCK0_LX4	PP8704	BUCK2_LX4	PP8724	BUCK11_LX0	PP87B0		
BUCK1_LX0	PP8710	BUCK3_LX	PP8730	BUCK11_LX1	PP87B1		
BUCK1_LX1	PP8711	BUCK4_LX0	PP8740	BUCK13_LX	PP87D0		
BUCK1_LX2	PP8712	BUCK4_LX1	PP8741				
BUCK1_LX3	PP8713	BUCK4_LX2	PP8742				
BUCK1_LX4	PP8714						

SIGNAL PROBE POINTS

PMU_SGPIO_READY_REQ — TP8700 (TP-P5)

EARLY PMU CRASH SIGNAL FROM CHGR_EN_MVR

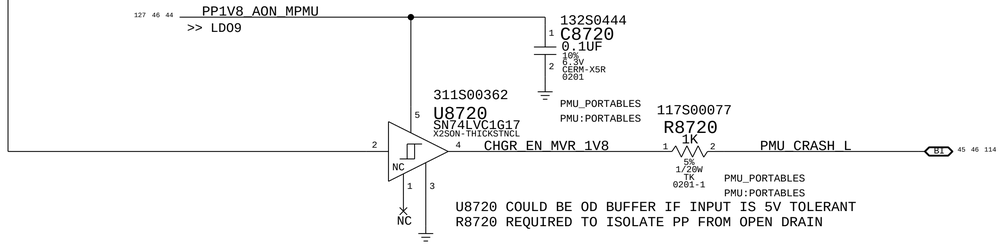
LEGACY FROM H14G (BOOST PULL DOWN CIRCUIT), NOT POR, <RDAR://84737210>
PACK_OPTION - PMU_PORTABLES
BOM_OPTION - PMU:PORTABLES OR PMU:DESKTOPS
R8782 - DESKTOPS WILL NEED TO JUMPER OR ALIAS IN SUPPORT PAGE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S00073	1	RES,TK,0OHM,1A MAX,1/20W,0201	R8782	PMU:PORTABLES
117S00073	1	RES,TK,0OHM,1A MAX,1/20W,0201	R8782	PMU:DESKTOPS

R8782 SHOULD BE 118S00375 (3.16K) IF ENABLING THIS CIRCUIT

POR FOR H15G <RDAR://85477785>
PACK_OPTION - PMU_PORTABLES



U8720 COULD BE OD BUFFER IF INPUT IS 5V TOLERANT
R8720 REQUIRED TO ISOLATE PP FROM OPEN DRAIN

BOM_COST_GROUP=SOC POWER

PAGE TITLE	MPMU: SUPPORT
	Apple Inc.
DRAWING NUMBER	051-07754
SIZE	D
REVISION	6.0.0
BRANCH	dvt-1
PAGE	87 OF 999
SHEET	47 OF 147

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*** PROJECT SPECIFIC ***

ALIAS SPECIFIC TO FF (DIFFER FOR DEV)

45 OUT PMU_RSLOC_RST_L = PMU_RSLOC_RST_L MAKE_BASE=TRUE 46 47 107 113 116
42 NC_MPMU_XIN = NC_MPMU_XIN MAKE_BASE=TRUE NO_TEST=1
45 SOC_WDOG = SOC_WDOG MAKE_BASE=TRUE 6 114
45 SOC_SOCHOT_L = SOC_SOCHOT_L MAKE_BASE=TRUE 6 113
45 PMU_RESET_L = PMU_RESET_L MAKE_BASE=TRUE 6 113 116
45 PMU_ACTIVE_READY = PMU_ACTIVE_READY MAKE_BASE=TRUE 6 69 113
45 DBL_CLICK_DET = DBL_CLICK_DET MAKE_BASE=TRUE 8 114 135
45 SOC_FORCE_DFU = SOC_FORCE_DFU MAKE_BASE=TRUE 6 70 113 116 132

46 45 BUCK0_THERMAL_THROTTLE_L = BUCK0_THERMAL_THROTTLE_L MAKE_BASE=TRUE 8 114 135
46 45 BUCK1_THERMAL_THROTTLE_L = BUCK1_THERMAL_THROTTLE_L MAKE_BASE=TRUE 8 114 135
46 45 TPT_MPMU_THROTTLE2_L = TPT_MPMU_THROTTLE2_L MAKE_BASE=TRUE
46 45 MPMU_VDDHI_UVWARN_L = MPMU_VDDHI_UVWARN_L MAKE_BASE=TRUE 114 135
46 45 MPMU_VDDMAIN_UVWARN_L = MPMU_VDDMAIN_UVWARN_L MAKE_BASE=TRUE 8 36 114 135

VBUS_DET SET AS IPU PER OTP (RDAR://71130901)
ADD BACKUP FOR DEV BUT NC FOR FF.

45 NC_MPMU_VBUS_DET = NC_MPMU_VBUS_DET MAKE_BASE=TRUE NO_TEST=1

45 GND = MAKE_BASE=TRUE

SPMU

40 39 SPMU_VDDMAIN_UVWARN_L = SPMU_VDDMAIN_UVWARN_L MAKE_BASE=TRUE 114 135
39 GND = MAKE_BASE=TRUE

ALIAS SPECIFIC TO FF (DIFFER FOR DEV)

46 NC_P3V3S2_PWR_EN = NC_P3V3S2_PWR_EN MAKE_BASE=TRUE NO_TEST=1

MPMU_XOUT = MPMU_XOUT MAKE_BASE=TRUE 42 44

44 42 PMU_CLK32K_WLBT_R = PMU_CLK32K_WLBT_R MAKE_BASE=TRUE

BOM_COST_GROUP=SOC POWER

PAGE TITLE: PMU PROJECT SUPPORT

Apple Inc.

DRAWING NUMBER: 051-07754 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
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* OK2INTEGRATE *

5V_S2 Voltage Regulator (low power option)

SET ONE OPTION FOR PBUS CAPS

PACK_OPTION=5VS2TPS_PBUS-B12
PACK_OPTION=5VS2TPS_PBUS-D2
PACK_OPTION=5VS2TPS_PBUS-D12
PACK_OPTION=5VS2TPS_PBUS-18V

SET ONE OPTION FOR OUTPUT VOLTAGE

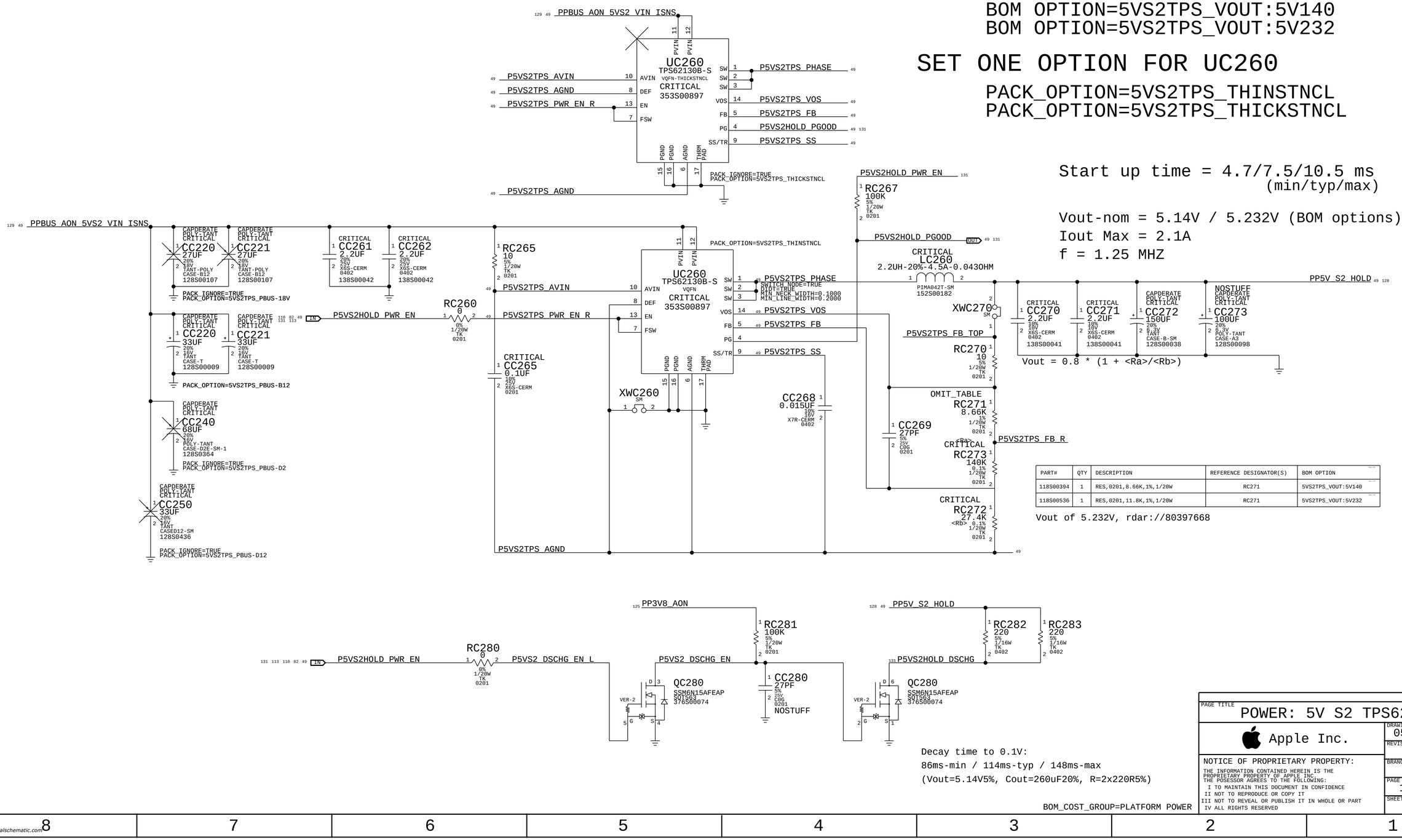
BOM OPTION=5VS2TPS_VOUT:5V140
BOM OPTION=5VS2TPS_VOUT:5V232

SET ONE OPTION FOR UC260

PACK_OPTION=5VS2TPS_THINSTNCL
PACK_OPTION=5VS2TPS_THICKSTNCL

Start up time = 4.7/7.5/10.5 ms (min/typ/max)

Vout-nom = 5.14V / 5.232V (BOM options)
Iout Max = 2.1A
f = 1.25 MHZ



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S00394	1	RES,0201,8.66K,1%,1/20W	RC271	5VS2TPS_VOUT:5V140
118S00536	1	RES,0201,11.8K,1%,1/20W	RC271	5VS2TPS_VOUT:5V232

Vout of 5.232V, rdar://80397668

Decay time to 0.1V:
86ms-min / 114ms-typ / 148ms-max
(Vout=5.14V5%, Cout=260uF20%, R=2x220R5%)

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: POWER: 5V S2 TPS62130

Apple Inc.

DRAWING NUMBER: 051-07754
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
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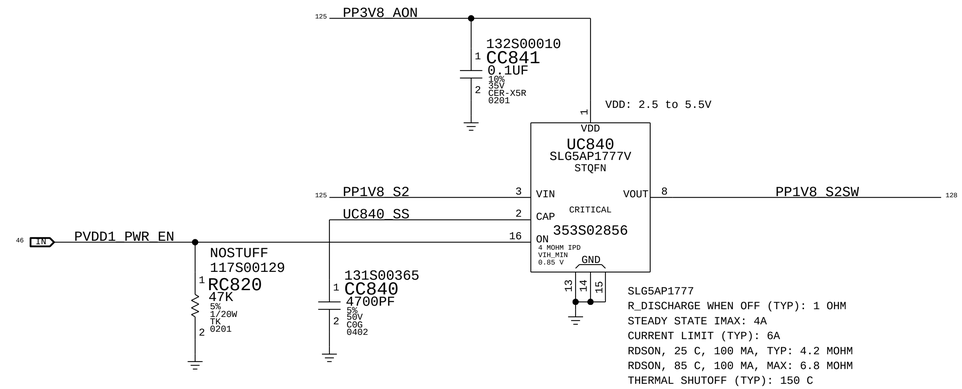
VDD1 1V8 SWITCH

<RDAR://82948742>



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
POWER: EXTERNAL SWITCHES

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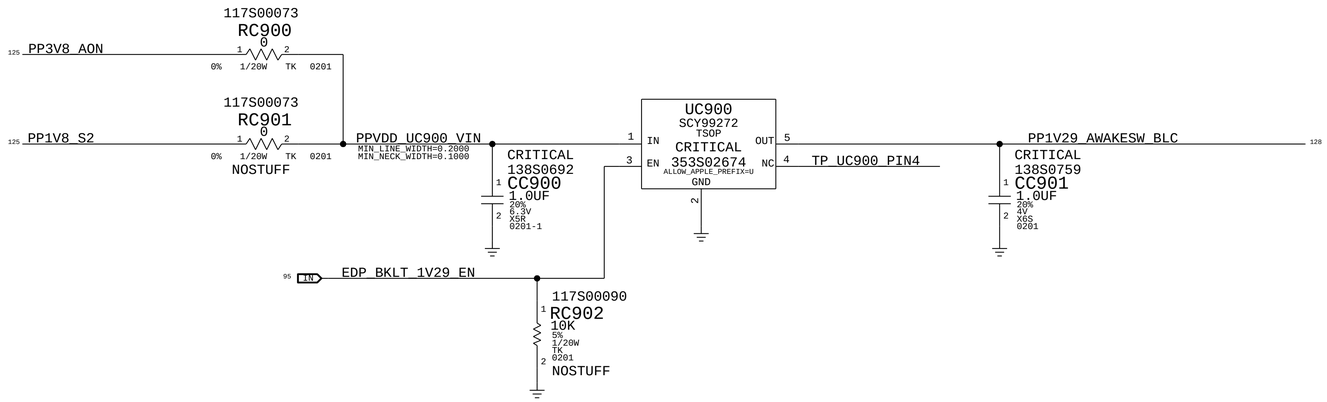
1.29V LDO FOR ATRANI VDDHOST
VDDHOST(MIN) IS 1.11V SO DISPLAY TEAM REQUESTS A HIGHER NOMINAL VOLTAGE



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: POWER: EXTERNAL LDOS

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SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
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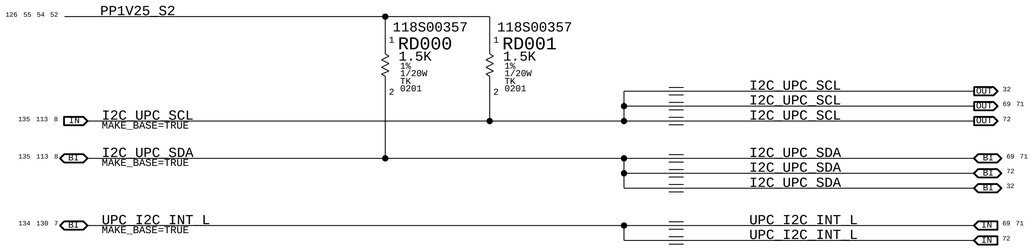
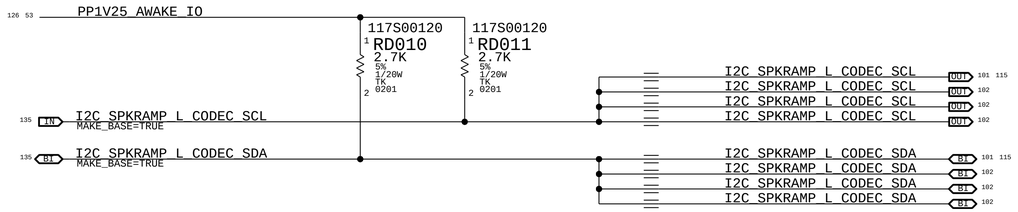
AP_I2C0

DEVICE	DIAGS BUS	7B	8B WR
UPC 0	0	0X38	0X70
UPC 1		0X3F	0X7E
UPC 5		0X3A	0X74
ALL CALL		0X6B	0XD6



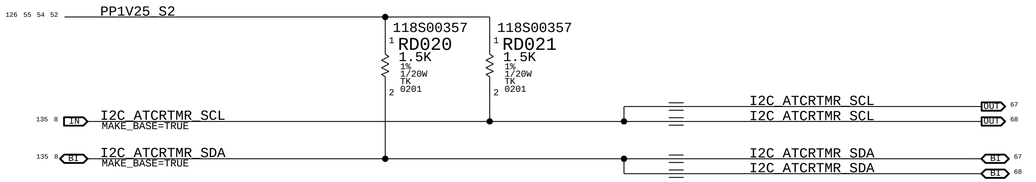
AP_I2C1

DEVICE	DIAGS BUS	7B	8B WR
SPKRAMP TAWANG A	1	0X38	0X70
SPKRAMP TAWANG B		0X39	0X72
SPKRAMP TAWANG C		0X3A	0X74
CODEC CARLOW		0X4B	0X96



AP_I2C2

DEVICE	DIAGS BUS	7B	8B WR
RT13 0	2	0X18	0X30
RT13 1		0X19	0X32



BOM_COST_GROUP=SOC

PAGE TITLE
SOC I2C: AP (1/2)

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DRAWING NUMBER 051-07754
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REVISION 6.0.0
BRANCH dvt-1
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AP_I2C3

DEVICE	DIAGS BUS	7B	8B WR
SPKRAMP TAWANG D	3	0X3B	0X76
SPKRAMP TAWANG E		0X3C	0X78
SPKRAMP TAWANG F		0X3D	0X7A
HDMI		0X08	0X10

<RDAR://85531475> HDMI I2C OK TO PU TO SYSTEM RAIL

126 53 52 PP1V25_AWAKE_IO

117S00120 RD100 2.7K 5% 1/20W TK 0201

117S00120 RD101 2.7K 5% 1/20W TK 0201

135 130 117 IN I2C_HDMI_SPKRAMP_R_SCL
MAKE_BASE=TRUE

135 130 117 BI I2C_HDMI_SPKRAMP_R_SDA
MAKE_BASE=TRUE

I2C_HDMI_SPKRAMP_R_SCL OUT 103 115
I2C_HDMI_SPKRAMP_R_SCL OUT 103
I2C_HDMI_SPKRAMP_R_SCL OUT 103

I2C_HDMI_SPKRAMP_R_SDA BI 103 115
I2C_HDMI_SPKRAMP_R_SDA BI 103
I2C_HDMI_SPKRAMP_R_SDA BI 103

AP_I2C4

DEVICE	DIAGS BUS	7B	8B WR
AVELLINO PMIC	4	0X44	0X88
LUXE		?	?
GL9755A SD CARD		0X20	0X40

126 53 52 PP1V25_AWAKE_IO

(SOC MASTER, 1.2V)

135 8 IN I2C_SD_DISP_BKLT_SCL
CKPLUS_WAIVE=I2C_PULLUP

135 8 BI I2C_SD_DISP_BKLT_SDA
CKPLUS_WAIVE=I2C_PULLUP

117S00073 RD110 0 0% 1/20W TK 0201
PLACE_NEAR=RD111.2:5MM

117S00073 RD111 0 0% 1/20W TK 0201
PLACE_NEAR=RD112.2:5MM

I2C_SD_DISP_BKLT_SCL_R

I2C_SD_DISP_BKLT_SDA_R

117S00087 RD112 4.7K 5% 1/20W TK 0201
PLACE_NEAR=RD113.2:5MM

117S00087 RD113 4.7K 5% 1/20W TK 0201
PLACE_NEAR=RD114.1:5MM

NOTE: THE LAYOUT
INTENT FOR ALL THESE
RESISTORS IS A CENTRALLY
LOCATED STAR TOPOLOGY.
BUT IT'S ALL DEBUG
SO NOT CRITICAL

NOSTUFF 117S00073 RD114 0 0% 1/20W TK 0201
PLACE_NEAR=RD113.2:5MM

NOSTUFF 117S00073 RD115 0 0% 1/20W TK 0201
PLACE_NEAR=RD114.1:5MM

(LUXE, 1.2V)

I2C_LUXE_DEBUG_SCL OUT 96 115

I2C_LUXE_DEBUG_SDA BI 96 115

126 53 52 PP1V25_AWAKE_IO

117S00073 RD116 0 0% 1/20W TK 0201
PLACE_NEAR=RD113.2:5MM

117S00073 RD117 0 0% 1/20W TK 0201
PLACE_NEAR=RD116.1:5MM

CD110 0.1UF 10% 16V X5R-CERM 0201

CKPLUS_WAIVE=I2C_PULLUP
I2C_LUXE_1V2_SCL

CKPLUS_WAIVE=I2C_PULLUP
I2C_LUXE_1V2_SDA

CRITICAL
UD110 LSF0101-I2C SON OPT-2
VBIAS
SCLB SCLA
SDAB SDAA
311S00244 GND

125 54 PP1V8_S2

(AVELLINO, 1.8V)

I2C_BKLT_1V8_SCL

I2C_BKLT_1V8_SDA

117S00120 RD120 2.7K 5% 1/20W TK 0201

117S00120 RD121 2.7K 5% 1/20W TK 0201

I2C_BKLT_1V8_SCL OUT 97 113

I2C_BKLT_1V8_SDA BI 97 113

117S00073 RD118 0 0% 1/20W TK 0201
PLACE_NEAR=RD113.2:5MM

117S00073 RD119 0 0% 1/20W TK 0201
PLACE_NEAR=RD118.1:5MM

(GL9755A, LS AT REF DESIGN)

MAKE_BASE=TRUE
I2C_SD_DEBUG_SCL 115
I2C_SD_DEBUG_SCL OUT 85

I2C_SD_DEBUG_SDA BI 85
I2C_SD_DEBUG_SDA 115
MAKE_BASE=TRUE

BOM_COST_GROUP=SOC

PAGE TITLE: SOC I2C: AP (2/2)

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DRAWING NUMBER: 051-07754 SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
PAGE: 131 OF 999
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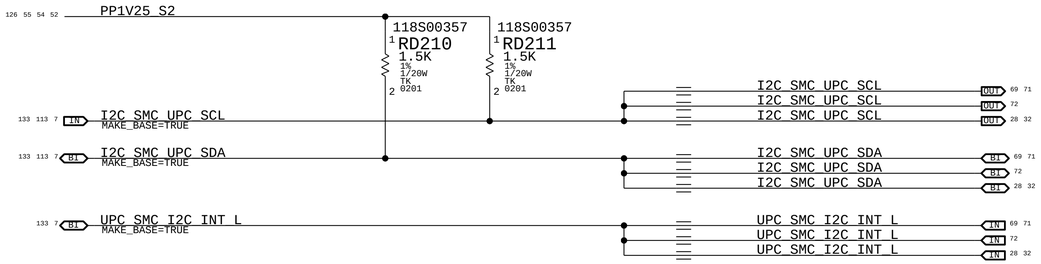
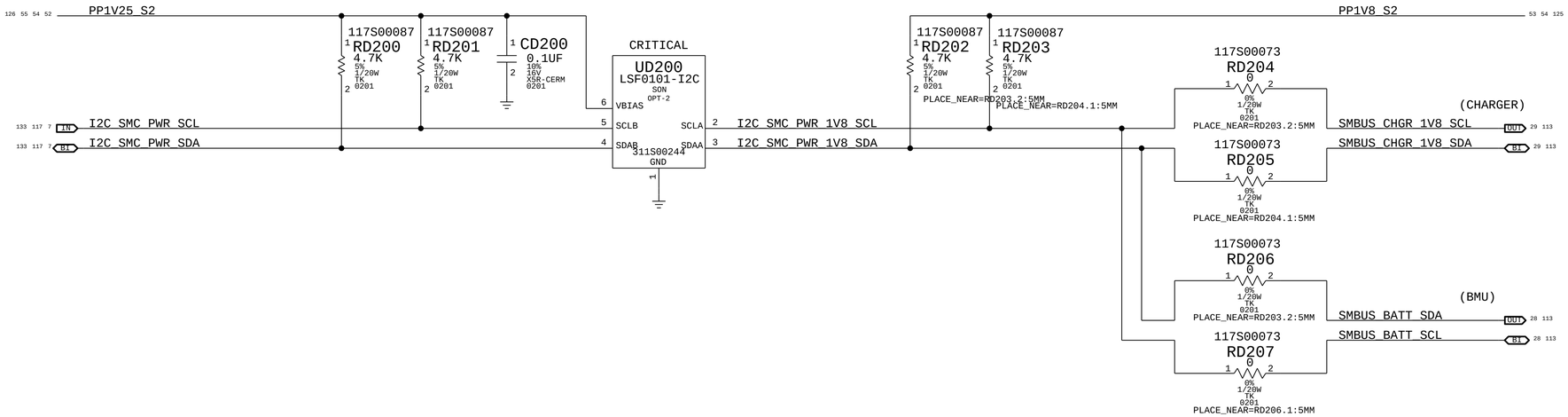
SMC_I2C0

DEVICE	DIAGS BUS	7B	8B WR
UPC 0	9	0x38	0x70
UPC 1		0x3F	0x7E
UPC 5		0x3A	0x74
ALL CALL		0X6B	0XD6



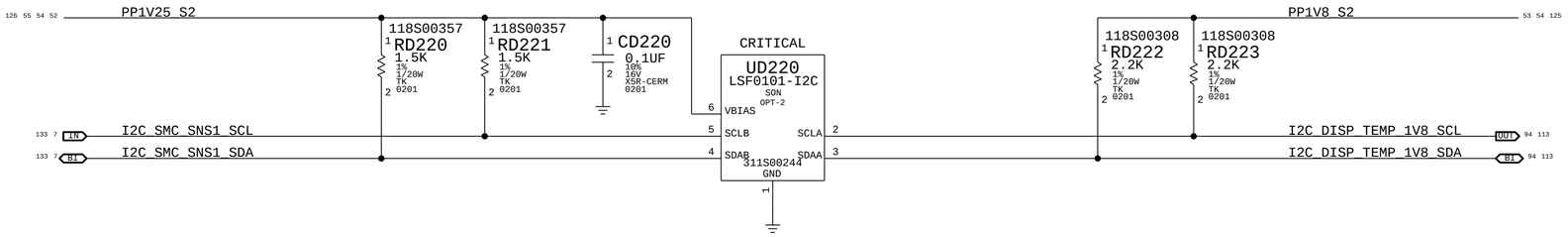
SMC_I2C1

DEVICE	DIAGS BUS	7B	8B WR
CHARGER WHAMOLA	10	0x09	0x12
BMU		0x0B	0x16
IOEXPANDER (W)		0X20	0X40
IOEXPANDER (R)			0X41



SMC_I2C2

DEVICE	DIAGS BUS	7B	8B WR
DISPLAY TEMP SENSOR	11	0X48	0X90



BOM_COST_GROUP=SOC

PAGE TITLE: SOC I2C: SMC (1/2)

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REVISION: 6.0.0

BRANCH: dvt-1

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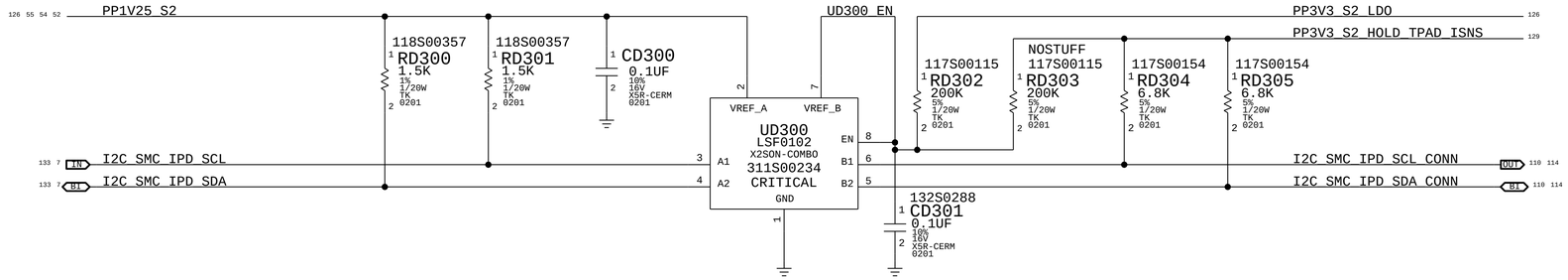
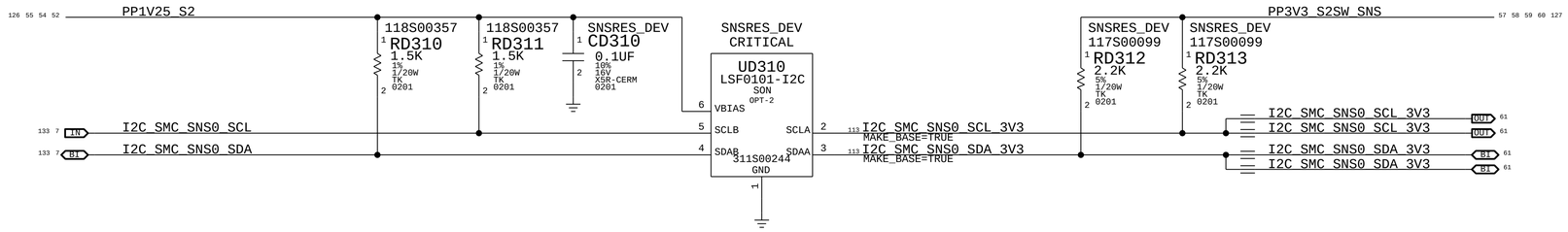
SMC_I2C3

DEVICE	DIAGS BUS	7B	8B WR
PALM REST TEMP	12	0x4C	0x98



SMC_I2C4

DEVICE	DIAGS BUS	7B	8B WR
DEV ADC 1	13	0X17	0X2E
DEV ADC 2		0X10	0X20



BOM_COST_GROUP=SOC

PAGE TITLE
SOC I2C: SMC (2/2)

Apple Inc.

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REVISION 6.0.0
BRANCH dvt-1
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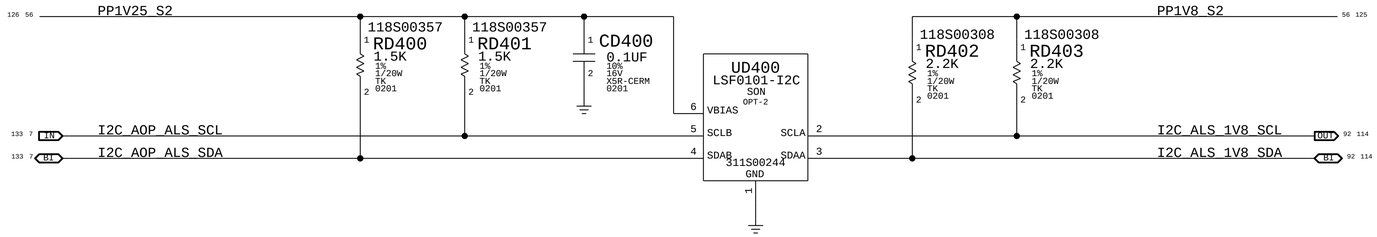
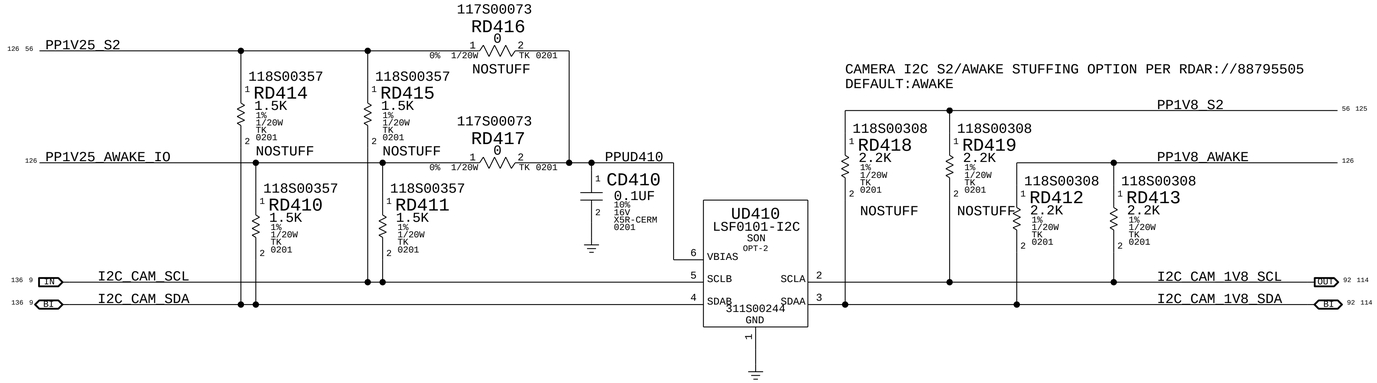
AOP_I2C0

DEVICE	DIAGS BUS	7B	8B WR
ALS	5	0x29	0X52
ALS TEMP SENSOR		0x48	0X90



ISP_I2C0

DEVICE	DIAGS BUS	7B	8B WR
CAMERA PMIC FHSI+	NONE	0x10	0x20
CAMERA SENSOR FARGO		0x6C	0xD8



SI2C0

DEVICE	DIAGS BUS	7B	8B WR
STOCT	NONE	0X71	0XE2

PUS ON THE REF DESIGN PAGE

BOM_COST_GROUP=SOC

PAGE TITLE
SOC I2C: AOP, ISP, SEP

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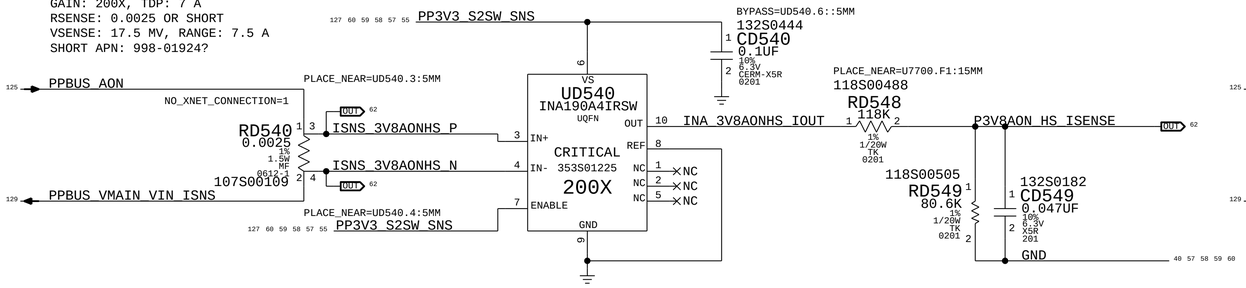
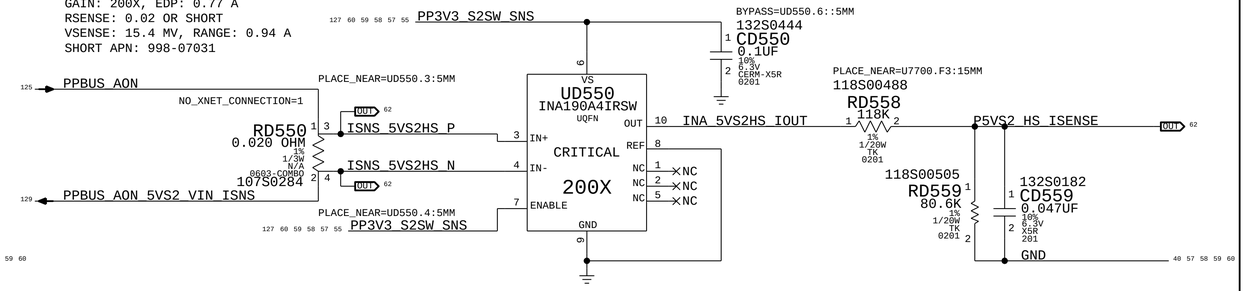
P3V8 AON HIGH SIDE CURRENT SENSE (IMVR)

GAIN: 200X, TDP: 7 A
RSENSE: 0.0025 OR SHORT
VSENSE: 17.5 MV, RANGE: 7.5 A
SHORT APN: 998-01924?



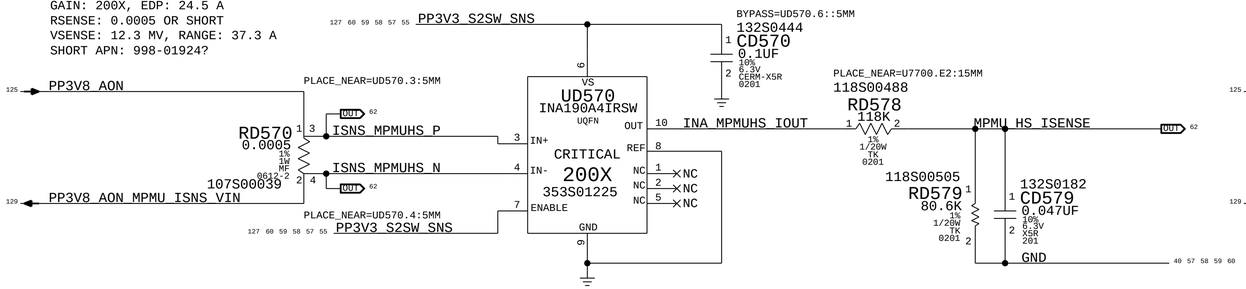
5V S2 VR HIGH SIDE CURRENT SENSE (IO5R)

GAIN: 200X, EDP: 0.77 A
RSENSE: 0.02 OR SHORT
VSENSE: 15.4 MV, RANGE: 0.94 A
SHORT APN: 998-07031



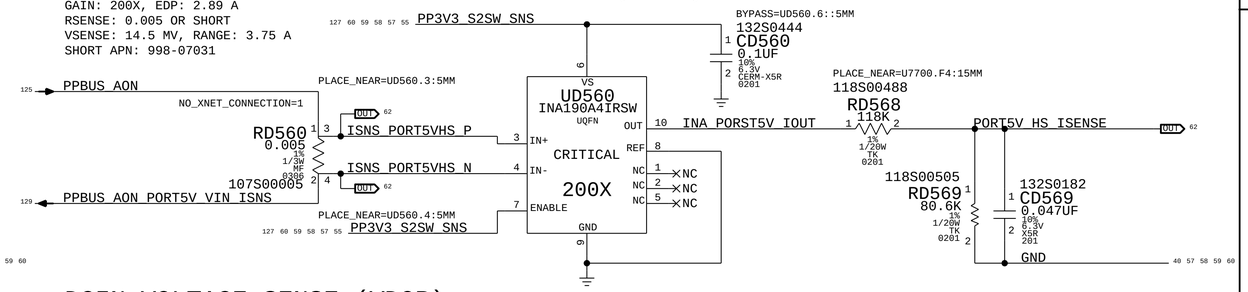
MAIN PMU HIGH SIDE CURRENT SENSE (IPMR)

GAIN: 200X, EDP: 24.5 A
RSENSE: 0.0005 OR SHORT
VSENSE: 12.3 MV, RANGE: 37.3 A
SHORT APN: 998-01924?



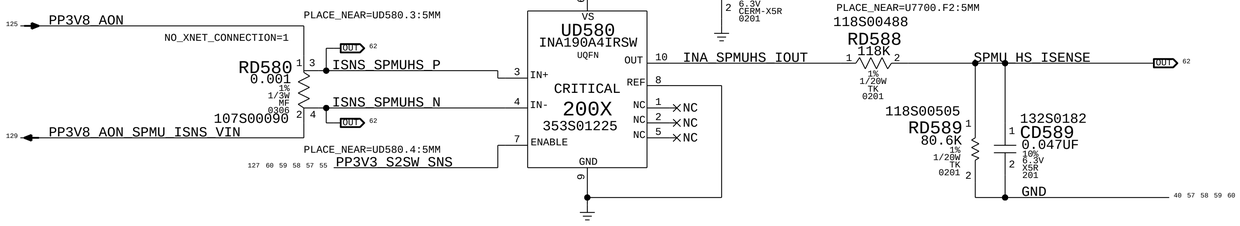
USB PORT 5V HIGH SIDE CURRENT SENSE (IU5R)

GAIN: 200X, EDP: 2.89 A
RSENSE: 0.005 OR SHORT
VSENSE: 14.5 MV, RANGE: 3.75 A
SHORT APN: 998-07031



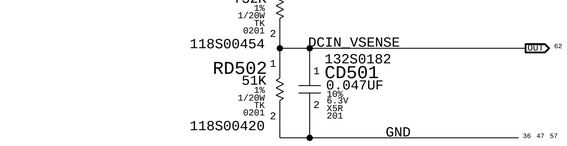
SECONDARY PMU HIGH SIDE CURRENT SENSE (IPSR)

GAIN: 200X, EDP: 9.92 A
RSENSE: 0.001 OR SHORT
VSENSE: 9.9 MV, RANGE: 18.7 A
SHORT APN: 998-07031

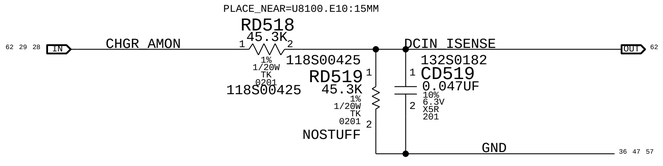


DCIN VOLTAGE SENSE (VD0R)

PMU AMUX inputs are not fail safe but RD501 limits the current rdar://60591705

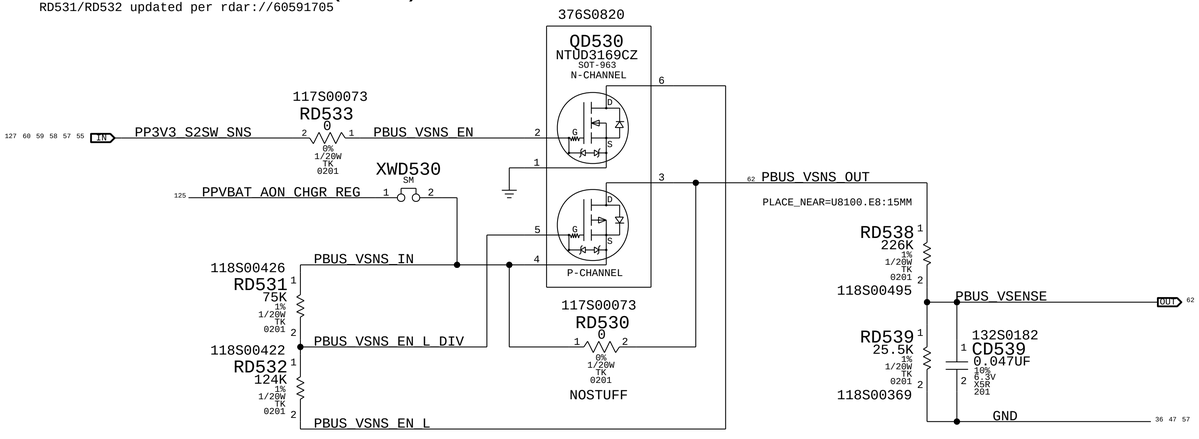


DCIN CURRENT SENSE [AMON] (ID0R)

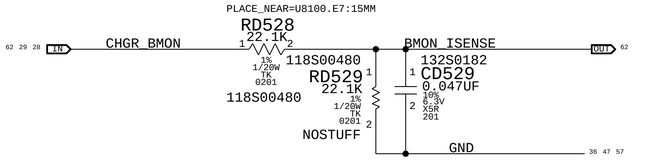


PBUS VOLTAGE SENSE (VP0R)

RD531/RD532 updated per rdar://60591705



BATTERY CHARGER CURRENT SENSE [BMON] (IPBR)



BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: POWER HIGH SIDE

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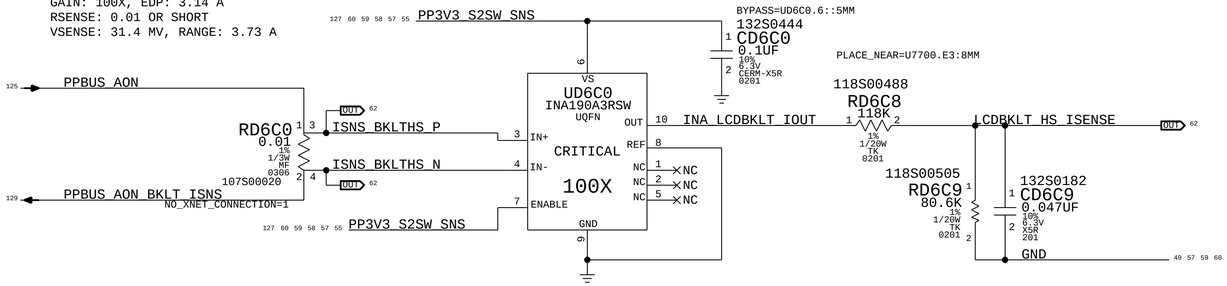
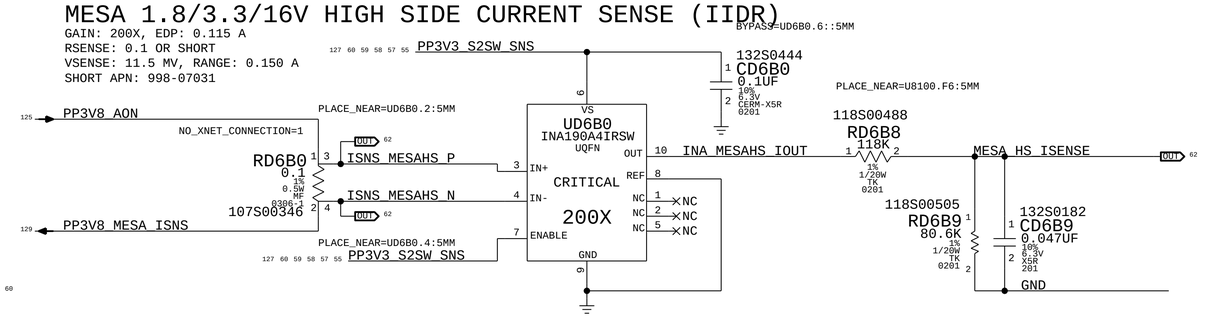
LCD BACKLIGHT HIGH SIDE CURRENT SENSE (IBLR)

GAIN: 100X, EDP: 3.14 A
RSENSE: 0.01 OR SHORT
VSENSE: 31.4 MV, RANGE: 3.73 A



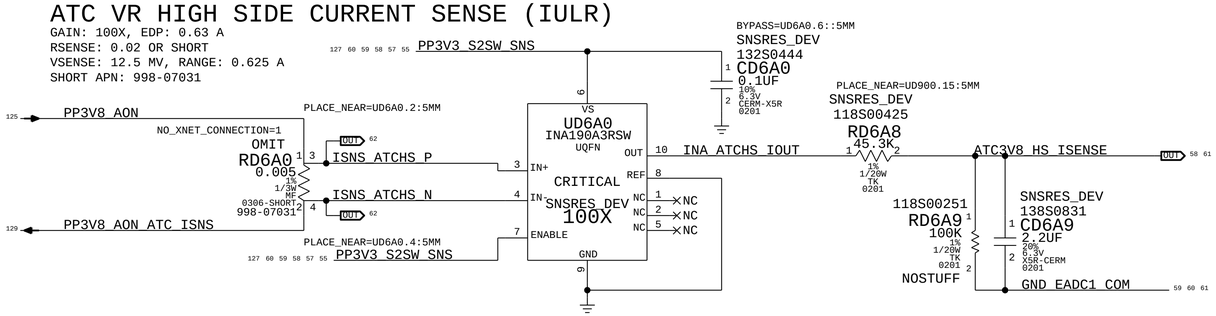
MESA 1.8/3.3/16V HIGH SIDE CURRENT SENSE (IIDR)

GAIN: 200X, EDP: 0.115 A
RSENSE: 0.1 OR SHORT
VSENSE: 11.5 MV, RANGE: 0.150 A
SHORT APN: 998-07031



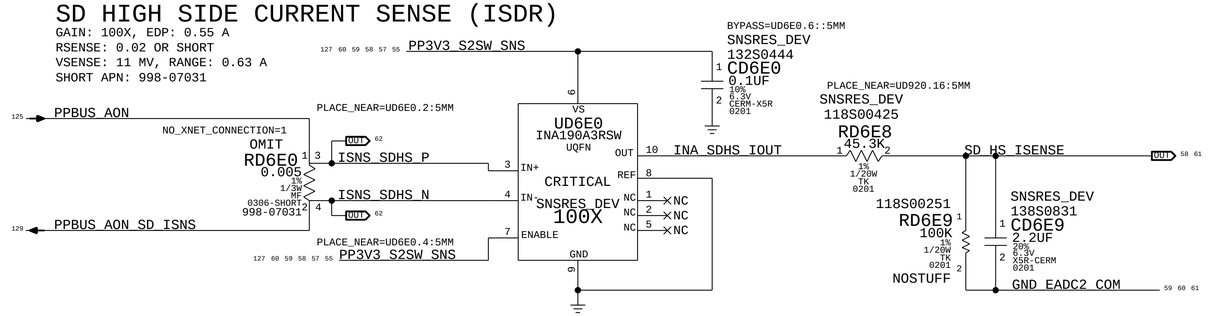
ATC VR HIGH SIDE CURRENT SENSE (IULR)

GAIN: 100X, EDP: 0.63 A
RSENSE: 0.02 OR SHORT
VSENSE: 12.5 MV, RANGE: 0.625 A
SHORT APN: 998-07031



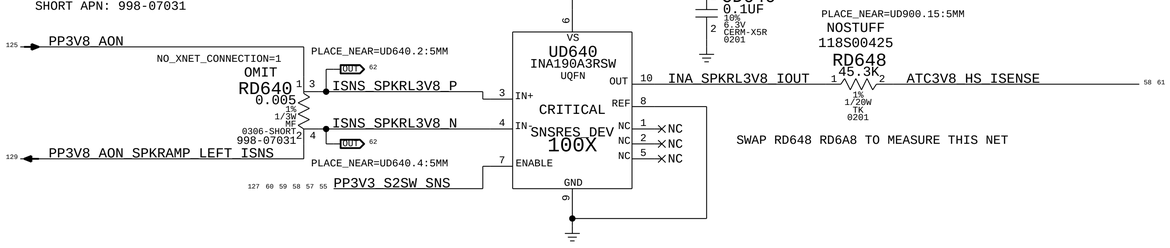
SD HIGH SIDE CURRENT SENSE (ISDR)

GAIN: 100X, EDP: 0.55 A
RSENSE: 0.02 OR SHORT
VSENSE: 11 MV, RANGE: 0.63 A
SHORT APN: 998-07031



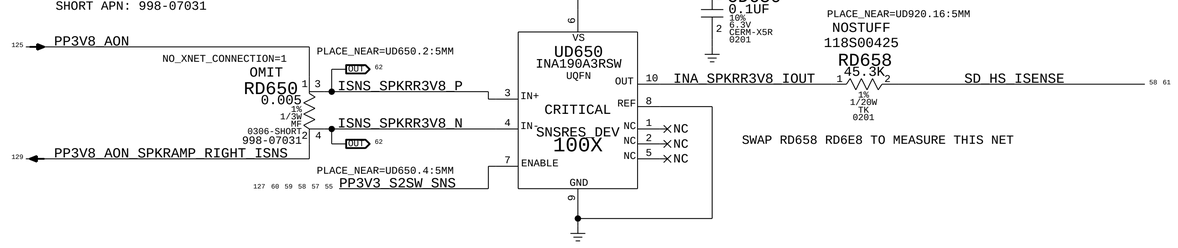
LEFT SPEAKER 3.8V CURRENT SENSE (N/A)

GAIN: 100X, EDP: 0.55 A
RSENSE: 0.02 OR SHORT
VSENSE: 11 MV, RANGE: 0.63 A
SHORT APN: 998-07031



RIGHT SPEAKER 3.8V CURRENT SENSE (N/A)

GAIN: 100X, EDP: 0.55 A
RSENSE: 0.02 OR SHORT
VSENSE: 11 MV, RANGE: 0.63 A
SHORT APN: 998-07031



BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: POWER LOAD SIDE (1/3)

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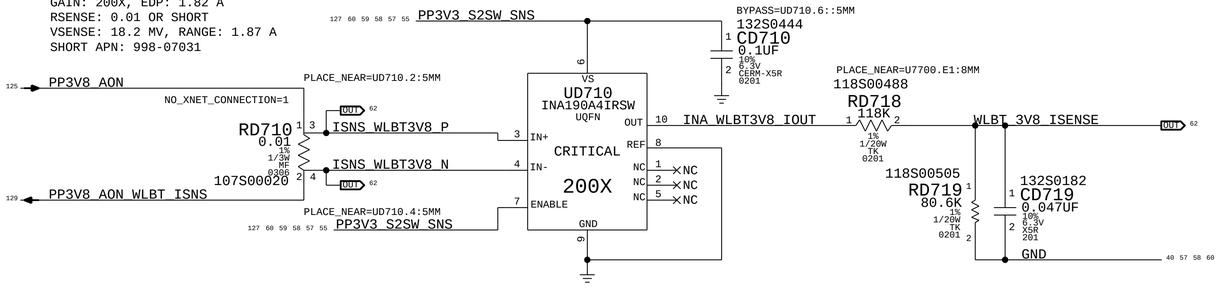
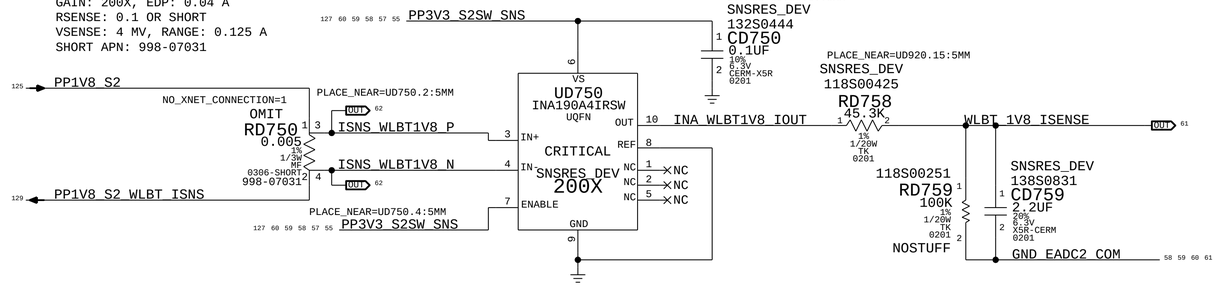
WLAN BT 3V8 CURRENT SENSE (IW3C)

GAIN: 200X, EDP: 1.82 A
RSENSE: 0.01 OR SHORT
VSENSE: 18.2 MV, RANGE: 1.87 A
SHORT APN: 998-07031



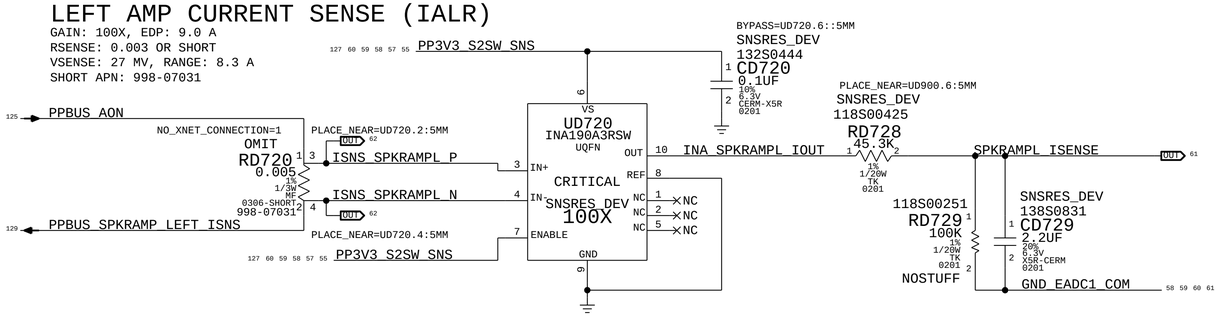
WLAN BT 1V8 S2 CURRENT SENSE (IW2C)

GAIN: 200X, EDP: 0.04 A
RSENSE: 0.1 OR SHORT
VSENSE: 4 MV, RANGE: 0.125 A
SHORT APN: 998-07031



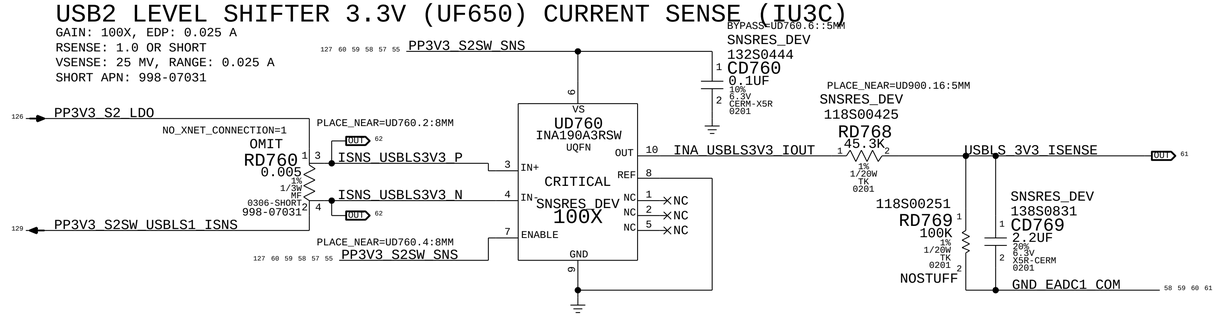
LEFT AMP CURRENT SENSE (IALR)

GAIN: 100X, EDP: 9.0 A
RSENSE: 0.003 OR SHORT
VSENSE: 27 MV, RANGE: 8.3 A
SHORT APN: 998-07031



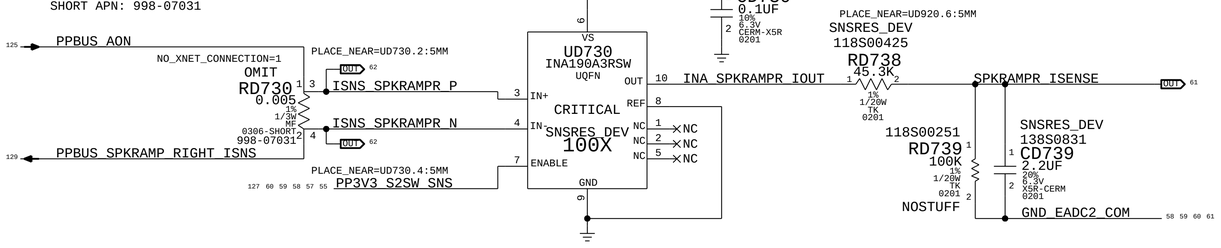
USB2 LEVEL SHIFTER 3.3V (UF650) CURRENT SENSE (IU3C)

GAIN: 100X, EDP: 0.025 A
RSENSE: 1.0 OR SHORT
VSENSE: 25 MV, RANGE: 0.025 A
SHORT APN: 998-07031



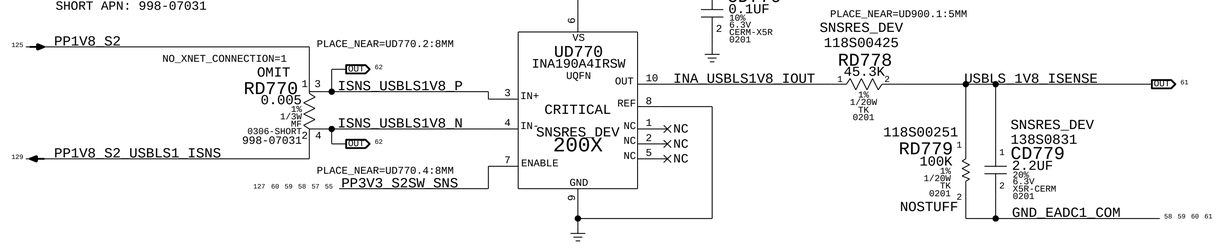
RIGHT AMP CURRENT SENSE (IARR)

GAIN: 100X, EDP: 9.0 A
RSENSE: 0.003 OR SHORT
VSENSE: 27 MV, RANGE: 8.3 A
SHORT APN: 998-07031



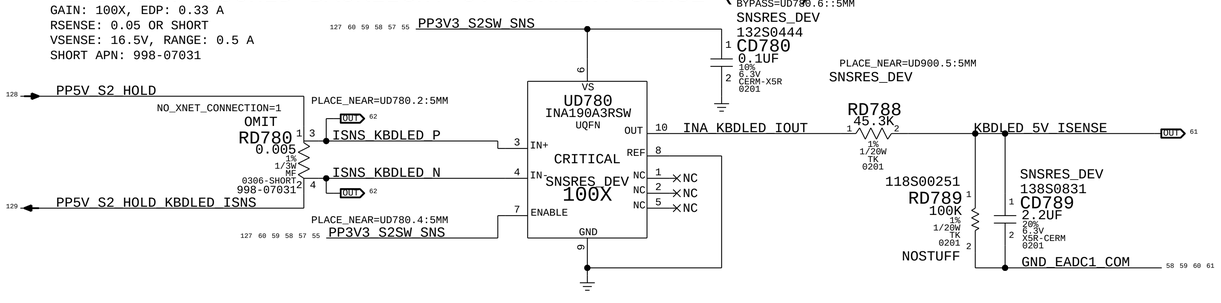
USB2 LEVEL SHIFTER 1.8V (UF650) CURRENT SENSE (IU2C)

GAIN: 200X, EDP: 0.34 A
RSENSE: 0.035 OR SHORT
VSENSE: 11.9 MV, RANGE: 0.36 A
SHORT APN: 998-07031



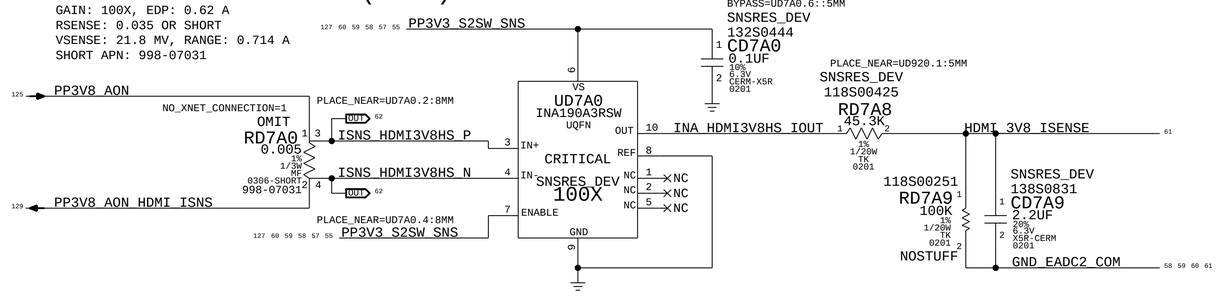
KEYBOARD/TOUCHID BACKLIGHT 5V CURRENT SENSE (IKBC)

GAIN: 100X, EDP: 0.33 A
RSENSE: 0.05 OR SHORT
VSENSE: 16.5V, RANGE: 0.5 A
SHORT APN: 998-07031



HDMI 3.8V HIGH SIDE (IDHC)

GAIN: 100X, EDP: 0.62 A
RSENSE: 0.035 OR SHORT
VSENSE: 21.8 MV, RANGE: 0.714 A
SHORT APN: 998-07031



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PAGE TITLE
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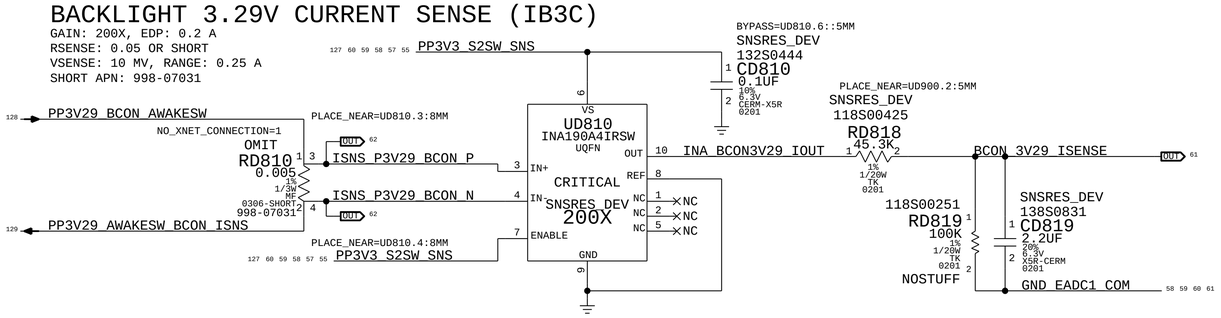
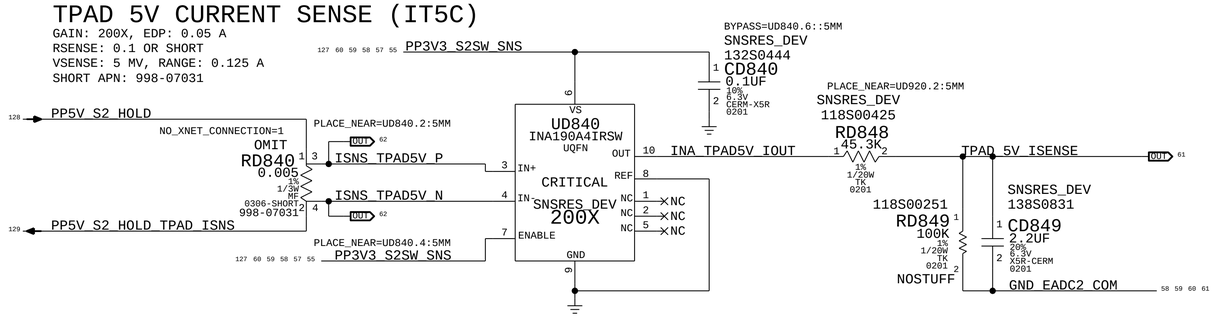
BACKLIGHT 3.29V CURRENT SENSE (IB3C)

GAIN: 200X, EDP: 0.2 A
RSENSE: 0.05 OR SHORT
VSENSE: 10 MV, RANGE: 0.25 A
SHORT APN: 998-07031



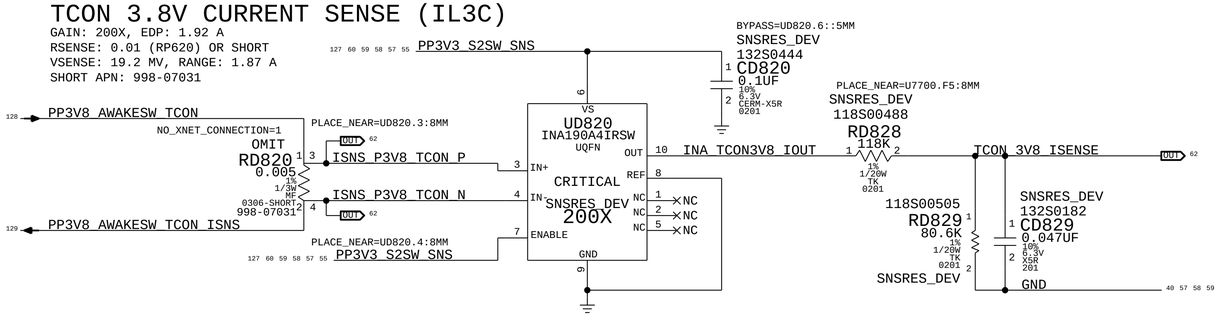
TPAD 5V CURRENT SENSE (IT5C)

GAIN: 200X, EDP: 0.05 A
RSENSE: 0.1 OR SHORT
VSENSE: 5 MV, RANGE: 0.125 A
SHORT APN: 998-07031



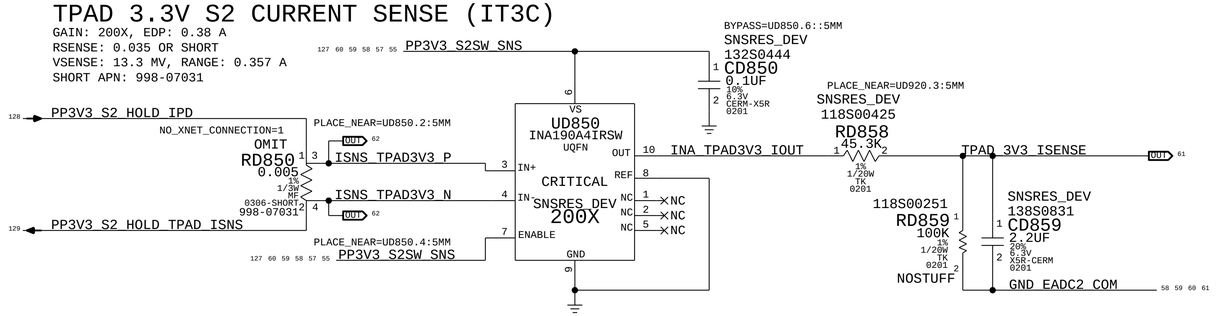
TCON 3.8V CURRENT SENSE (IL3C)

GAIN: 200X, EDP: 1.92 A
RSENSE: 0.01 (RP620) OR SHORT
VSENSE: 19.2 MV, RANGE: 1.87 A
SHORT APN: 998-07031



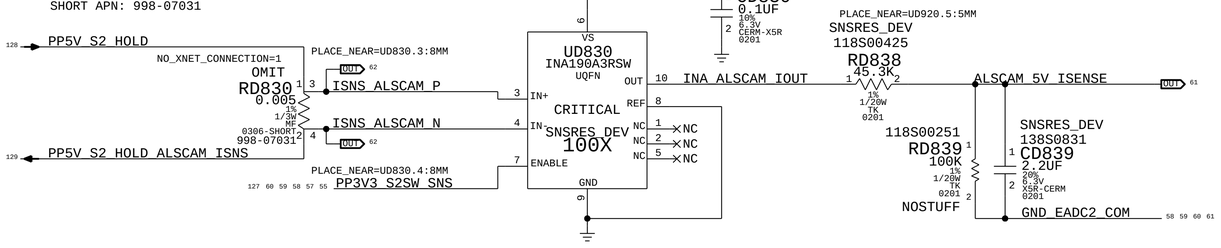
TPAD 3.3V S2 CURRENT SENSE (IT3C)

GAIN: 200X, EDP: 0.38 A
RSENSE: 0.035 OR SHORT
VSENSE: 13.3 MV, RANGE: 0.357 A
SHORT APN: 998-07031



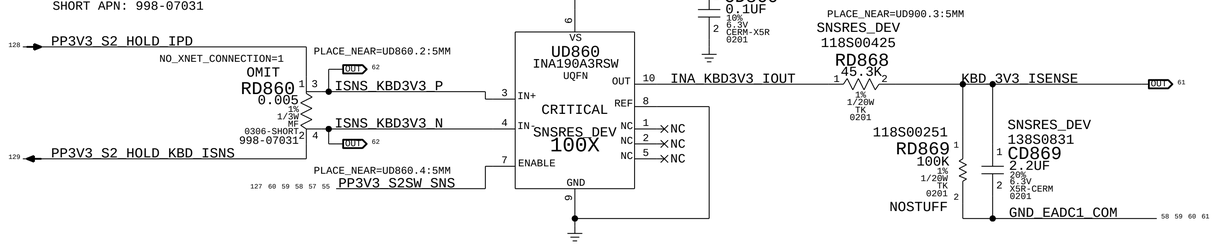
ALSCAM 5V CURRENT SENSE (ICMC)

GAIN: 100X, EDP: 0.166 A
RSENSE: 0.1 OR SHORT
VSENSE: 16.6 MV, RANGE: 0.25 A
SHORT APN: 998-07031



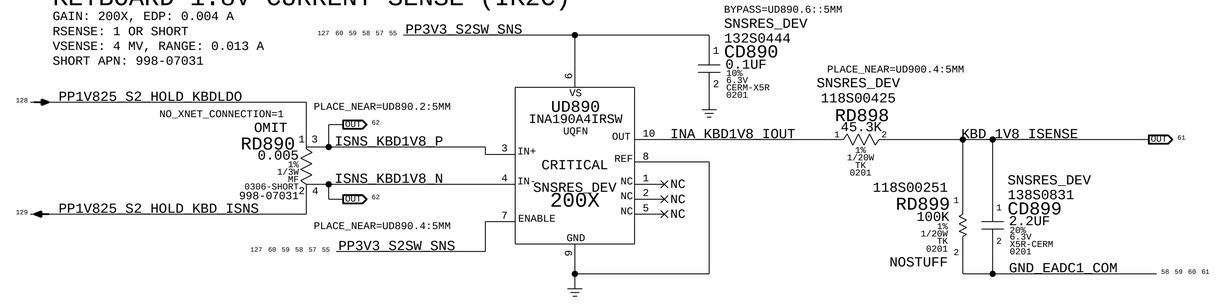
KBD 3.3V S2 CURRENT SENSE (IK3C)

GAIN: 100X, EDP: 0.02 A
RSENSE: 1.0 OR SHORT
VSENSE: 20 MV, RANGE: 0.025 A
SHORT APN: 998-07031



KEYBOARD 1.8V CURRENT SENSE (IK2C)

GAIN: 200X, EDP: 0.004 A
RSENSE: 1 OR SHORT
VSENSE: 4 MV, RANGE: 0.013 A
SHORT APN: 998-07031



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PAGE TITLE
SENSORS: POWER LOAD SIDE (3/3)

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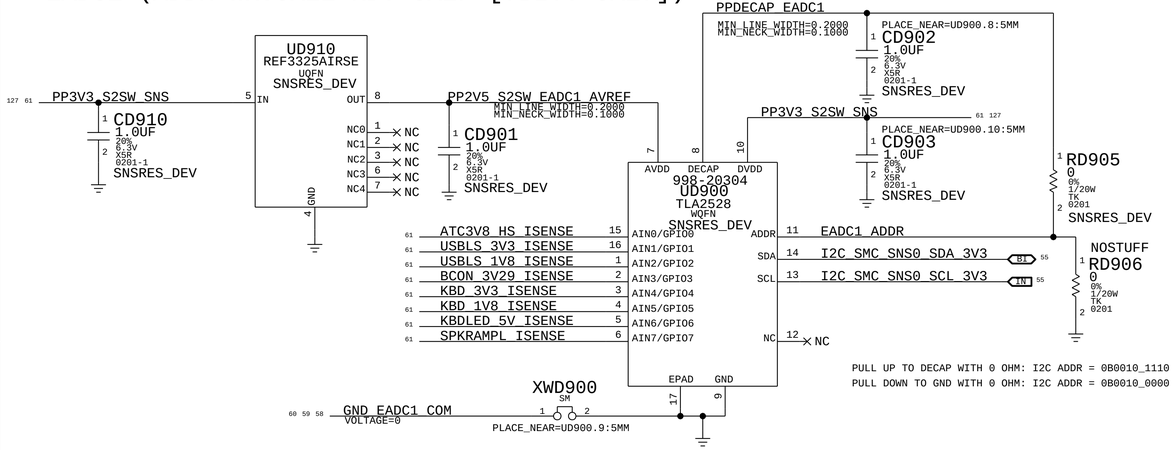
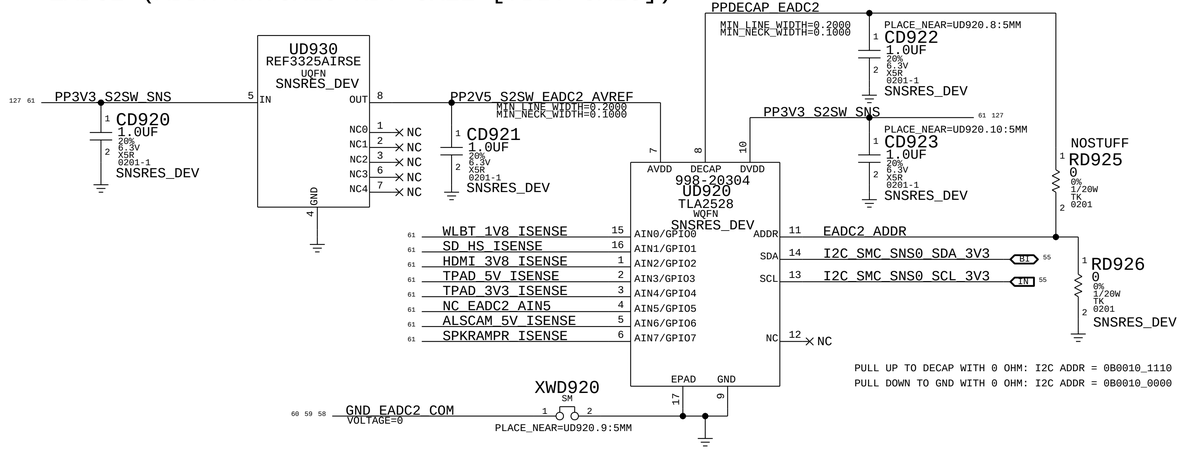
EADC1 (ADDR WR:0X2E RD: 0X2F [7BIT: 0X17])



EADC2 (ADDR WR:0X20 RD: 0X21 [7BIT 0X10])



EADC1 AIN ALIAS

ATC3V8_HS_ISENSE = ATC3V8_HS_ISENSE
USBLS_3V3_ISENSE = USBLS_3V3_ISENSE
USBLS_1V8_ISENSE = USBLS_1V8_ISENSE
BCON_3V29_ISENSE = BCON_3V29_ISENSE
KBD_3V3_ISENSE = KBD_3V3_ISENSE
KBD_1V8_ISENSE = KBD_1V8_ISENSE
KBDLED_5V_ISENSE = KBDLED_5V_ISENSE
SPKRAMPL_ISENSE = SPKRAMPL_ISENSE

(MAKE_BASE=TRUE, NO_TEST=1)

EADC2 AIN ALIAS

WLBT_1V8_ISENSE = WLBT_1V8_ISENSE
SD_HS_ISENSE = SD_HS_ISENSE
HDMI_3V8_ISENSE = HDMI_3V8_ISENSE
TPAD_5V_ISENSE = TPAD_5V_ISENSE
TPAD_3V3_ISENSE = TPAD_3V3_ISENSE
NC_EADC2_AIN5 = NC_EADC2_AIN5
ALSCAM_5V_ISENSE = ALSCAM_5V_ISENSE
SPKRAMPR_ISENSE = SPKRAMPR_ISENSE

(MAKE_BASE=TRUE, NO_TEST=1)

BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: EADC

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DRAWING NUMBER: 051-07754
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REVISION: 6.0.0
BRANCH: dvt-1
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SOC SENSE LINES

PPE0A1	VDD_PCPU_SENSE	17	1	NO_TEST=1
PPE0A2	VSS_PCPU_SENSE	17	1	NO_TEST=1
PPE0A3	VDD_PCPU_ABSMIN	17	1	NO_TEST=1
PPE0A4	VDD_ECPU_SENSE	18	1	NO_TEST=1
PPE0A5	VSS_GPU_SENSE	21	1	NO_TEST=1
PPE0A6	VDD_SOC_SENSE	18	1	NO_TEST=1
PPE0A7	VDD_DISP_S1_SENSE	20	1	NO_TEST=1
PPE0A8	VDD2H_SENSE_1	21	1	NO_TEST=1
PPE0A9	VSS_SENSE_1	21	1	NO_TEST=1
PPE0AA	VDD2H_SENSE_2	21	1	NO_TEST=1
PPE0AB	VSS_SENSE_2	21	1	NO_TEST=1
PPE0AE	VSS_DDR_SENSE	21	1	NO_TEST=1
PPE0AF	VDD_GPU_SENSE	20	1	NO_TEST=1

All: P4MM SM, IN, PP

PPE0AC P4MM SM 1 PP

PPE0AD P4MM SM 1 PP

SOC POWER PROBE POINTS

PPE0B1	PPVDD_AWAKE_CPU_SRAM	125 19	1
PPE0B2	PP0V779_S1_SRAM	125 19	1
PPE0B4	PP0V72_S2_VDD_LOW	126 24	1

All: P4MM SM, IN, PP

PMU AMUX INPUTS

57	DCIN_VSENSE	DCIN_VSENSE	45
57	DCIN_ISENSE	DCIN_ISENSE	45
57	PBUS_VSENSE	PBUS_VSENSE	45
57	BMON_ISENSE	BMON_ISENSE	45

All: IN, MAKE_BASE=TRUE, OUT

MPMU AMUX_B<1..3> NOT USED

36	P3V8AON_IMEAS	P3V8AON_IMEAS	45
58	MESA_HS_ISENSE	MESA_HS_ISENSE	45
63 62 46	MPMU_AMUXTDEV_TERM	MPMU_AMUXTDEV_TERM	45
63 62 46	MPMU_AMUXTDEV_TERM	MPMU_AMUXTDEV_TERM	45
57	MPMU_HS_ISENSE	MPMU_HS_ISENSE	39
57	SPMU_HS_ISENSE	SPMU_HS_ISENSE	39
57	P3V8AON_HS_ISENSE	P3V8AON_HS_ISENSE	39
59	WLBT_3V8_ISENSE	WLBT_3V8_ISENSE	39
57	P5VS2_HS_ISENSE	P5VS2_HS_ISENSE	39
57	PORT5V_HS_ISENSE	PORT5V_HS_ISENSE	39
60	TCON_3V8_ISENSE	TCON_3V8_ISENSE	39
58	LCDBKLT_HS_ISENSE	LCDBKLT_HS_ISENSE	39

All: IN, MAKE_BASE=TRUE, OUT

SENSE RESISTOR TEST POINTS

TPE001	ISNS_3V8AONHS_P	57	PLACE_NEAR=RD540.3:5MM
TPE002	ISNS_3V8AONHS_N	57	PLACE_NEAR=RD540.4:5MM
TPE003	ISNS_5VS2HS_P	57	PLACE_NEAR=RD550.3:5MM
TPE004	ISNS_5VS2HS_N	57	PLACE_NEAR=RD550.4:5MM
TPE005	ISNS_PORT5VHS_P	57	PLACE_NEAR=RD560.3:5MM
TPE006	ISNS_PORT5VHS_N	57	PLACE_NEAR=RD560.4:5MM
TPE007	PPDCIN_USBC_AON	125 57	PLACE_NEAR=RD501.1:5MM
TPE008			PLACE_NEAR=RD502.2:5MM
TPE009	CHGR_AMON	57 29 28	
TPE010			PLACE_NEAR=TPE009.1:5MM
TPE011	CHGR_BMON	57 29 28	
TPE012			PLACE_NEAR=TPE011.1:5MM
TPE013	PBUS_VSNS_OUT	57	
TPE014			PLACE_NEAR=TPE013.1:6MM
TPE015	ISNS_MPMUHS_P	57	PLACE_NEAR=RD570.3:10MM
TPE016	ISNS_MPMUHS_N	57	PLACE_NEAR=RD570.4:10MM
TPE017	ISNS_SPMUHS_P	57	PLACE_NEAR=RD580.3:5MM
TPE018	ISNS_SPMUHS_N	57	PLACE_NEAR=RD580.4:5MM
TPE019	ISNS_ATCHS_P	58	PLACE_NEAR=RD6A0.3:5MM
TPE020	ISNS_ATCHS_N	58	PLACE_NEAR=RD6A0.4:5MM
TPE021	ISNS_SDHS_P	58	PLACE_NEAR=RD6E0.3:5MM
TPE022	ISNS_SDHS_N	58	PLACE_NEAR=RD6E0.4:5MM
TPE023	ISNS_MESAHS_P	58	PLACE_NEAR=RD6B0.3:5MM
TPE024	ISNS_MESAHS_N	58	PLACE_NEAR=RD6B0.4:5MM
TPE025	ISNS_BKLTHS_P	58	PLACE_NEAR=RP850.4:5MM
TPE026	ISNS_BKLTHS_N	58	PLACE_NEAR=RP850.3:5MM
TPE027	ISNS_WLBT3V8_P	59	PLACE_NEAR=RD710.3:5MM
TPE028	ISNS_WLBT3V8_N	59	PLACE_NEAR=RD710.4:5MM
TPE029	ISNS_SPKRAMPL_P	59	PLACE_NEAR=RD720.3:5MM
TPE030	ISNS_SPKRAMPL_N	59	PLACE_NEAR=RD720.4:5MM
TPE031	ISNS_SPKRAMPR_P	59	PLACE_NEAR=RD730.3:5MM
TPE032	ISNS_SPKRAMPR_N	59	PLACE_NEAR=RD730.4:5MM
TPE033	ISNS_KBDLED_P	59	PLACE_NEAR=RD780.3:5MM
TPE034	ISNS_KBDLED_N	59	PLACE_NEAR=RD780.4:5MM
TPE035	ISNS_WLBT1V8_P	59	PLACE_NEAR=RD750.3:5MM
TPE036	ISNS_WLBT1V8_N	59	PLACE_NEAR=RD750.4:5MM
TPE037	ISNS_USBLS3V3_P	59	PLACE_NEAR=RD760.3:5MM
TPE038	ISNS_USBLS3V3_N	59	PLACE_NEAR=RD760.4:5MM
TPE039	ISNS_USBLS1V8_P	59	PLACE_NEAR=RD770.3:5MM
TPE040	ISNS_USBLS1V8_N	59	PLACE_NEAR=RD770.4:5.2MM
TPE041	ISNS_ALSCAM_P	60	PLACE_NEAR=RD830.3:5MM
TPE042	ISNS_ALSCAM_N	60	PLACE_NEAR=RD830.4:5MM
TPE043	ISNS_P3V29_BCON_P	60	PLACE_NEAR=RD810.3:5MM
TPE044	ISNS_P3V29_BCON_N	60	PLACE_NEAR=RD810.4:5MM
TPE045	ISNS_P3V8_TCON_P	60	PLACE_NEAR=RD820.3:5MM
TPE046	ISNS_P3V8_TCON_N	60	PLACE_NEAR=RD820.4:5MM
TPE047	ISNS_TPAD5V_P	60	PLACE_NEAR=RD840.3:5MM
TPE048	ISNS_TPAD5V_N	60	PLACE_NEAR=RD840.4:5MM
TPE049	ISNS_TPAD3V3_P	60	PLACE_NEAR=RD850.3:5MM
TPE050	ISNS_TPAD3V3_N	60	PLACE_NEAR=RD850.4:5MM
TPE051	ISNS_KBD3V3_P	60	PLACE_NEAR=RD860.3:5MM
TPE052	ISNS_KBD3V3_N	60	PLACE_NEAR=RD860.4:5MM
TPE053	ISNS_KBD1V8_P	60	PLACE_NEAR=RD890.3:5MM
TPE054	ISNS_KBD1V8_N	60	PLACE_NEAR=RD890.4:5MM
TPE055	CHGR_CSI_P	29	
TPE056	CHGR_CSI_N	29	PLACE_NEAR=TPE055.1:5MM
TPE057	CHGR_CSO_P	29	
TPE058	CHGR_CSO_N	29	PLACE_NEAR=TPE057.1:5MM
TPE061	ISNS_SPKRL3V8_P	58	PLACE_NEAR=RD640.3:5MM
TPE062	ISNS_SPKRL3V8_N	58	PLACE_NEAR=RD640.4:5MM
TPE063	ISNS_SPKRR3V8_P	58	PLACE_NEAR=RD650.3:5MM
TPE064	ISNS_SPKRR3V8_N	58	PLACE_NEAR=RD650.4:5MM
TPE059	ISNS_HDMI3V8HS_P	59	PLACE_NEAR=RD7A0.3:5MM
TPE060	ISNS_HDMI3V8HS_N	59	PLACE_NEAR=RD7A0.4:5MM

All: IN, TP-P4, TP

BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: POWER SUPPORT

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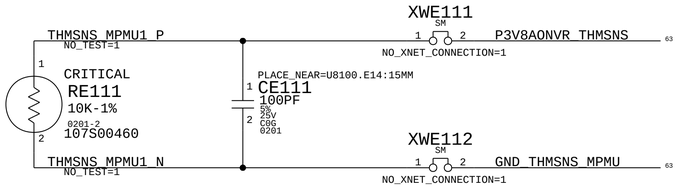
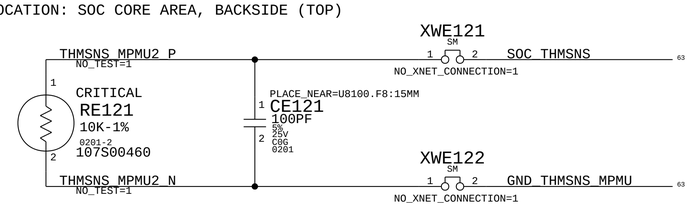
MAIN PMU TDEV1 [TMVR]

LOCATION: 3.8V AON VR BETWEEN PHASE 2 AND PHASE3 MOSFETS



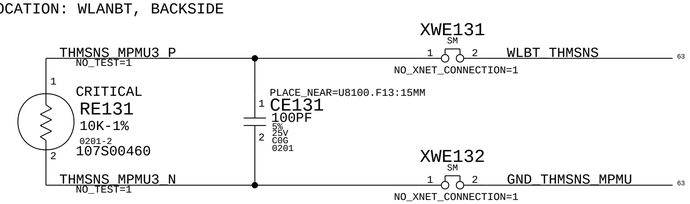
MAIN PMU TDEV2 [TSCD]

LOCATION: SOC CORE AREA, BACKSIDE (TOP)



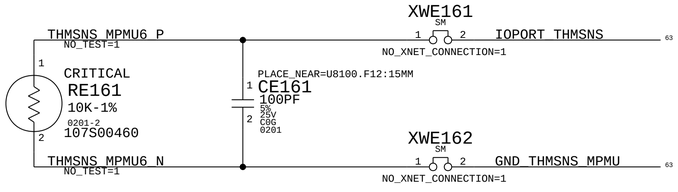
MAIN PMU TDEV3 [TW0P]

LOCATION: WLANBT, BACKSIDE



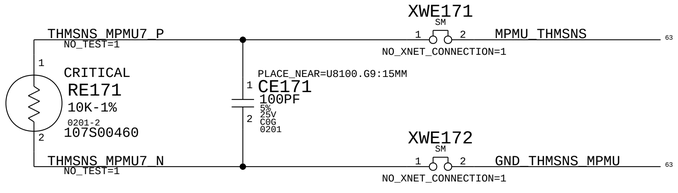
MAIN PMU TDEV6 [TIOP]

LOCATION: IO PORT PROXIMITY



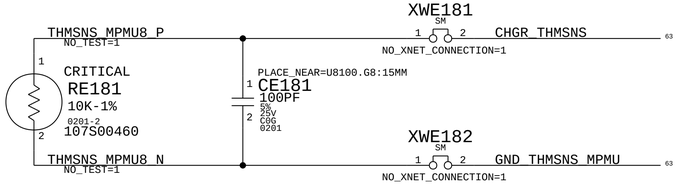
MAIN PMU TDEV7 [TPMP]

LOCATION: MAIN PMU, BETWEEN BUCK0 AND BUCK1 INDUCTORS



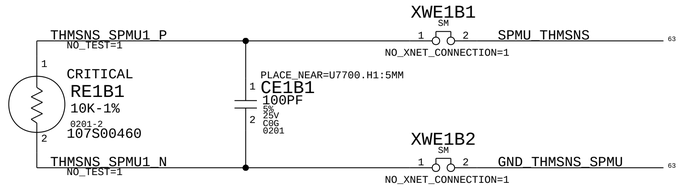
MAIN PMU TDEV8 [TCHP]

LOCATION: CHARGER, BETWEEN INDUCTOR AND MOSFETS



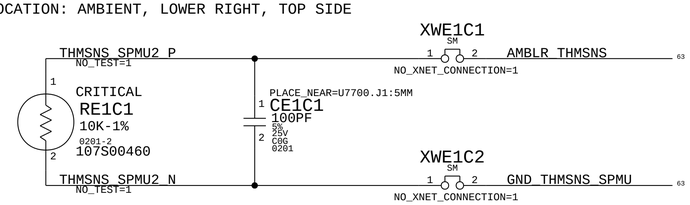
SECONDARY PMU TDEV1 [TPSP]

LOCATION: SECONDARY PMU, BUCK10 INDUCTOR PROXIMITY



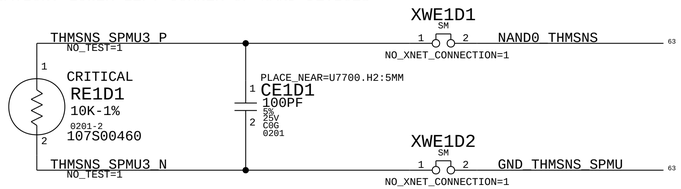
SECONDARY PMU TDEV2 [TaLR]

LOCATION: AMBIENT, LOWER RIGHT, TOP SIDE



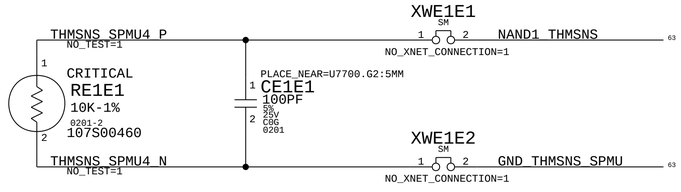
SECONDARY PMU TDEV3 [TH0a]

LOCATION: LOWER LEFT CORNER OF NAND DEVICES



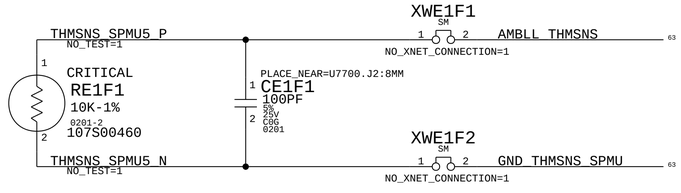
SECONDARY PMU TDEV4 [TH0b]

LOCATION: UPPER RIGHT CORNER OF NAND DEVICES

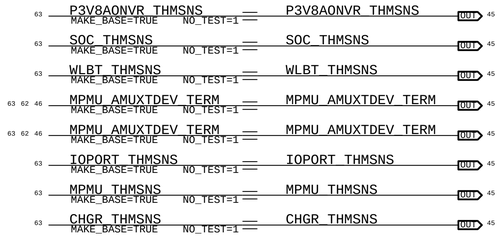


SECONDARY PMU TDEV5 [TaLW]

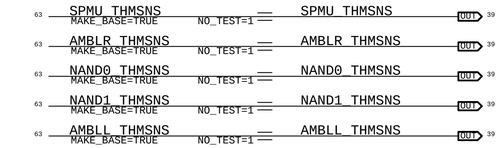
LOCATION: AMBIENT, LOWER LEFT, TOP SIDE



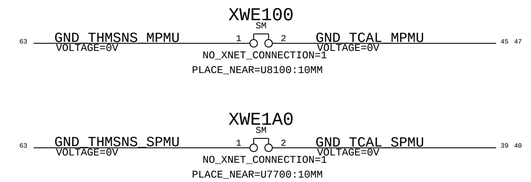
MPMU TDEV MAPPING



SPMU TDEV MAPPING

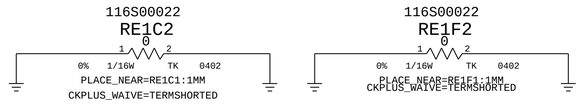


TAP NEGATIVE CLOSE TO VSS_REF



MAIN PMU TDEV<4-5>: UNUSED

DUMMY COMPONENTS FOR DFM



BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: THERMAL

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DRAWING NUMBER: 051-07754 | SIZE: D

REVISION: 6.0.0

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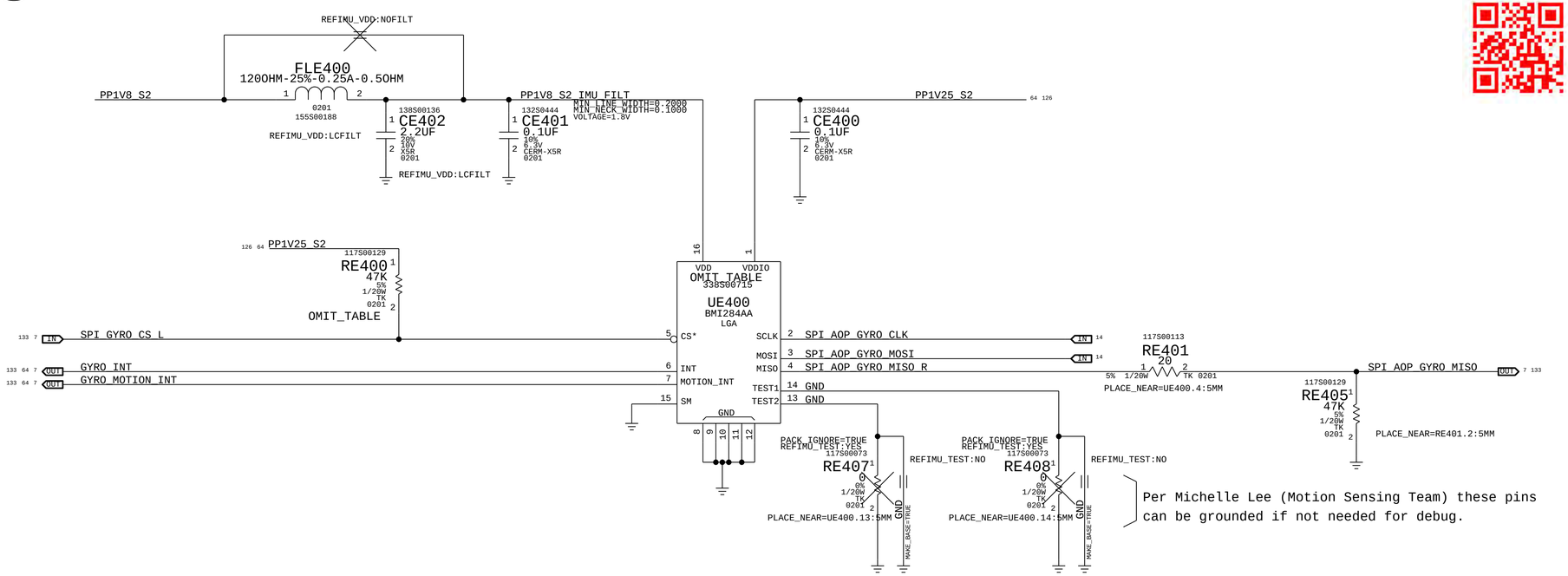
*** OK2INTEGRATE ***

A Sovereign Accelerometer and Gyroscope

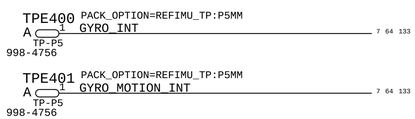
Datasheet Radar:



Per Michelle Lee (Motion Sensing Team) these pins can be grounded if not needed for debug.

MFG: Bosch
MPN: BMI284AA
APN: 338S00715
URL: https://www.bosch-sensortec.com/products/motion-sensors/imus/
Radar: rdar://61521702 (Sovereign: Datasheet)

B Test Points



C Sovereign BOM Options

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00715	1	IC,SOVEREIGN,BMI284,AA,LGA16	UE400	CRITICAL	REFIMU_IC:BMI284
338S00849	1	IC,SOVEREIGN2,BMI286,AA,LGA16	UE400	CRITICAL	REFIMU_IC:BMI286
117S00129	1	RES,TK,47K OHM,5%,1/20W,0201	RE400	CRITICAL	REFIMU_RE400:47K
118S00521	1	RES,TK,30K OHM,1%,1/20W,0201	RE400	CRITICAL	REFIMU_RE400:30K

BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: MOTION

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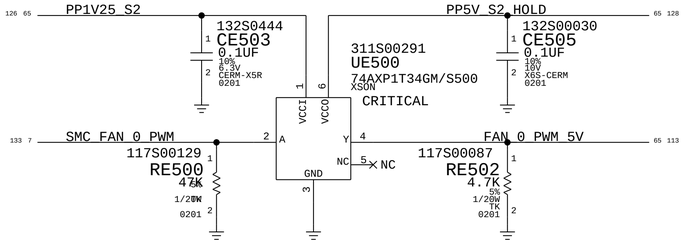
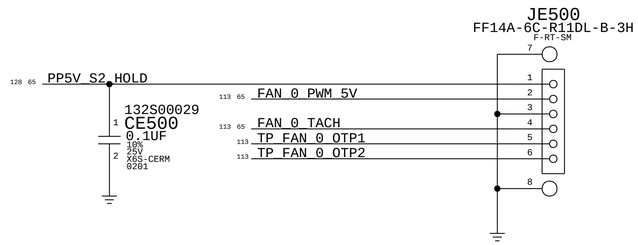
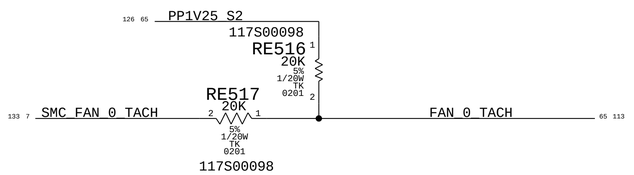
FAN CONTROLLERS

FAN PWM LEVEL SHIFTER



PWM FAN0 (LEFT) CONNECTOR





BOM_COST_GROUP=FANS

PAGE TITLE: FANS

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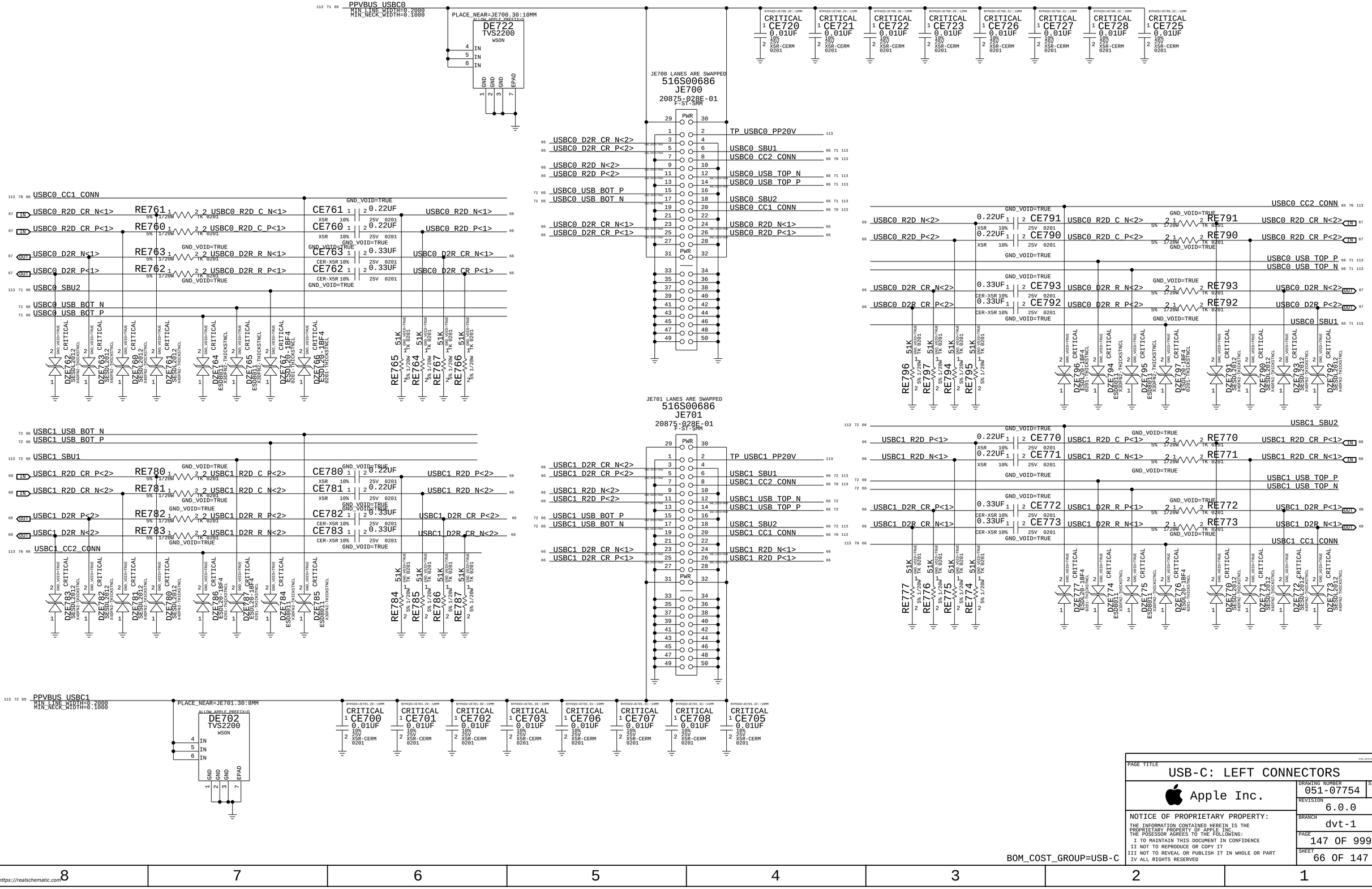

PAGE TITLE

USB-C: LEFT CONNECTORS

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*** OK2INTEGRATE ***

No lane swapping is allowed
Re-timer to SOC connections are set

USBC HIGH-SPEED AC COUPLING

139 12 IN	USBC_ATC0_R2D_C_P<1>	CF020 0.22UF	USBC_ATC0_R2D_P<1>	67	GND_VOID=TRUE
139 12 IN	USBC_ATC0_R2D_C_N<1>	CF021 0.22UF	USBC_ATC0_R2D_N<1>	67	GND_VOID=TRUE
139 12 IN	USBC_ATC0_R2D_C_P<2>	CF024 0.22UF	USBC_ATC0_R2D_P<2>	67	GND_VOID=TRUE
139 12 IN	USBC_ATC0_R2D_C_N<2>	CF025 0.22UF	USBC_ATC0_R2D_N<2>	67	GND_VOID=TRUE
139 12 BI	USBC_ATC0_D2R_P<1>	CF022 0.22UF	USBC_ATC0_D2R_C_P<1>	67	GND_VOID=TRUE
139 12 BI	USBC_ATC0_D2R_N<1>	CF023 0.22UF	USBC_ATC0_D2R_C_N<1>	67	GND_VOID=TRUE
139 12 BI	USBC_ATC0_D2R_P<2>	CF026 0.22UF	USBC_ATC0_D2R_C_P<2>	67	GND_VOID=TRUE
139 12 BI	USBC_ATC0_D2R_N<2>	CF027 0.22UF	USBC_ATC0_D2R_C_N<2>	67	GND_VOID=TRUE

All: 1 | 2 | 20% 6.3V 0201 X5R

RF043 1/20W 1 5% 2 47K TK 0201 CIO_ATC0_LSTX 67 130 139
RF044 1/20W 1 5% 2 47K TK 0201 CIO_ATC0_LSRX 67 130 139

ATCRTMR0_CFP_RCAL_NEG 67
CF011 10PF 1 | 2 5% 25V C0G 0201
RF011 200 1 | 2 1% 1/20W TF 0201-1
ATCRTMR0_CFP_RCAL_POS 67

ATCRTMR0_SFP_RCAL_NEG 67
CF010 10PF 1 | 2 5% 25V C0G 0201
RF010 200 1 | 2 1% 1/20W TK 0201-1
ATCRTMR0_SFP_RCAL_POS 67

ATCRTMR0_XTAL24M_OUT 67
RF060 499 1% 1/20W TK 0201 1 | 2
197S0591 CRITICAL YF000 1.6X1.2MM 24.000MHZ-20PPM-9.5PF-60OHM
ATC0_24M_O_R 1 | 3 | 2 | 4
CF060 CRITICAL 15PF 5% 50V C0G 0201
ATCRTMR0_XTAL24M_IN 67
CF061 CRITICAL 131S0831 15PF 5% 50V C0G 0201

PP0V855_USBC_CIO 128 123
CF030 CRITICAL 14UF 20% X5R 4V 0402-D2X-1 3 | 1 | 4 | 2
CF031 CRITICAL 14UF 20% X5R 4V 0402-D2X-1 3 | 1 | 4 | 2
138S00149
CF032 0.1UF 10% 6.3V X6S 0201
CF033 0.1UF 10% 6.3V X6S 0201

PP0V805_USBC_FIXED 128 123 67
CF040 0.1UF 10% 6.3V X6S 0201
CF041 0.1UF 10% 6.3V X6S 0201
CF042 2.2UF 20% 4V X6S-CERM 0201
CF043 2.2UF 20% 4V X6S-CERM 0201
CF044 2.2UF 20% 4V X6S-CERM 0201
CF045 CRITICAL 14UF 20% X5R 4V 0402-D2X-1 3 | 1 | 4 | 2
CF046 CRITICAL 14UF 20% X5R 4V 0402-D2X-1 3 | 1 | 4 | 2

PP0V805_USBC_FIXED 128 123 67
CF050 0.1UF 10% 6.3V X6S 0201
PLACE_NEAR=UF000.G7:5MM

PPVDD_FIXED_ATCRTMR0_XTAL_R
PP0V805_USBC_FIXED 128
RF051 10 5% 1/20W TK 0201 1 | 2 VOLTAGE=0.805V
CF051 4UF 20% 2.5V X6S 0201
117S00094
138S00329

UF000 TMNB25B1-K1S1 FCCSP 338S00888 SYM 2 OF 2

J4	VDD_CIO_0	OMIT_TABLE CRITICAL	VDDIO12_CIO_0	K5	
J6	VDD_CIO_0		VDDIO12_CIO_0	K7	
J8	VDD_CIO_0		VDDIO12_CIO_0	L6	
F4	VDD_CIO_1		VDDIO12_CIO_1	D6	
F6	VDD_CIO_1		VDDIO12_CIO_1	E5	
F8	VDD_CIO_1		VDDIO12_CIO_1	E7	
			VDDIO12_PLL_SOC0	K8	
			VDDIO12_PLL_SOC1	H8	
			VDDIO12_XTAL	H9	
			VDDIO12	E9	
			VDDIO12	H3	
			VDDIO12	K9	
G4	VDD_FIXED		VDDIO12_EFUSE1	F3	
G5	VDD_FIXED		VDDIO12_AMUX	F7	
H5	VDD_FIXED				
H6	VDD_FIXED				
G7	VDD_FIXED_PLL				
G9	VDD_FIXED_XTAL				

VSS: A1, A2, A4, A6, A8, A10, A11, B2, B4, B6, B8, B10, C3, C5, C6, C7, C9, D1, D5, D7, D11, E3, E4, E6, E8, F2, F5, F10, G3, G6, G8

VSS: H4, H7, J2, J3, J5, J7, J10, K4, K6, K1, L5, L7, L11, M3, M5, M6, M7, M9, N2, N4, N6, N8, N10, P1, P2, P4, P6, P8, P10, P11

132S0395 CF034 0.1UF 10% 6.3V X6S 0201
138S00039 CF035 2.2UF 20% 4V X6S-CERM 0201
CF036 CRITICAL 14UF 20% X5R 4V 0402-D2X-1 3 | 1 | 4 | 2
CF037 CRITICAL 14UF 20% X5R 4V 0402-D2X-1 3 | 1 | 4 | 2
PP1V2_USBC_VDDIO 70 123 128

138S00039 CF052 2.2UF 20% 4V X6S-CERM 0201
PLACE_NEAR=UF000.K8:5MM
PP1V2_USBC_VDDIO 128

PP1V2_ATCRTMR0_VDDIO_XTAL_F VOLTAGE=1.2V
155S0644 FLF000 240-OHM-0.2A-0.9-OHM 0201
CF063 2.2UF 20% 4V X6S-CERM 0201 138S00039
CF062 0.1UF 10% 6.3V X6S 0201 132S0395
PP1V2_USBC_VDDIO 128

Connect to GND directly or via a resistor
GND 130

132S0395 CF064 0.1UF 10% 6.3V X6S 0201
PP1V2_USBC_VDDIO 128

PACK_OPTION=ATC_BOUNDARYSCAN:YES
RF045 47K 5% 1/20W TK 0201
ATCRTMR0_JTAG_TDO 67
PACK_OPTION=ATC_BOUNDARYSCAN:NO
RF047 47K 5% 1/20W TK 0201
ATCRTMR0_JTAGL_SEL 67
PACK_OPTION=ATC_BOUNDARYSCAN:YES
RF040 10K 5% 1/20W TK 0201
ATCRTMR0_TESTMODE 67
PACK_OPTION=ATC_BOUNDARYSCAN:NO

Re-timer to connector connections are set

UF000 TMNB25B1-K1S1 FCCSP 338S00888 SYM 1 OF 2
OMIT_TABLE CRITICAL

67	USBC_ATC0_D2R_C_P<1> GND_VOID=TRUE	P9	SFP_PHY_RXTX_0_P	SFP PHY	CFP PHY	A9	USBC0_R2D_CR_P<1> GND_VOID=TRUE OUT 66
67	USBC_ATC0_D2R_C_N<1> GND_VOID=TRUE	N9	SFP_PHY_RXTX_0_N			B9	USBC0_R2D_CR_N<1> GND_VOID=TRUE OUT 66
67	USBC_ATC0_D2R_C_P<2> GND_VOID=TRUE	P5	SFP_PHY_RXTX_2_P			A5	USBC0_R2D_CR_P<2> GND_VOID=TRUE OUT 66
67	USBC_ATC0_D2R_C_N<2> GND_VOID=TRUE	N5	SFP_PHY_RXTX_2_N			B5	USBC0_R2D_CR_N<2> GND_VOID=TRUE OUT 66
67	USBC_ATC0_R2D_P<1> GND_VOID=TRUE	P7	SFP_PHY_RXTX_1_P			A7	USBC0_D2R_P<1> BI 66
67	USBC_ATC0_R2D_N<1> GND_VOID=TRUE	N7	SFP_PHY_RXTX_1_N			B7	USBC0_D2R_N<1> BI 66
67	USBC_ATC0_R2D_P<2> GND_VOID=TRUE	P3	SFP_PHY_RXTX_3_P			A3	USBC0_D2R_P<2> GND_VOID=TRUE BI 66
67	USBC_ATC0_R2D_N<2> GND_VOID=TRUE	N3	SFP_PHY_RXTX_3_N			B3	USBC0_D2R_N<2> GND_VOID=TRUE BI 66
69 BI	USBC_ATC0_AUX_C_P	L4	SFP_LPDP_AUX_P			D4	USBC0_AUX_P BI 69
69 BI	USBC_ATC0_AUX_C_N	M4	SFP_LPDP_AUX_N			C4	USBC0_AUX_N TR 69
139 130 67 IN	CIO_ATC0_LSTX	G1	USB4_SFP_SB_RX			F1	USBC0_CIO_LSRX IN 74
139 130 67 OUT	CIO_ATC0_LSRX	G2	USB4_SFP_SB_TX			E1	USBC0_CIO_LSTX BI 74
						H1	ATCRTMR0_LSTX_DIR USB4_CFP_SB_TX_DIR OUT 74
67	ATCRTMR0_SFP_RCAL_POS	M8	SFP_PHY_RCAL_P			C8	ATCRTMR0_CFP_RCAL_POS 67
67	ATCRTMR0_SFP_RCAL_NEG	L8	SFP_PHY_RCAL_N			D8	ATCRTMR0_CFP_RCAL_NEG 67
70 IN	ATCRTMR0_CHIPID_0	M1	CHIP_ID_0	GPIO	PERIPHERAL	N11	SPI_ATCRTMR0_CS_L QSPI_CS* 67
70 IN	ATCRTMR0_CHIPID_1	N1	CHIP_ID_1			M11	SPI_ATCRTMR0_CLK QSPI_SCLK 67
70 IN	ATCRTMR0_BOOT_CONFIG0	H2	BOOT_CONFIG0			K10	SPI_ATCRTMR0_DIO<0> QSPI_DQ0 67
70 IN	ATCRTMR0_BOOT_CONFIG1	J1	BOOT_CONFIG1			K11	SPI_ATCRTMR0_DIO<1> QSPI_DQ1 67
70 IN	ATCRTMR0_BOOT_CONFIG2	K1	BOOT_CONFIG2			J9	SPI_ATCRTMR0_DIO<2> QSPI_DQ2 67
113 71 69 IN	ATCRTMR0_FORCE_DFU	C1	FORCE_DFU			J11	SPI_ATCRTMR0_DIO<3> QSPI_DQ3 67
130	NC_ATCRTMR0_GPIO0	K2	GPIO0			C2	I2C_ATCRTMR_SCL I2C0_SCL IN 52
	NC_ATCRTMR0_GPIO1 NO_TEST=1	L3	GPIO1			D3	I2C_ATCRTMR_SDA I2C0_SDA BI 52
130	NC_ATCRTMR0_GPIO2	K3	GPIO2			E2	I2C_UPC0_ATCRTMR0_SCL_1V2 I2C1_SCL IN 77
130	NC_ATCRTMR0_GPIO3	L10	GPIO3			D2	I2C_UPC0_ATCRTMR0_SDA_1V2 I2C1_SDA BI 77
						B1	INT_I2C_UPC0_ATCRTMR0_L I2C1_INT OUT 69 71
130 113 74 IN	ATCRTMR0_RESET_1V2_L	L2	COLD_RESET*	CLOCKS AND RESET	TEST AND DEBUG	L9	ATCRTMR0_TESTMODE TESTMODE 67
		M2	CFSB			C11	ATCRTMR0_JTAGL_SEL JTAG_SEL 67
67	ATCRTMR0_XTAL24M_IN	F11	XI0			B11	SWD_NUB_ATCRTMR_SWCLK JTAG_TCK BI 130
67	ATCRTMR0_XTAL24M_OUT	E11	XO0			D10	SWD_NUB_ATCRTMR_SWDIO JTAG_TMS BI 130
						D9	TST_ATCRTMR0_JTAG_TDI JTAG_TDI 77 130
						C10	ATCRTMR0_JTAG_TDO JTAG_TDO 67
						E10	TST_ATCRTMR0_JTAG_TRESET JTAG_TRST* 77 130
						F9	TST_ATCRTMR0_ANALOGMUX_OUT ANALOGMUX_OUT 77 130
						M10	NC_ATCRTMR0_TST_CLKOUT TST_CLKOUT 130
						H10	NC_ATCRTMR0_CLK_LVDS_P<0> TST_CLK_LVDS_0_P NO_TEST=1
						H11	NC_ATCRTMR0_CLK_LVDS_N<0> TST_CLK_LVDS_0_N NO_TEST=1
						G11	NC_ATCRTMR0_CLK_LVDS_P<1> TST_CLK_LVDS_1_P NO_TEST=1
						G10	NC_ATCRTMR0_CLK_LVDS_N<1> TST_CLK_LVDS_1_N NO_TEST=1

RF097 1/20W 1 5% 2 33 TK 0201 SPI_ATCRTMR0_DIO<0> 67 | SPI_ATCRTMR0_R_DIO<0> 67
RF098 1/20W 1 5% 2 33 TK 0201 SPI_ATCRTMR0_DIO<1> 67 | SPI_ATCRTMR0_R_DIO<1> 67

PP1V2_USBC_VDDIO 67 128
RF090 3.3K 5% 1/20W TK 0201
NOSTUFF RF091 3.3K 5% 1/20W TK 0201
NOSTUFF RF092 3.3K 5% 1/20W TK 0201
NOSTUFF RF093 3.3K 5% 1/20W TK 0201
CF090 1.0UF 20% 6.3V X5R 0201-1

OMIT_TABLE CRITICAL 335S00574
UF090 64MBIT-1.2V W25Q64NE XSON-1

67	SPI_ATCRTMR0_CLK	RF094 33	SPI_ATCRTMR0_CLK_R	6 CLK
67	SPI_ATCRTMR0_CS_L			1 CS*
67	SPI_ATCRTMR0_DIO<2>	RF095 33	SPI_ATCRTMR0_R_DIO<2>	3 WP*(IO2)
67	SPI_ATCRTMR0_DIO<3>	RF096 33	SPI_ATCRTMR0_R_DIO<3>	7 HOLD*(IO3)
			SPI_ATCRTMR0_R_DIO<0>	5 DI(IO0)
			SPI_ATCRTMR0_R_DIO<1>	2 DO(IO1)

GND 4 EPAD 9
PACK_OPTION=ATC_RTMR_ROM:XSON

PP1V2_USBC_VDDIO 128
OMIT_TABLE CRITICAL
UF090 MX25S6473F WLCSP 335S00594

67	SPI_ATCRTMR0_CLK_R	D2	SCLK
67	SPI_ATCRTMR0_CS_L	B3	CS*
67	SPI_ATCRTMR0_R_DIO<2>	D3	SIO2
67	SPI_ATCRTMR0_R_DIO<3>	C2	SIO3
		E2	SI/SIO0 SPI_ATCRTMR0_R_DIO<0> 67
		C3	SO/SIO1 SPI_ATCRTMR0_R_DIO<1> 67
		A1	NC
		A4	NC
		F1	NC
		F4	NC

VCC B2 | GND E3
PACK_IGNORE=TRUE
PACK_OPTION=ATC_RTMR_ROM:WLCSP

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C: High Speed ATC0

Apple Inc.

DRAWING NUMBER 051-07754 | SIZE D
REVISION 6.0.0
BRANCH dvt-1
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SHEET 67 OF 147

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*** OK2INTEGRATE ***

No lane swapping is allowed
Re-timer to SOC connections are set

USBC HIGH-SPEED AC COUPLING

USBC_ATC1_R2D_C_P<1>	CF120 0.22UF	USBC_ATC1_R2D_P<1>	GND_VOID=TRUE
USBC_ATC1_R2D_C_N<1>	CF121 0.22UF	USBC_ATC1_R2D_N<1>	GND_VOID=TRUE
USBC_ATC1_R2D_C_P<2>	CF124 0.22UF	USBC_ATC1_R2D_P<2>	GND_VOID=TRUE
USBC_ATC1_R2D_C_N<2>	CF125 0.22UF	USBC_ATC1_R2D_N<2>	GND_VOID=TRUE
USBC_ATC1_D2R_P<1>	CF122 0.22UF	USBC_ATC1_D2R_C_P<1>	GND_VOID=TRUE
USBC_ATC1_D2R_N<1>	CF123 0.22UF	USBC_ATC1_D2R_C_N<1>	GND_VOID=TRUE
USBC_ATC1_D2R_P<2>	CF126 0.22UF	USBC_ATC1_D2R_C_P<2>	GND_VOID=TRUE
USBC_ATC1_D2R_N<2>	CF127 0.22UF	USBC_ATC1_D2R_C_N<2>	GND_VOID=TRUE

All: 20% 6.3V X5R 0201

RF143 47K 1/20W 5% TK 0201 — CIO_ATC1_LSTX
RF144 47K 1/20W 5% TK 0201 — CIO_ATC1_LSRX

CF111 10PF 5% 25V C0G 0201 — RF111 200 1% 1/20W TF 0201-1 — ATCRTMR1_CFP_RCAL_NEG / ATCRTMR1_CFP_RCAL_POS
CF110 10PF 5% 25V C0G 0201 — RF110 200 1% 1/20W TF 0201-1 — ATCRTMR1_SFP_RCAL_NEG / ATCRTMR1_SFP_RCAL_POS

RF160 499 1% 1/20W TK 0201 — ATCRTMR1_XTAL24M_OUT
197S0591 CRITICAL YF100 1.6X1.2OMM 24.000MHZ-20PPM-9.5PF-60OHM — ATC1_24M_O_R
CF160 CRITICAL 15PF 5% 50V C0G 0201
CF161 CRITICAL 131S0831 15PF 5% 50V C0G 0201 — ATCRTMR1_XTAL24M_IN

PP0V855_USBC_CIO
CF130 CRITICAL 14UF 20% X5R 4V 0402-D2X-1
CF131 CRITICAL 14UF 20% X5R 4V 0402-D2X-1
CF132 0.1UF 10% 6.3V X6S 0201
CF133 0.1UF 10% 6.3V X6S 0201

PP0V805_USBC_FIXED
CF140 0.1UF 10% 6.3V X6S 0201
CF141 0.1UF 10% 6.3V X6S 0201
CF142 2.2UF 20% 4V X6S-CERM 0201
CF143 2.2UF 20% 4V X6S-CERM 0201
CF144 2.2UF 20% 4V X6S-CERM 0201
CF145 CRITICAL 14UF 20% X5R 4V 0402-D2X-1
CF146 CRITICAL 14UF 20% X5R 4V 0402-D2X-1

PP0V805_USBC_FIXED
CF150 0.1UF 10% 6.3V X6S 0201
PLACE_NEAR=UF100.G7:5MM

PPVDD_FIXED_ATCRTMR1_XTAL_R
PP0V805_USBC_FIXED
RF151 10 5% 1/20W TK 0201 — VOLTAGE=0.805V
CF151 4UF 20% 2.5V X6S 0201 — 138S00329
117S00094

UF100 TMNB25B1-K1S1 FCCSP 338S00888 SYM 2 OF 2
OMIT_TABLE CRITICAL

J4, J6, J8	VDD_CIO_0	VDDIO12_CIO_0	K5, K7, L6
F4, F6, F8	VDD_CIO_1	VDDIO12_CIO_1	D6, E5, E7
G4, G5, H5, H6	VDD_FIXED	VDDIO12_PLL_SOC0	K8
G7	VDD_FIXED_PLL	VDDIO12_PLL_SOC1	H8
G9	VDD_FIXED_XTAL	VDDIO12_XTAL	H9
		VDDIO12	E9, H3, K9
		VDDIO12_EFUSE1	F3
		VDDIO12_AMUX	F7
A1, A2, A4, A6, A8, A10, A11, B2, B4, B6, B8, B10, C3, C5, C6, C7, C9, D1, D5, D7, D11, E3, E4, E6, E8, F2, F5, F10, G3, G6, G8	VSS	H4, H7, J2, J3, J5, J7, J10, K4, K6, L1, L5, L7, L11, M3, M5, M6, M7, M9, N2, N4, N6, N8, N10, P1, P2, P4, P6, P8, P10, P11	VSS

PP1V2_USBC_VDDIO
132S0395 CF134 0.1UF 10% 6.3V X6S 0201
138S00039 CF135 2.2UF 20% 4V X6S-CERM 0201
CF136 CRITICAL 14UF 20% X5R 4V 0402-D2X-1
CF137 CRITICAL 14UF 20% X5R 4V 0402-D2X-1

138S00039 CF152 2.2UF 20% 4V X6S-CERM 0201 — PLACE_NEAR=UF100.K8:5MM
PP1V2_USBC_VDDIO
PP1V2_ATCRTMR1_VDDIO_XTAL_F — VOLTAGE=1.2V
155S0644 FLE100 240-OHM-0.2A-0.9-OHM 0201
CF163 2.2UF 20% 4V X6S-CERM 0201 — 138S00039
CF162 0.1UF 10% 6.3V X6S 0201 — 132S0395
PP1V2_USBC_VDDIO

Connect to GND directly or via a resistor
GND
PP1V2_USBC_VDDIO
132S0395 CF164 0.1UF 10% 6.3V X6S 0201

PACK_OPTION=ATC_BOUNDARYSCAN:YES
RF145 47K 1/20W 5% TK 0201 — ATCRTMR1_JTAG_TDO
PACK_OPTION=ATC_BOUNDARYSCAN:NO
RF147 47K 1/20W 5% TK 0201 — ATCRTMR1_JTAGL_SEL
PACK_OPTION=ATC_BOUNDARYSCAN:YES
RF140 10K 1/20W 5% TK 0201 — ATCRTMR1_TESTMODE
PACK_OPTION=ATC_BOUNDARYSCAN:NO

Re-timer to connector connections are set

UF100 TMNB25B1-K1S1 FCCSP 338S00888 SYM 1 OF 2
OMIT_TABLE CRITICAL

SFP PHY

USBC_ATC1_D2R_C_P<1>	P9	SFP_PHY_RXTX_0_P	CFP_PHY_RXTX_0_P — USBC1_R2D_CR_P<1>
USBC_ATC1_D2R_C_N<1>	N9	SFP_PHY_RXTX_0_N	CFP_PHY_RXTX_0_N — USBC1_R2D_CR_N<1>
USBC_ATC1_D2R_C_P<2>	P5	SFP_PHY_RXTX_2_P	CFP_PHY_RXTX_2_P — USBC1_R2D_CR_P<2>
USBC_ATC1_D2R_C_N<2>	N5	SFP_PHY_RXTX_2_N	CFP_PHY_RXTX_2_N — USBC1_R2D_CR_N<2>
USBC_ATC1_R2D_P<1>	P7	SFP_PHY_RXTX_1_P	CFP_PHY_RXTX_1_P — USBC1_D2R_P<1>
USBC_ATC1_R2D_N<1>	N7	SFP_PHY_RXTX_1_N	CFP_PHY_RXTX_1_N — USBC1_D2R_N<1>
USBC_ATC1_R2D_P<2>	P3	SFP_PHY_RXTX_3_P	CFP_PHY_RXTX_3_P — USBC1_D2R_P<2>
USBC_ATC1_R2D_N<2>	N3	SFP_PHY_RXTX_3_N	CFP_PHY_RXTX_3_N — USBC1_D2R_N<2>
USBC_ATC1_AUX_C_P	L4	SFP_LPDP_AUX_P	CFP_LPDP_AUX_P — USBC1_AUX_P
USBC_ATC1_AUX_C_N	M4	SFP_LPDP_AUX_N	CFP_LPDP_AUX_N — USBC1_AUX_N
CIO_ATC1_LSTX	G1	USB4_SFP_SB_RX	USB4_CFP_SB_RX — USBC1_CIO_LSRX
CIO_ATC1_LSRX	G2	USB4_SFP_SB_TX	USB4_CFP_SB_TX — USBC1_CIO_LSTX
			USB4_CFP_SB_TX_DIR — ATCRTMR1_LSTX_DIR
ATCRTMR1_SFP_RCAL_POS	M8	SFP_PHY_RCAL_P	CFP_PHY_RCAL_P — ATCRTMR1_CFP_RCAL_POS
ATCRTMR1_SFP_RCAL_NEG	L8	SFP_PHY_RCAL_N	CFP_PHY_RCAL_N — ATCRTMR1_CFP_RCAL_NEG

GPIO

ATCRTMR1_CHIPID_0	M1	CHIP_ID_0	
ATCRTMR1_CHIPID_1	N1	CHIP_ID_1	
ATCRTMR1_BOOT_CONFIG0	H2	BOOT_CONFIG0	
ATCRTMR1_BOOT_CONFIG1	J1	BOOT_CONFIG1	
ATCRTMR1_BOOT_CONFIG2	K1	BOOT_CONFIG2	
ATCRTMR1_FORCE_DFU	C1	FORCE_DFU	
NC_ATCRTMR1_GPIO0	K2	GPIO0	
NC_ATCRTMR1_GPIO1 NO_TEST=1	L3	GPIO1	
NC_ATCRTMR1_GPIO2	K3	GPIO2	
NC_ATCRTMR1_GPIO3	L10	GPIO3	

PERIPHERAL

		QSPI_CS*	N11 SPI_ATCRTMR1_CS_L
		QSPI_SCLK	M11 SPI_ATCRTMR1_CLK
		QSPI_DQ0	K10 SPI_ATCRTMR1_DIO<0>
		QSPI_DQ1	K11 SPI_ATCRTMR1_DIO<1>
		QSPI_DQ2	J9 SPI_ATCRTMR1_DIO<2>
		QSPI_DQ3	J11 SPI_ATCRTMR1_DIO<3>
		I2C0_SCL	C2 I2C_ATCRTMR_SCL
		I2C0_SDA	D3 I2C_ATCRTMR_SDA
		I2C1_SCL	E2 I2C_UPC1_ATCRTMR1_SCL_1V2
		I2C1_SDA	D2 I2C_UPC1_ATCRTMR1_SDA_1V2
		I2C1_INT	B1 INT_I2C_UPC1_ATCRTMR1_L

CLOCKS AND RESET

ATCRTMR1_RESET_1V2_L	L2	COLD_RESET*	
	M2	CFSB	
ATCRTMR1_XTAL24M_IN	F11	XI0	
ATCRTMR1_XTAL24M_OUT	E11	XO0	

TEST AND DEBUG

		TESTMODE	L9 ATCRTMR1_TESTMODE
		JTAG_SEL	C11 ATCRTMR1_JTAGL_SEL
		JTAG_TCK	B11 SWD_NUB_ATCRTMR_SWCLK
		JTAG_TMS	D10 SWD_NUB_ATCRTMR_SWDIO
		JTAG_TDI	D9 NC_ATCRTMR1_JTAG_TDI
		JTAG_TDO	C10 ATCRTMR1_JTAG_TDO
		JTAG_TRST*	E10 NC_ATCRTMR1_JTAG_TRESET
		ANALOGMUX_OUT	F9 NC_ATCRTMR1_ANALOGMUX_OUT
		TST_CLKOUT	M10 NC_ATCRTMR1_TST_CLKOUT
		TST_CLK_LVDS_0_P	H10 NC_ATCRTMR1_CLK_LVDS_P<0> NO_TEST=1
		TST_CLK_LVDS_0_N	H11 NC_ATCRTMR1_CLK_LVDS_N<0> NO_TEST=1
		TST_CLK_LVDS_1_P	G11 NC_ATCRTMR1_CLK_LVDS_P<1> NO_TEST=1
		TST_CLK_LVDS_1_N	G10 NC_ATCRTMR1_CLK_LVDS_N<1> NO_TEST=1

RF197 33 1/20W 5% TK 0201 — SPI_ATCRTMR1_DIO<0> / SPI_ATCRTMR1_R_DIO<0>
RF198 33 1/20W 5% TK 0201 — SPI_ATCRTMR1_DIO<1> / SPI_ATCRTMR1_R_DIO<1>

PP1V2_USBC_VDDIO
RF190 3.3K 5% 1/20W TK 0201
NOSTUFF RF191 3.3K 5% 1/20W TK 0201
NOSTUFF RF192 3.3K 5% 1/20W TK 0201
NOSTUFF RF193 3.3K 5% 1/20W TK 0201
CF190 1.0UF 20% 6.3V X5R 0201-1

UF190 64MBIT-1.2V W25Q64NE XSON-1 335S00574 — OMIT_TABLE CRITICAL
PACK_OPTION=ATC_RTMR_ROM:XSON

SPI_ATCRTMR1_CLK	RF194 33	SPI_ATCRTMR1_CLK_R	CLK
SPI_ATCRTMR1_CS_L		SPI_ATCRTMR1_CS_L	CS*
SPI_ATCRTMR1_DIO<2>	RF195 33	SPI_ATCRTMR1_R_DIO<2>	WP*(IO2)
SPI_ATCRTMR1_DIO<3>	RF196 33	SPI_ATCRTMR1_R_DIO<3>	HOLD*(IO3)
		SPI_ATCRTMR1_R_DIO<0>	DI(IO0)
		SPI_ATCRTMR1_R_DIO<1>	DO(IO1)

PP1V2_USBC_VDDIO
UF190 MX25S6473F WLCSP 335S00594 — OMIT_TABLE CRITICAL
PACK_IGNORE=TRUE
PACK_OPTION=ATC_RTMR_ROM:WLCSP

SPI_ATCRTMR1_CLK_R	D2	SCLK	
SPI_ATCRTMR1_CS_L	B3	CS*	
SPI_ATCRTMR1_R_DIO<2>	D3	SIO2	
SPI_ATCRTMR1_R_DIO<3>	C2	SIO3	
	E2	SI/SIO0	SPI_ATCRTMR1_R_DIO<0>
	C3	SO/SIO1	SPI_ATCRTMR1_R_DIO<1>
	A1, A4, F1, F4	NC	NC

BOM_COST_GROUP=TBT

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	Apple Inc.
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*** OK2INTEGRATE ***

PP3V3_UPC0_LDO

RF260 3.3K 5% 1/20W TK 0201

RF261 3.3K 5% 1/20W TK 0201

RF263 3.3K 5% 1/20W TK 0201

RF262 3.3K 5% 1/20W TK 0201

CF260 1UF 10% 6.3V CERM 402

SPI Master Ace

UF260 8MBIT-3.0V W25Q80DVUXIE USON OMIT_TABLE CRITICAL 335S00133

CLK, CS*, WP*(IO2), HOLD*(IO3), DI(IO0), DO(IO1), GND, EPAD

ROM_UPC01_WP_L

ROM_UPC01_HOLD_L

NOSTUFF RF264 3.3K 5% 1/20W TK 0201

SPI_UPC01_MOSI — RF289 15 — SPI_UPC01_R_MOSI

SPI_UPC01_MISO — RF288 15 — SPI_UPC01_R_MISO

NO_XNET_CONNECTION=1

RF284 100 — SPI_UPC01_CLK_DBG

SPI_UPC01_CLK — RF285 15 — SPI_UPC01_R_CLK

RF287 15 — SPI_UPC01_CS_L — SPI_UPC01_R_CS_L

PP1V25_S2

PP3V3_S2_LDO

CF230 0.1UF 10% 6.3V CERM-X5R 0201

CF231 0.1UF 10% 6.3V CERM-X5R 0201

UF230 SN74AXC1T45-S SOT-5X3 CRITICAL

VCCA, VCCB, DIR, A, B, GND

PMU_ACTIVE_READY — ATCRTMR01_ACTIVE_READY_3V3

PACK_OPTION=ACTIVE_READY:LARGE_PITCH

UF230 SN74AXC1T45 X2SON CRITICAL 311S00212

PACK_IGNORE=TRUE

PACK_OPTION=ACTIVE_READY:SMALL_PITCH_CHECK_WITH_DFM

RF212 1.5K 5% 1/20W TK 0201

RF213 1.5K 5% 1/20W TK 0201

INT_I2C_UPC0_ATCRTMR0_L

INT_I2C_UPC1_ATCRTMR1_L

USBC_ATC1_AUX_P — CF236 0.1UF 10% 6.3V CERM-X5R 0201 — USBC_ATC1_AUX_C_P

USBC_ATC1_AUX_N — CF237 0.1UF 10% 6.3V CERM-X5R 0201 — USBC_ATC1_AUX_C_N

USBC_ATC0_AUX_P — CF275 0.1UF 10% 6.3V CERM-X5R 0201 — USBC_ATC0_AUX_C_P

USBC_ATC0_AUX_N — CF276 0.1UF 10% 6.3V CERM-X5R 0201 — USBC_ATC0_AUX_C_N

Ace 0 is SPI Ace?

PACK_OPTION=USBC_SPI_UPC0

SPI_UPC01_R_CLK, SPI_UPC01_R_CS_L, SPI_UPC01_R_MOSI, SPI_UPC01_R_MISO — MAKE_BASE=TRUE

Ace 1 is SPI Ace?

PACK_OPTION=USBC_SPI_UPC1

GND, GND, GND, GND

SWD_UPC_SWCLK — SWD_UPC_SWCLK

SWD_UPC_SWDIO0 — SWD_UPC_SWDIO0

PP3V3_UPC0_LDO — PP3V3_UPC0_LDO MAKE_BASE=TRUE

Ace 1 is UART Ace?

PACK_OPTION=USBC_SPI_UPC0

GND, GND, GND, GND

SWD_UPC01_UART_CLK — SWD_UPC01_UART_CLK

SWD_UPC01_UART_DATA — SWD_UPC01_UART_DATA

PACK_OPTION=USBC_SPI_UPC0

RF273 100K 1/20W 5% TK 0201 — PD_UPC1_HPD

UART_UPC01_TX — UART_UPC01_TX

UART_UPC01_RX — UART_UPC01_RX

UART_UPC01_RX

Ace 0 is UART Ace?

PACK_OPTION=USBC_SPI_UPC1

SPI_UPC01_R_CLK, SPI_UPC01_R_CS_L, SPI_UPC01_R_MOSI, SPI_UPC01_R_MISO — MAKE_BASE=TRUE

SWD_UPC_SWCLK, SWD_UPC_SWDIO0

RF274 100K 1/20W 5% TK 0201 — PD_UPC0_HPD

UART_UPC01_RX — UART_UPC01_RX

UART_UPC01_TX — UART_UPC01_TX

ACE ARKANOID CONN

JF200 USBC_DBG 505070-1222 M-ST-SM

PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

SMC		SOC
ATCRTMR0_FORCE_DFU		UPC_I2C_INT_L
I2C_SMC_UPC_SCL		I2C_UPC_SDA
I2C_SMC_UPC_SDA		I2C_UPC_SCL
UPC_SMC_I2C_INT_L		UPC0_SER_DBG
SPI_UPC01_CLK_DBG		UPC1_SER_DBG
UART_UPC01_TX		UART_UPC01_RX

SPI Ace — SPI Ace

BRIDGE ARKANOID CONN

JF201 USBC_DBG 505070-1222 M-ST-SM

PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

ATCRTMR0_RESET_L	INT_I2C_UPC0_ATCRTMR0_L
UPC0_ATCRTMR01_PWR_EN	I2C_UPC0_ATCRTMR0_SCL
PP1V2_USBC_VDDIO	I2C_UPC0_ATCRTMR0_SDA
PP0V855_USBC_CIO	UPC1_ATCRTMR01_PWR_EN
ATCRTMR1_RESET_L	INT_I2C_UPC1_ATCRTMR1_L
I2C_UPC1_ATCRTMR1_SDA	I2C_UPC1_ATCRTMR1_SCL

USBC_DBG

RF280 200K 0201 5% 1/20W

PP1V25_S2 — CF281 0.1UF 10% 6.3V CERM-X5R 0201

PP3V3_S2_LDO — CF280 0.1UF 10% 6.3V CERM-X5R 0201

RF282 5.1K 5% 1/20W TK 0201

RF283 5.1K 5% 1/20W TK 0201

PACK_OPTION=PKGS:SMALL_PITCH

UF280 LSF0102 X2SON-COMBO 311S00234

VREF_A, VREF_B, A1, A2, B1, B2, EN, GND

I2C_UPC_SCL — I2C_UPC01_3V3_SCL

I2C_UPC_SDA — I2C_UPC01_3V3_SDA

PACK_IGNORE=TRUE

PACK_OPTION=PKGS:LARGER_PITCH

UF280 LSF0102 VSSOP 311S00257

AARDVARKANOID CONN

JF202 USBC_DBG 505070-1222 M-ST-SM

PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

SPI ACE

PP1V25_S2	SPI_UPC01_CS_L
SWD_UPC_SWDIO0_JF202	SPI_UPC01_CLK
SWD_UPC_SWCLK_JF202	SPI_UPC01_MOSI
SPI_UPC01_MISO	SWD_UPC01_UART_CLK
I2C_UPC01_3V3_SDA	SWD_UPC01_UART_DATA
I2C_UPC01_3V3_SCL	PP1V25_S2

UART ACE

BOM_COST_GROUP=USB-C

ATCRTMR01_ACTIVE_READY_3V3 — NO_XNET_CONNECTION=1

RF290 100K 0201 5% 1/20W TK

USBC0_AUX_N — CF290 0.1UF 10% 6.3V CERM-X5R 0201 — USBC0_AUX_C_N

USBC0_AUX_P — CF291 0.1UF 10% 6.3V CERM-X5R 0201 — USBC0_AUX_C_P

RF292 33K 5% 1/20W TK 0201

RF293 33K 5% 1/20W TK 0201

RF291 100K 5% 1/20W TK 0201

ATCRTMR01_ACTIVE_READY_3V3 — NO_XNET_CONNECTION=1

RF298 100K 5% 1/20W TK 0201

USBC1_AUX_N — CF292 0.1UF 10% 6.3V CERM-X5R 0201 — USBC1_AUX_C_N

USBC1_AUX_P — CF293 0.1UF 10% 6.3V CERM-X5R 0201 — USBC1_AUX_C_P

RF296 33K 5% 1/20W TK 0201

RF297 33K 5% 1/20W TK 0201

RF299 100K 5% 1/20W TK 0201

HV POWER ALIASES

Fuses for laptop charging.

Desktops only need connection for programming OTP.

PACK_OPTION=USBC_LAPTOP

PACK_IGNORE=TRUE

PACK_OPTION=USBC_DESKTOP

CRITICAL 0603-1 FF200 6A-32V 740S00053

PPDCIN_USBC_AON — PPHV_INT0_AONSW

PLACE_NEAR=UF400:5MM

RF200 0 0% 1/20W TK 0201

PPHV_INT0_AONSW

CRITICAL 0603-1 FF201 6A-32V 740S00053

PPHV_INT1_AONSW

PLACE_NEAR=UF500:5MM

RF201 0 0% 1/20W TK 0201

PPHV_INT1_AONSW

PPVBUS_USBC0 — PPVBUS_USBC0

PPVBUS_USBC1 — PPVBUS_USBC1

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*** OK2INTEGRATE ***

UPC 0 is the Debug Port

ATC0 / UPC0 / RTMR0

UART_DEBUGPRT_R2D (IN) — MAKE_BASE=TRUE — UART_DEBUGPRT_R2D (IN)
UART_DEBUGPRT_D2R (OUT) — MAKE_BASE=TRUE — UART_DEBUGPRT_D2R (IN)
SWD_SOC_SWCLK (BI) — MAKE_BASE=TRUE — SWD_SOC_SWCLK (OUT)
SWD_SOC_SWDIO (BI) — MAKE_BASE=TRUE — SWD_SOC_SWDIO (OUT)
PD_UPC0_DBG_R — MAKE_BASE=TRUE — PD_UPC0_DBG_R (IN)

RF321 1/20W 5% 100K TK 0201 PD_UPC0_DBG_R
RF397 1/20W 5% 100K TK 0201 PD_UPC0_GPIO1 — MAKE_BASE=TRUE — PD_UPC0_GPIO1 (BI)
RF398 1/20W 5% 100K TK 0201 PD_UPC0_GPIO6 — MAKE_BASE=TRUE — PD_UPC0_GPIO6 (BI)

SOC_DFU_STATUS (IN) — MAKE_BASE=TRUE — SOC_DFU_STATUS (OUT)
SOC_FORCE_DFU (OUT) — MAKE_BASE=TRUE — SOC_FORCE_DFU (IN)
SOC_DOCK_CONNECT_DBG_UPC (OUT) — MAKE_BASE=TRUE — SOC_DOCK_CONNECT_DBG_UPC (IN)

UPC 1 GPIOs

CKPLUS_WAIVE=SINGLE_NODENET — ATC1 / UPC1 / RTMR1

RF320 1/20W 5% 100K TK 0201 PD_UPC1_DBG_R — MAKE_BASE=TRUE — PD_UPC1_DBG_R (BI) ×6
RF396 1/20W 5% 100K TK 0201 PD_UPC1_GPIO1 — MAKE_BASE=TRUE — PD_UPC1_GPIO1 (BI)
RF399 1/20W 5% 100K TK 0201 PD_UPC1_GPIO6 — MAKE_BASE=TRUE — PD_UPC1_GPIO6 (BI)
RF373 1/20W 5% 100K TK 0201 — SOC_DOCK_CONNECT_DUAL_KIS (IN)

PACK_OPTION=TADFU:YES — SOC_DFU_STATUS (OUT)
RF330 1/20W 5% 100K TK 0201 PD_UPC1_GPIO9 — MAKE_BASE=TRUE
PACK_IGNORE=TRUE PACK_OPTION=TADFU:NO

PACK_OPTION=TADFU:YES — SOC_FORCE_DFU (OUT)
RF331 1/20W 5% 100K TK 0201 PD_UPC1_GPIO10 — MAKE_BASE=TRUE
PACK_IGNORE=TRUE PACK_OPTION=TADFU:NO

on all nets above.

ATCRTMR Boot Config

[2:0] = [011] 30Mhz QSPI and Test Mode Enabled
POR config should be [010] Test Mode Disabed

RF380 10K 5% 1/20W TK 0201 ATCRTMR0_BOOT_CONFIG2 (OUT)
RF381 10K 5% 1/20W TK 0201 ATCRTMR0_BOOT_CONFIG1 (OUT) NOSTUFF
RF382 10K 5% 1/20W TK 0201 ATCRTMR0_BOOT_CONFIG0 (OUT) LFKA_TEST_MODE:NO

RF383 10K 5% 1/20W TK 0201 ATCRTMR1_BOOT_CONFIG2 (OUT)
RF384 10K 5% 1/20W TK 0201 ATCRTMR1_BOOT_CONFIG1 (OUT) NOSTUFF
RF385 10K 5% 1/20W TK 0201 ATCRTMR1_BOOT_CONFIG0 (OUT) LFKA_TEST_MODE:NO

LFKA_TEST_MODE:YES
RF386 10K 5% 1/20W TK 0201
RF387 10K 5% 1/20W TK 0201
RF388 10K NOSTUFF 5% 1/20W TK 0201 — PP1V2_USBC_VDDIO
ATCRTMR0_BOOT_CONFIG2 (OUT)
ATCRTMR0_BOOT_CONFIG1 (OUT)
ATCRTMR0_BOOT_CONFIG0 (OUT)

LFKA_TEST_MODE:YES
RF389 10K 5% 1/20W TK 0201
RF390 10K 5% 1/20W TK 0201
RF391 10K NOSTUFF 5% 1/20W TK 0201 — PP1V2_USBC_VDDIO
ATCRTMR1_BOOT_CONFIG2 (OUT)
ATCRTMR1_BOOT_CONFIG1 (OUT)
ATCRTMR1_BOOT_CONFIG0 (OUT)

Unused ports

RF31A 1/20W 5% 100K TK 0201 PD_UPC0_USBP3_RP — MAKE_BASE=TRUE — PD_UPC0_USBP3_RP (BI) ×2

BOMOPTION=USBC_DUAL_KIS:NO
RF328 1/20W 5% 100K TK 0201 USB_ATC1_DBG_LS_P (BI)
RF329 1/20W 5% 100K TK 0201 USB_ATC1_DBG_LS_N (BI)

RF32A 1/20W 5% 100K TK 0201 PD_UPC1_USBP3_RP — MAKE_BASE=TRUE — PD_UPC1_USBP3_RP (BI) ×2

KIS pack options for UPC1

PACK_OPTION=DUAL_KIS:YES
SOC_DOCK_CONNECT_DUAL_KIS (OUT) — MAKE_BASE=TRUE — SOC_DOCK_CONNECT_DUAL_KIS (IN)
USB_ATC1_DBG_LS_P (BI) — USB_ATC1_DBG_LS_P (BI)
USB_ATC1_DBG_LS_N (BI) — USB_ATC1_DBG_LS_N (BI)

ATCRTMR0 CHIP 0X00

PACK_OPTION=ATC_PU_PD:YES
RF392 10K 5% 1/20W TK 0201 ATCRTMR0_CHIPID_0 (OUT)
PACK_OPTION=ATC_PU_PD:NO
PACK_OPTION=ATC_PU_PD:YES
RF393 10K 5% 1/20W TK 0201 ATCRTMR_CHIPID_1 (OUT)
MAKE_BASE=TRUE
PACK_OPTION=ATC_PU_PD:NO

ATCRTMR1 CHIP 0X01

PP1V2_USBC_VDDIO
PACK_OPTION=ATC_PU_PD:YES
XWF300 SHORT-16L-0.1MM-SM
RF395 47K 5% 1/20W TK 0201
ATCRTMR1_CHIPID_0 (OUT)
PACK_IGNORE=TRUE
PACK_OPTION=ATC_PU_PD:NO

PACK_OPTION=ATC_PU_PD:YES
RF394 10K 5% 1/20W TK 0201 ATCRTMR1_CHIPID_1 (OUT)
MAKE_BASE=TRUE
PACK_OPTION=ATC_PU_PD:NO

Connections for Laptops (USBC power in)

PACK_OPTION=USBC_LAPTOP
PP3V3_UPC0_LDO (OUT) — MAKE_BASE=TRUE — PP3V3_UPC0_LDO (IN)
USBC0_CC1 (BI) — MAKE_BASE=TRUE — USBC0_CC1 (BI)
USBC0_CC2 (BI) — MAKE_BASE=TRUE — USBC0_CC2 (BI)

Connections for Desktops (No USBC power in)

PACK_OPTION=USBC_DESKTOP
MAKE_BASE=TRUE

Connections for Laptops (USBC power in)

PACK_OPTION=USBC_LAPTOP
PP3V3_UPC1_LDO (OUT) — MAKE_BASE=TRUE — PP3V3_UPC1_LDO (IN)
USBC1_CC1 (BI) — MAKE_BASE=TRUE — USBC1_CC1 (BI)
USBC1_CC2 (BI) — MAKE_BASE=TRUE — USBC1_CC2 (BI)

Connections for Desktops (No USBC power in)

PACK_OPTION=USBC_DESKTOP
MAKE_BASE=TRUE

USBC0 PP_CABLE Protection

PP3V3_UPC0_LDO — CF300 1.0UF 20% 6.3V X5R 0201-1
USBC0_VBIAS_PRT — CF301 0.1UF 10% 50V CERM-X7R 0402
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

UF300 TPD4S311A BGA 338S00753
NC_USBC0_CC_FLT_L (NO_TEST=1) — FLT*
USBC0_CC1 — CC1
USBC0_CC2 — CC2
C_SBU1, C_SBU2, C_CC1, C_CC2, RPD_G1, RPD_G2
USBC0_CC1_CONN (BI) — MAKE_BASE=TRUE
USBC0_CC2_CONN (BI) — MAKE_BASE=TRUE
PACK_OPTION=USBC_DESKTOP
PACK_OPTION=USBC_LAPTOP pack option for all component

USBC1 PP_CABLE Protection

PP3V3_UPC1_LDO — CF350 1.0UF 20% 6.3V X5R 0201-1
USBC1_VBIAS_PRT — CF351 0.1UF 10% 50V CERM-X7R 0402
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

UF350 TPD4S311A BGA 338S00753
NC_USBC1_CC_FLT_L (NO_TEST=1) — FLT*
USBC1_CC1 — CC1
USBC1_CC2 — CC2
C_SBU1, C_SBU2, C_CC1, C_CC2, RPD_G1, RPD_G2
USBC1_CC1_CONN (BI) — MAKE_BASE=TRUE
USBC1_CC2_CONN (BI) — MAKE_BASE=TRUE
PACK_OPTION=USBC_DESKTOP
PACK_OPTION=USBC_LAPTOP pack option for all component

ATC0: I2C_ADDR=GND, I2CM_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC1: I2C_ADDR=Float, I2CM_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC2: I2C_ADDR=GND, I2CM_*_CNFG=1M\u03a9 pull-downs
ATC3: I2C_ADDR=Float, I2CM_*_CNFG=1M\u03a9 pull-downs

GND (OUT) — MAKE_BASE=TRUE
NC_UPC1_I2C_ADDR (OUT) — MAKE_BASE=TRUE — NC_UPC1_I2C_ADDR NO_TEST=1

Configure to enable VDDIO and use it for SWD.
GND (OUT) — MAKE_BASE=TRUE
GND (OUT) — MAKE_BASE=TRUE

Is UPCx_5V_EN being used?

UPC01_5V_EN — RF350 100K 5% 1/20W TK 0201
UPC01_5V_EN — RF351 100K 5% 1/20W TK 0201
PACK_IGNORE=TRUE
PACK_OPTION=USBC01_VR5V_LOCAL_NO
BOM_COST_GROUP=USB-C

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	Apple Inc.
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*** OK2INTEGRATE ***

PP3V3_UPC0_LDO 69 70 71 113

Internal Pull-ups
Enabled after reading straps

RF409 470K 5% 1/20W TK 0201 — I2C_UPC0_ATCRTMR0_SCL 69 71 74 — CKPLUS_WAIVE=I2C_PULLUP
RF408 470K 5% 1/20W TK 0201 — I2C_UPC0_ATCRTMR0_SDA 69 71 74 — CKPLUS_WAIVE=I2C_PULLUP

RF405 1M 5% 1/20W TK 0201 — UART_UPC01_RX 69 71
RF406 100K 5% 1/20W TK 0201 — PD_UPC0_MRESET 71

Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

CRITICAL
RF403 15K 0.1% 1/20W TK 0201
GND_I2C_ADDR
PRIMARY ONLY

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

69 PPHV_INT0_AONSW

MAX 100uF TOTAL ON RAIL

128 72 PP5V_S2_UPC
128 72 PP5V_S2_UPC

CF406 138S00123 10UF 20% 10V X5R 0402

PP_5V0: K9 L10 M9 N10 K11 L12 M11 N12
PP_CABLE: N14 M13
PP_HV: G2 G4 H1 H3 J2 J4 K1 K3 L2 L4 M1 M3 M2 N4
VBUS: G6 G8 H5 H7 J6 J8 K5 K7 L6 L8 M5 M7 N6 N8

UF400
CD3217B13HACE
FCBGA
353S02993
CRITICAL
OMIT_TABLE

		B13	HRESET
71	PD_UPC0_MRESET	A14	MRESET
113 74 69 OUT	ATCRTMR0_RESET_L	B17	RESET* 3V3
113 69 OUT	UPC0_SER_DBG	A2	GPIO0 OUT,PP
		B1	
70 OUT	PD_UPC0_GPIO1	D1	GPIO1 BI,N_OD
69 67 IN	INT_I2C_UPC0_ATCRTMR0_L	F1	GPIO2 1V2 IN
130 70 OUT	UPC01_5V_EN	C2	GPIO3 3V3 OUT,P_OD
113 69 67 OUT	ATCRTMR0_FORCE_DFU	E2	GPIO4 1V2 OUT,PP
77 OUT	UPC0_CHGR_AUX_DET_SHORT	B3	GPIO5 3V3 OUT,P_OD
70 IN	PD_UPC0_GPIO6	C4	GPIO6 IN DIGITAL CORE I/O & CONTROL
70 OUT	SOC_DOCK_CONNECT_DBG_UPC	D3	GPIO7 OUT,P_OD
130 72 OUT	UPC_PMU_RESET_1V2_ACE2	E4	GPIO8 OUT,P_OD
70 IN	SOC_DFU_STATUS	F3	GPIO9 IN
70 OUT	SOC_FORCE_DFU	F7	GPIO10 OUT,P_OD
70	PP3V3_UPC0_LDO	A18	BUSPOWER
70	GND	M19	I2C_ADDR IPU-BOOT
	UPC0_R_OSC	M21	R_OSC
74 71 69 BI	I2C_UPC0_ATCRTMR0_SDA	A16	I2CM_SDA_CNFG IPU-AFTER-BOOT
74 71 69 BI	I2C_UPC0_ATCRTMR0_SCL	B15	I2CM_SCL_CNFG IPU-AFTER-BOOT
69 52 BI	I2C_UPC_SDA	B5	I2C_SDA1
69 52 BI	I2C_UPC_SCL	A4	I2C_SCL1
69 52 OUT	UPC_I2C_INT_L	D7	I2C_IRQ1*
69 54 BI	I2C_SMC_UPC_SDA	B7	I2C_SDA2
69 54 BI	I2C_SMC_UPC_SCL	A6	I2C_SCL2
69 54 OUT	UPC_SMC_I2C_INT_L	C8	I2C_IRQ2*
69 OUT	SPI_UPC01_R_CLK	B9	SPI_CLK
69 OUT	SPI_UPC01_R_MOSI	B11	SPI_MOSI
69 IN	SPI_UPC01_R_MISO	A10	SPI_MISO
69 OUT	SPI_UPC01_R_CS_L	A8	SPI_SSZ
69 BI	SWD_UPC_SWDIO0	E20	SWD_DATA IPU
69 BI	SWD_UPC_SWCLK	E16	SWD_CLK IPU
71 69 IN	UART_UPC01_RX	B19	UART_RX
69 OUT	UART_UPC01_TX	A20	UART_TX
77 BI	USB2_UPC0_P1_P	H19	USB_RP1_P
77 BI	USB2_UPC0_P1_N	H21	USB_RP1_N
130 BI	USB_ATC0_DBG_LS_P	G20	USB_RP2_P
130 BI	USB_ATC0_DBG_LS_N	G22	USB_RP2_N
70 BI	PD_UPC0_USBP3_RP	F19	USB_RP3_P
70 BI	PD_UPC0_USBP3_RP	F21	USB_RP3_N
69 BI	USBC0_AUX_C_P	J12	AUX_P
69 BI	USBC0_AUX_C_N	H11	AUX_N
69 OUT	PD_UPC0_HPD	C12	HPD
70 IN	UART_DEBUGPRT_R2D	G12	DEBUG0
70 OUT	UART_DEBUGPRT_D2R	F11	DEBUG1
70 OUT	SWD_SOC_SWCLK	E8	DEBUG2
70 BI	SWD_SOC_SWDIO	E12	DEBUG3
70 IN	PD_UPC0_DBG_R	G16	DEBUG4
70 OUT	PD_UPC0_DBG_R	F15	DEBUG5
74 BI	USBC0_CIO_LSTX_3V3	D15	DEBUG6
74 OUT	USBC0_CIO_LSRX_3V3	D19	DEBUG7

PORT_MUX

POWER

TYPE-C

GND

GND: A22 H9 N20 B21 K15 N22

PPVBUS_USBC0 66 69 113

CF401 1UF 10% 35V X5R 0402
DF400 DSN2 NSR20F40NX_G CRITICAL 371S00085

PP3V3_S2_LDO 69 72 126

CF400 10UF 20% 6.3V CERM 0402

PP1V25_S2 69 72 126

CF402 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3
PP3V3_UPC0_LDO 69 70 71 113

CF408 138S0801 10UF 20% 6.3V CERM 0402

PP1V8_S2 125

CF403 132S0444 0.1UF 10% 6.3V CERM-X5R 0201

UPC0_ATCRTMR01_PWR_EN 69 74 113
(cap needed when used as power source)

VIN_3V3	C20		
VDDIO	A12		
VDDIO_CFG	D11	GND	70
LDO_3V3	C22		
	D21		
VIN_LV	L20		
VOUT_LV	L18		
VRET	C16		
SS	L22	UPC0_SS	
LDO_CORE	E22	PP1V5_UPC0_LDO_CORE	113
VBUS_OPT	D5	PPVBUS_USBC0	69
PP_HV_OPT	F5	PPHV_INT0_AONSW	69
C_CC1	M15	USBC0_CC1	
	N16		
C_CC2	M17	USBC0_CC2	
	N18		
RPD_G1	L14	USBC0_CC1	BI 70
RPD_G2	L16	USBC0_CC2	BI 70
C_USB_TP	K19	USBC0_USB_TOP_P	BI 66 113
C_USB_TN	K21	USBC0_USB_TOP_N	BI 66 113
C_USB_BP	J20	USBC0_USB_BOT_P	BI 66
C_USB_BN	J22	USBC0_USB_BOT_N	BI 66
C_SBU1	J16	USBC0_SBU1	BI 66 113
C_SBU2	H15	USBC0_SBU2	BI 66 113

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
CF405 138S0801 10UF 20% 6.3V CERM 0402

PACK_OPTION=ACE2_SS_CAP
CF409 0.68UF 5% 6.3V X6S 0402
PACK_OPTION=ACE2_SS_GND
GND
MAKE_BASE=TRUE

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
70 BI

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
70 BI

CF414 131S00464 220PF 5% 50V C0G 0201-1
CF413 131S00464 220PF 5% 50V C0G 0201-1

GND_OPT	C18	
GND_OPT	E18	
GND_OPT	D17	
GND_OPT	G18	

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: Port Controller ATC0

Apple Inc.

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DRAWING NUMBER 051-07754 SIZE D
REVISION 6.0.0
BRANCH dvt-1
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*** OK2INTEGRATE ***

PP3V3_UPC1_LDO 69 70 72 113

1 470K 2 RF509 5% 1/20W TK 0201 I2C_UPC1_ATCRTMR1_SCL CKPLUS_WAIVE=I2C_PULLUP 69 72 74

1 470K 2 RF508 5% 1/20W TK 0201 I2C_UPC1_ATCRTMR1_SDA CKPLUS_WAIVE=I2C_PULLUP 69 72 74

1 1M 2 RF505 5% 1/20W TK 0201 UART_UPC01_TX 69 72

1 100K 2 RF506 5% 1/20W TK 0201 PD_UPC1_MRESET 72

Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

CRITICAL
RF503 1 15K 0.1% 1/20W TK 0201 2
GND_I2C_ADDR
PRIMARY ONLY

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

69 PPHV_INT1_AONSW

MAX 100uF TOTAL ON RAIL

128 71 PP5V_S2_UPC
128 71 PP5V_S2_UPC

138S00123
CF506 1 2 10UF 20% 10V X5R 0402

PP_5V0: K9 L10 M9 N10 K11 L12 M11 M12
PP_CABLE: N14 M13
PP_HV: G2 G4 H1 H3 J2 J4 K1 K3 L2 L4 M1 M3 M2 N4
VBUS: G6 G8 H5 H7 J6 J8 K5 K7 L6 L8 M5 M7 N6 N8

UF500
CD3217B13HACE
FCBGA

353S02993
CRITICAL
OMIT_TABLE

		B13	HRESET	
72	PD_UPC1_MRESET	A14	MRESET	
74 69 OUT	ATCRTMR1_RESET_L	B17	RESET* 3V3	
113 69 OUT	UPC1_SER_DBG	A2	GPIO0	OUT,PP
		B1		
70 OUT	PD_UPC1_GPIO1	D1	GPIO1	BI,N_OD
69 68 IN	INT_I2C_UPC1_ATCRTMR1_L	F1	GPIO2	1V2 IN
130 70 OUT	UPC01_5V_EN	C2	GPIO3	3V3 OUT,P_OD
68 OUT	ATCRTMR1_FORCE_DFU	E2	GPIO4	1V2 OUT,PP
77 OUT	UPC1_CHGR_AUX_DET_SHORT	B3	GPIO5	3V3 OUT,P_OD
70 IN	PD_UPC1_GPIO6	C4	GPIO6	IN DIGITAL CORE I/O & CONTROL
70 OUT	SOC_DOCK_CONNECT_DUAL_KIS	D3	GPIO7	OUT,P_OD
130 71 OUT	UPC_PMU_RESET_1V2_ACE2	E4	GPIO8	OUT,P_OD
70 IN	SOC_DFU_STATUS	F3	GPIO9	IN
70 OUT	SOC_FORCE_DFU	F7	GPIO10	OUT,P_OD
70	PP3V3_UPC1_LDO	A18	BUSPOWER	
70	NC_UPC1_I2C_ADDR	M19	I2C_ADDR	IPU-BOOT
	UPC1_R_OSC	M21	R_OSC	
74 72 69 BI	I2C_UPC1_ATCRTMR1_SDA	A16	I2CM_SDA_CNFG	IPU-AFTER-BOOT
74 72 69 BI	I2C_UPC1_ATCRTMR1_SCL	B15	I2CM_SCL_CNFG	IPU-AFTER-BOOT
52 BI	I2C_UPC_SDA	B5	I2C_SDA1	
52 BI	I2C_UPC_SCL	A4	I2C_SCL1	
52 OUT	UPC_I2C_INT_L	D7	I2C_IRQ1*	
54 BI	I2C_SMC_UPC_SDA	B7	I2C_SDA2	
54 BI	I2C_SMC_UPC_SCL	A6	I2C_SCL2	
54 OUT	UPC_SMC_I2C_INT_L	C8	I2C_IRQ2*	
69 OUT	GND	B9	SPI_CLK	
69 OUT	GND	B11	SPI_MOSI	
69 IN	GND	A10	SPI_MISO	
69 OUT	GND	A8	SPI_SSZ	
69 BI	SWD_UPC01_UART_DATA	E20	SWD_DATA	IPU
69 BI	SWD_UPC01_UART_CLK	E16	SWD_CLK	IPU
72 69 IN	UART_UPC01_TX	B19	UART_RX	
69 OUT	UART_UPC01_RX	A20	UART_TX	
77 BI	USB2_UPC1_P1_P	H19	USB_RP1_P	
77 BI	USB2_UPC1_P1_N	H21	USB_RP1_N	
130 70 BI	USB_ATC1_DBG_LS_P	G20	USB_RP2_P	
130 70 BI	USB_ATC1_DBG_LS_N	G22	USB_RP2_N	
70 BI	PD_UPC1_USBP3_RP	F19	USB_RP3_P	
70 BI	PD_UPC1_USBP3_RP	F21	USB_RP3_N	
69 BI	USBC1_AUX_C_P	J12	AUX_P	
69 BI	USBC1_AUX_C_N	H11	AUX_N	
69 OUT	PD_UPC1_HPD	C12	HPD	
70 BI	PD_UPC1_DBG_R	G12	DEBUG0	
70 BI	PD_UPC1_DBG_R	F11	DEBUG1	
70 OUT	PD_UPC1_DBG_R	E8	DEBUG2	
70 BI	PD_UPC1_DBG_R	E12	DEBUG3	
70 BI	PD_UPC1_DBG_R	G16	DEBUG4	
70 BI	PD_UPC1_DBG_R	F15	DEBUG5	
74 BI	USBC1_CIO_LSTX_3V3	D15	DEBUG6	
74 OUT	USBC1_CIO_LSRX_3V3	D19	DEBUG7	

PORT_MUX

POWER

TYPE-C

GND

GND
A22 H9 N20 B21 K15 N22

PPVBUS_USBC1 66 69 113

CF501 1 2 1UF 20% 35V X5R 0402

DF500 DSN2 NSR20F40NX_G CRITICAL 371S00085 (K A)

PP3V3_S2_LDO 69 71 126

138S0801
CF500 1 2 10UF 20% 6.3V CERM 0402

PP1V25_S2 69 71 126

CF502 1 2 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V
PP3V3_UPC1_LDO 69 70 72 113

138S0801
CF508 1 2 10UF 20% 6.3V CERM 0402

PP1V8_S2 125

132S0444
CF503 1 2 0.1UF 10% 6.3V CERM-X5R 0201

UPC1_ATCRTMR01_PWR_EN 69 74 113
(cap needed when used as power source)

VIN_3V3	C20		
VDDIO	A12		
VDDIO_CFG	D11	GND	70
LDO_3V3	C22		
	D21		
VIN_LV	L20		
VOUT_LV	L18		
VRET	C16		
SS	L22	UPC1_SS	
LDO_CORE	E22 113	PP1V5_UPC1_LDO_CORE	
VBUS_OPT	D5	PPVBUS_USBC1	69
PP_HV_OPT	F5	PPHV_INT1_AONSW	69
C_CC1	M15	USBC1_CC1	BI 70
	N16		
C_CC2	M17	USBC1_CC2	BI 70
	N18		
RPD_G1	L14	USBC1_CC1	BI 70
RPD_G2	L16	USBC1_CC2	BI 70
C_USB_TP	K19	USBC1_USB_TOP_P	BI 66
C_USB_TN	K21	USBC1_USB_TOP_N	BI 66
C_USB_BP	J20	USBC1_USB_BOT_P	BI 66
C_USB_BN	J22	USBC1_USB_BOT_N	BI 66
C_SBU1	J16	USBC1_SBU1	BI 66 113
C_SBU2	H15	USBC1_SBU2	BI 66 113
GND_OPT	C18		
GND_OPT	E18		
GND_OPT	D17		
GND_OPT	G18		

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
138S0801
CF505 1 2 10UF 20% 6.3V CERM 0402

PACK_OPTION=ACE2_SS_CAP
CF509 1 2 0.68UF 5% 6.3V X6S 0402
PACK_OPTION=ACE2_SS_GND
GND
MAKE_BASE=TRUE

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

131S00464
CF514 1 2 220PF 5% 50V C0G 0201-1
131S00464
CF513 1 2 220PF 5% 50V C0G 0201-1

BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C: Port Controller ATC1
	Apple Inc.
DRAWING NUMBER	051-07754
SIZE	D
REVISION	6.0.0
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*** OK2INTEGRATE ***

MACAW 0

PP1V25_S2
CF612 1.0UF 20% 6.3V X5R 0201-1
CF613 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF600.A4:5MM
PLACE_NEAR=UF600.A4:5MM

PP1V8_S2
CF604 0.1UF 10% 10V X5R-CERM 0201
CF602 0.1UF 10% 10V X5R-CERM 0201
CF603 4.7UF 20% 4V CER-X5R 0201
CF600 1.0UF 20% 6.3V X5R 0201-1
CF615 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF600.B5:5MM
PLACE_NEAR=UF600.B5:5MM
PLACE_NEAR=UF600.B5:5MM
PLACE_NEAR=UF600.B5:5MM
PLACE_NEAR=UF600.B5:5MM

PP1V1_MACAW0_VCCD
VOLTAGE=1.1V
CF606 4.7UF 20% 6.3V X6S 0402

PP3V3_S2_LDO
CF607 0.1UF 10% 10V X5R-CERM 0201
CF608 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF600.C6:5MM
PLACE_NEAR=UF600.C6:5MM

UF600
CYUSB2405A2
CSP
338S00851
VCCD VDDD VDDIO VDD3V3

BOMOPTION=MACAW_I2C_MASK
VREFB_ATC0
QF601 NTNS4CS69N XDFN SYM_VER_2 376S00282
PP1V25_S2
RF603 47K 5% 1/20W TK 0201
BOMOPTION=MACAW_I2C_MASK

ATCRTMR0_RESET_1V2_L → RESET*
OMIT_TABLE
CRITICAL
INT I2C_EUSBLS0_L → INT
I2C_UPC0_RTMR0_EUSB0_SDA_1V2 → SDA
I2C_UPC0_RTMR0_EUSB0_SCL_1V2 → SCL
EUSB_ATC0_P → EDP0
EUSB_ATC0_N → EDN0
EUSB_ATC0_DBG_P → EDP1
EUSB_ATC0_DBG_N → EDN1
CROSS
TST_MACAW0_DEBUG_SWDCLK → GPIO_0/SWDCLK
TST_MACAW0_DEBUG_SWDDAT → GPIO_1/SWDDAT
VSS VSSQ

DP0 USB2_ATC0_LS_P
DN0 USB2_ATC0_LS_N
DP1 USB_ATC0_DBG_LS_P
DN1 USB_ATC0_DBG_LS_N

BOMOPTION=USBC_DUAL_KIS:NO
PLACE_NEAR=UF690.1:2MM
EUSB_DBG_P — RF690 0 1/20W 0% TK 0201 — EUSB_ATC0_DBG_P
EUSB_DBG_N — RF691 0 1/20W 0% TK 0201 — EUSB_ATC0_DBG_N
NO_XNET_CONNECTION=1
PLACE_NEAR=UF690.2:2MM

PP3V3_S2_LDO
CF690 1.0UF 20% 6.3V X5R 0201-1
BOMOPTION=USBC_DUAL_KIS:YES
NO_XNET_CONNECTION=1
UF690 CRITICAL TMUXHS221 UQFN 353S03251
EUSB_DBG_P ↔ EUSB_ATC0_DBG_P
EUSB_DBG_N ↔ EUSB_ATC0_DBG_N
EUSB_ATC1_DBG_P
EUSB_ATC1_DBG_N
SOC_DOCK_CONNECT_DUAL_KIS → SEL
OE* GND
100k PD on the support page

LOW --> UPC0 Default KIS
HIGH --> UPC1 KIS

XIP MACAW0_CLK24M_IN
XOP MACAW0_CLK24M_OUT_R
RF600 0 1/20W 0% TK 0201
MACAW0_CLK24M_OUT
YF600 1.60X1.20MM 197S0591
CRITICAL CF611 9.5PF +/-0.1PF 50V CER-C0G 0201 131S00077
CRITICAL 131S00077 CF610 9.5PF +/-0.1PF 50V CER-C0G 0201
RESREF MACAW0_RESREF
RF601 6.04K 1% 1/20W TK 0201

MACAW 1

PP1V25_S2
CF662 1.0UF 20% 6.3V X5R 0201-1
CF663 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF650.A4:5MM
PLACE_NEAR=UF650.A4:5MM

PP1V8_S2_USBLS1_ISNS
CF654 0.1UF 10% 10V X5R-CERM 0201
CF651 0.1UF 10% 10V X5R-CERM 0201
CF652 4.7UF 20% 4V CER-X5R 0201
CF653 1.0UF 20% 6.3V X5R 0201-1
CF665 1.0UF 20% 6.3V X5R 0201-1
138S00138
PLACE_NEAR=UF650.B5:5MM
PLACE_NEAR=UF650.B5:5MM
PLACE_NEAR=UF650.B5:5MM
PLACE_NEAR=UF650.B5:5MM
PLACE_NEAR=UF650.B5:5MM

PP1V1_MACAW1_VCCD
VOLTAGE=1.1V
CF656 4.7UF 20% 6.3V X6S 0402

PP3V3_S2SW_USBLS1_ISNS
CF657 0.1UF 10% 10V X5R-CERM 0201
CF658 1.0UF 20% 6.3V X5R 0201-1
PLACE_NEAR=UF650.C6:5MM
PLACE_NEAR=UF650.C6:5MM

UF650
CYUSB2405A2
CSP
338S00851
VCCD VDDD VDDIO VDD3V3

BOMOPTION=MACAW_I2C_MASK
VREFB_ATC1
QF651 NTNS4CS69N XDFN SYM_VER_2 376S00282
PP1V25_S2
RF653 47K 5% 1/20W TK 0201
BOMOPTION=MACAW_I2C_MASK

ATCRTMR1_RESET_1V2_L → RESET*
OMIT_TABLE
CRITICAL
INT I2C_EUSBLS1_L → INT
I2C_UPC1_RTMR1_EUSB1_SDA_1V2 → SDA
I2C_UPC1_RTMR1_EUSB1_SCL_1V2 → SCL
EUSB_ATC1_P → EDP0
EUSB_ATC1_N → EDN0
EUSB_ATC1_DBG_P ↔ EUSB_ATC1_DBG_P → EDP1
EUSB_ATC1_DBG_N ↔ EUSB_ATC1_DBG_N → EDN1
PACK_OPTION=DUAL_KIS:YES
CROSS
TST_MACAW1_DEBUG_SWDCLK → GPIO_0/SWDCLK
TST_MACAW1_DEBUG_SWDDAT → GPIO_1/SWDDAT
VSS VSSQ

DP0 USB2_ATC1_LS_P
DN0 USB2_ATC1_LS_N
DP1 USB_ATC1_DBG_LS_P ↔ USB_ATC1_DBG_LS_P
DN1 USB_ATC1_DBG_LS_N ↔ USB_ATC1_DBG_LS_N
PACK_OPTION=DUAL_KIS:YES
PACK_OPTION=DUAL_KIS:YES

BOMOPTION=USBC_DUAL_KIS:NO
RF697 0 1/20W 0% TK 0201
SOC_DOCK_CONNECT_DBG_UPC → SOC_DOCK_CONNECT

PP1V25_S2
BOMOPTION=USBC_DUAL_KIS:YES
CF695 0.1UF 10% 10V X5R-CERM 0201
UF695 PACK_IGNORE=TRUE PACK_OPTION=USBC_GATE_PACKAGE:XSON SN74AUP1G32 X2SON 311S00275
RF695 0 1/20W 0% TK 0201
SOC_DOCK_CONNECT_DUAL_KIS → SOC_DOCK_CONNECT_DUAL_KIS_R
SOC_DOCK_CONNECT
SOC_DOCK_CONNECT_DBG_UPC
RF696 100K 5% 1/20W TK 0201
NOSTUFF CF696 0.1UF 10% 10V X5R-CERM 0201
BOMOPTION=USBC_DUAL_KIS:YES
PP1V25_S2
UF695 SN74AUP1G32 SOT553 311S00301
PACK_OPTION=USBC_GATE_PACKAGE:SOT

XIP MACAW1_CLK24M_IN
XOP MACAW1_CLK24M_OUT_R
RF650 0 1/20W 0% TK 0201
MACAW1_CLK24M_OUT
YF660 1.60X1.20MM 197S0591
CRITICAL CF661 9.5PF +/-0.1PF 50V CER-C0G 0201 131S00077
CRITICAL 131S00077 CF660 9.5PF +/-0.1PF 50V CER-C0G 0201
RESREF MACAW1_RESREF
RF651 6.04K 1% 1/20W TK 0201

BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C: USB2 RPT
	Apple Inc.
DRAWING NUMBER	051-07754
SIZE	D
REVISION	6.0.0
BRANCH	dvt-1
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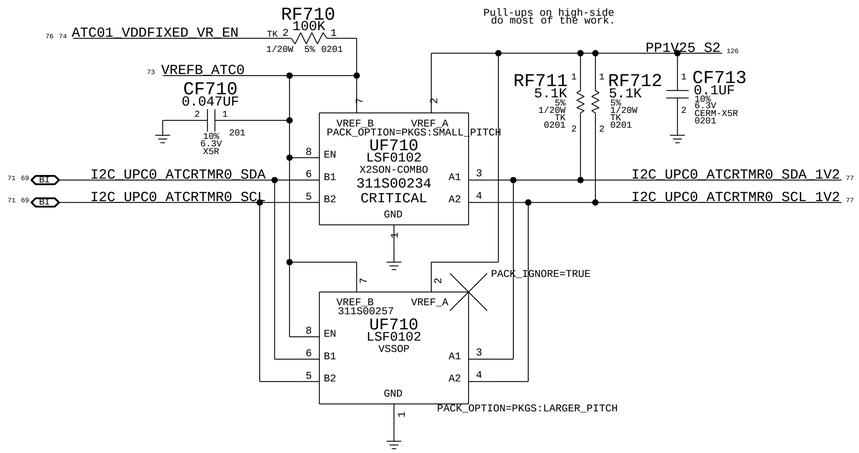
*** OK2INTEGRATE ***

Sequencing Requirements: 3.3V to UF790 --> system 1.2V (UF710,UF720) same time or before system 1.8V (UF400&UF500 VIN_LV pin)

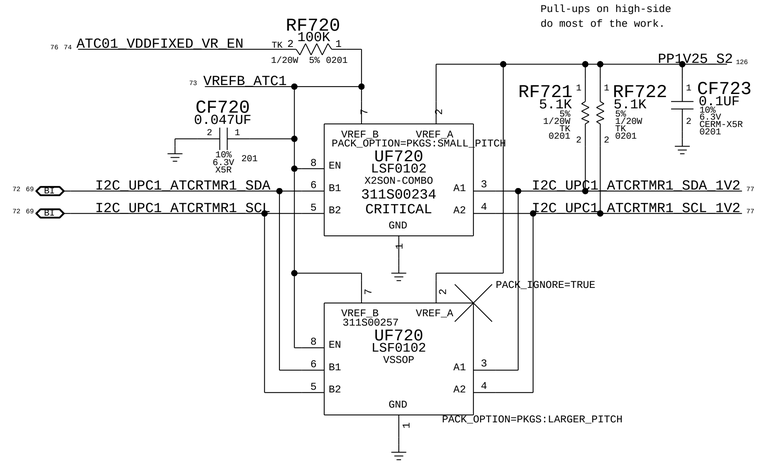
Power-up Sequence Requirements: 3.3_S2 to UF790 --> system 1.2V (UF710,UF720) same time or before system 1.8V (UF400&UF500 VIN_LV pin)

Power-down Sequence Requirements: The 1.8V first or at the same time as 1V2 --> 3V3_S2 needs to get disabled at minimum of 6ms from when 1V8 is discharged to below 300mV

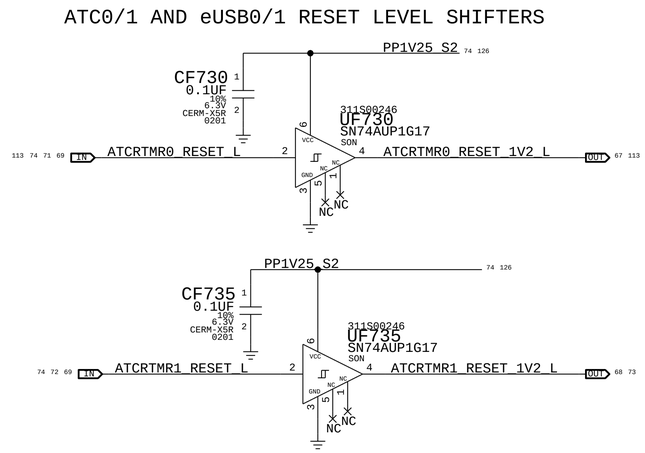
ATC0 RE-TIMER I2C LEVEL SHIFTERS



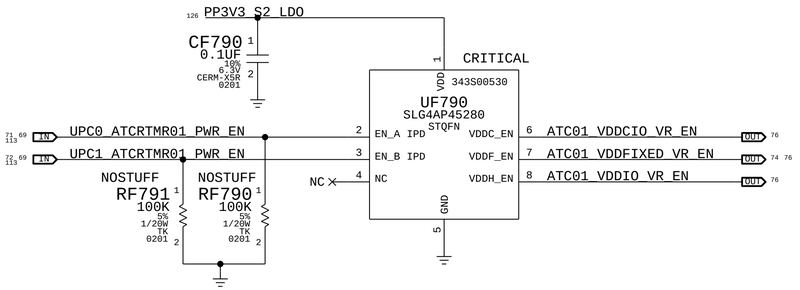
ATC1 RE-TIMER I2C LEVEL SHIFTERS



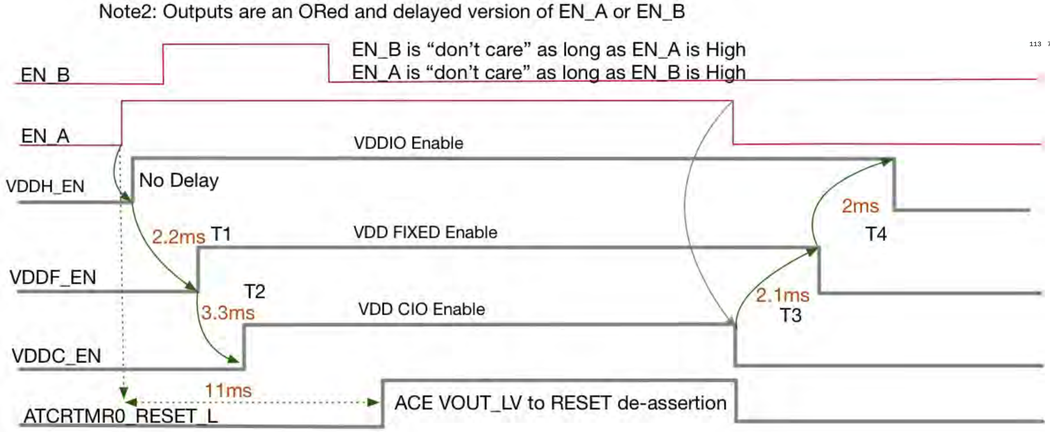
ATC0/1 AND eUSB0/1 RESET LEVEL SHIFTERS

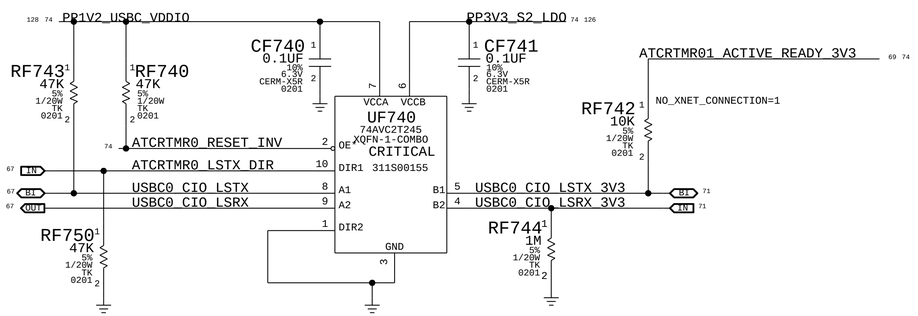


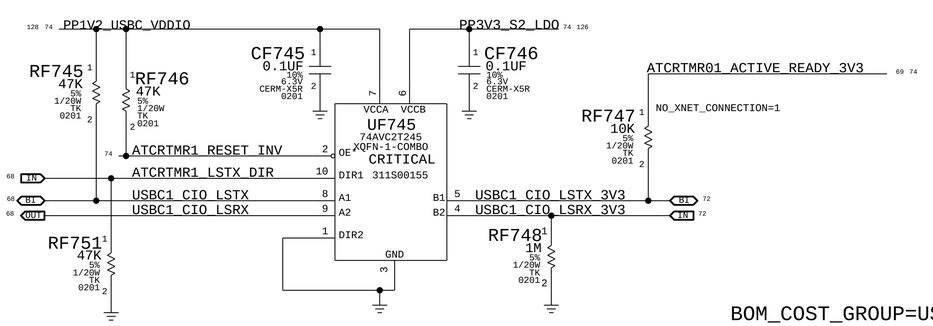
The 3.3V needs to be HIGH before VIN_LV of ACEs



Note1: As long as EN_A or EN_B are High, the outputs stay High
Note2: Outputs are an ORed and delayed version of EN_A or EN_B







BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: HS Level Shifters

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*** OK2INTEGRATE ***

SET ONE OPTION FOR THE PBUS CAPS

PACK_OPTION=5VUSBC01_PBUS-B12
PACK_OPTION=5VUSBC01_PBUS-D2
PACK_OPTION=5VUSBC01_PBUS-D12
PACK_OPTION=5VUSBC01_PBUS-18V

SET ONE OPTION FOR UF800

PACK_OPTION=5VUSBC01_THINSTNCL
PACK_OPTION=5VUSBC01_THICKSTNCL

SET ONE OPTION FOR UF840 BUFFER

PACK_OPTION=5VUSBC01_AND:PP
PACK_OPTION=5VUSBC01_AND:OD

Vout=5.23V
EDC=6.6A
F=1.5MHz
START UP TIME < 15 MS

3.3V tolerant I/O
Vih = 0.78 - 3.3V
Vil = 0 - 0.42V
@ VCC = 1.2V

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: 5V Regulator

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*** OK2INTEGRATE ***

D

PP1V2_USBC_VDDIO 69 76 128
NOSTUFF
RF904 4.7K 5% 1/20W TK 0201
P1V2_ATC01_PGOOD 76

XWF901 SM
129 PP3V8_AON_ATC_ISNS
NO_XNET_CONNECTION=1
VOLTAGE=3.8V MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000
CRITICAL CF902 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF903 10UF 20% 6.3V CER-X6S 0402-COMBO
PP3V8_ACT01_VDDIO_REG
CRITICAL CF904 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF905 10UF 20% 6.3V CER-X6S 0402-COMBO

XWF902 SM
P1V2_ATC01_SVR_PGND
VOLTAGE=0V NO_XNET_CONNECTION=1 PLACE_NEAR=UF900.8:2MM
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

152S00984
CRITICAL LF900 0.47UH-3.7A-0.034OHM
DIDT=TRUE SWITCH_NODE=TRUE PIJB16140H-SM
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

UF900 TPS628502 SOT583 353S02660
VIN EN MODE_SYNC PG COMP_FSET GND SW FB
76 74 IN ATC01_VDDIO_VR_EN
RF909 0 TK 1/20W 0% 0201
ATC01_VDDIO_VR_EN_R
P1V2_ATC01_SW
P1V2_ATC01_FB_RC
76 P1V2_ATC01_PGOOD
P1V2_ATC01_COMP_FSET
RF901 100K 1% 1/20W TK 0201
RF900 100K 1% 1/20W TK 0201
CF906 100PF 5% 50V C0G 0201
RF910 3.16K 1% 1/20W TK 0201
P1V2_ATC01_AGND 76
P1V2_ATC01_FB_TOP_R
RF905 10 5% 1/20W TK 0201
XWF903 SM NO_XNET_CONNECTION=1
XWF904 SM NO_XNET_CONNECTION=1
XWF900 SM VOLTAGE=0V NO_XNET_CONNECTION=1 PLACE_NEAR=UF900.8:2MM
76 P1V2_ATC01_AGND
<Rb> RF908 15K 0.1% 1/20W TK 0201
P1V2_ATC01_FB
<Ra> RF907 15K 0.1% 1/20W TK 0201
P1V2_ATC01_FB_R
RF906 316 TK 1% 1/20W 0201
CF901 3300PF 10% 10V X7R-CERM 0201
P1V2_ATC01_FB_TOP

Vout = 1.213V
Iout Max = 0.96A
F = 1.8 MHZ

CRITICAL CF908 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF909 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF910 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF911 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF912 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF913 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF914 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF915 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF916 10UF 20% 6.3V CER-X6S 0402-COMBO
138S00073
CRITICAL CF917 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF918 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF919 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF920 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF921 10UF 20% 6.3V CER-X6S 0402-COMBO
PP1V2_USBC_VDDIO 69 76 128

128 76 69 PP1V2_USBC_VDDIO
RF911 10 5% 1/5W TK 0402
RF912 10 5% 1/5W TK 0402
RF913 10 5% 1/5W TK 0402
P1V2_ATC01_DSCHG
129 76 PP3V8_AON_ATC_ISNS
117S00095
RF914 100K 5% 1/20W TK 0201
QF910 SSM6N37FEAP SOT563 376S00078
76 74 IN ATC01_VDDIO_VR_EN
ATC01_P1V2_DSCHG_EN_RC

C

PP1V2_USBC_VDDIO 69 76 128
NOSTUFF
RF934 4.7K 5% 1/20W TK 0201
P0V855_ATC01_PGOOD 76

XWF931 SM NO_XNET_CONNECTION=1
129 PP3V8_AON_ATC_ISNS
VOLTAGE=3.8V MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000
CRITICAL CF932 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF933 10UF 20% 6.3V CER-X6S 0402-COMBO
PP3V8_ACT01_VDDCIO_REG
CRITICAL CF934 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF935 10UF 20% 6.3V CER-X6S 0402-COMBO

XWF932 SM
P0V855_ATC01_SVR_PGND
VOLTAGE=0V NO_XNET_CONNECTION=1 PLACE_NEAR=UF930.8:2MM
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

152S00984
CRITICAL LF930 0.47UH-3.7A-0.034OHM
DIDT=TRUE SWITCH_NODE=TRUE PIJD16140H-SM
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

UF930 TPS628502 SOT583 353S02660
VIN EN MODE_SYNC PG COMP_FSET GND SW FB
76 74 IN ATC01_VDDCIO_VR_EN
RF939 0 TK 1/20W 0% 0201
ATC01_VDDCIO_VR_EN_R
P0V855_ATC01_SW
P0V855_ATC01_FB_RC
76 P0V855_ATC01_PGOOD
P0V855_ATC01_COMP_FSET
RF931 100K 1% 1/20W TK 0201
RF930 100K 1% 1/20W TK 0201
CF936 100PF 5% 50V C0G 0201
RF940 3.16K 1% 1/20W TK 0201
P0V855_ATC01_AGND 76
P0V855_ATC01_FB_TOP_R
RF935 10 5% 1/20W TK 0201
XWF933 SM NO_XNET_CONNECTION=1
XWF934 SM NO_XNET_CONNECTION=1
XWF930 SM VOLTAGE=0V NO_XNET_CONNECTION=1 PLACE_NEAR=UF930.8:2MM
76 P0V855_ATC01_AGND
<Rb> RF938 27.4K 0.1% 1/20W TK 0201
P0V855_ATC01_FB
<Ra> RF937 10K 0.1% 1/20W TK 0201
P0V855_ATC01_FB_R
RF936 1.96K 1% 1/20W TK 0201
CF931 3300PF 10% 10V X7R-CERM 0201
P0V855_ATC01_FB_TOP

Vout = 0.8621V
Iout Max = 0.5A
F = 1.8 MHZ

PP0V855_USBC_CIO
CRITICAL CF938 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF939 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF940 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF941 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF942 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF943 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF944 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF945 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF946 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF947 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF948 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF949 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF950 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF951 10UF 20% 6.3V CER-X6S 0402-COMBO
69 76 128

128 76 69 PP0V855_USBC_CIO
RF941 10 5% 1/5W TK 0402
RF942 10 5% 1/5W TK 0402
RF943 10 5% 1/5W TK 0402
P0V855_ATC01_DSCHG
129 76 PP3V8_AON_ATC_ISNS
117S00095
RF944 100K 5% 1/20W TK 0201
QF940 SSM6N37FEAP SOT563 376S00078
76 74 IN ATC01_VDDCIO_VR_EN
ATC01_P0V855_DSCHG_EN_RC
CF959 4700PF CER-X5R 10% 25V 0201-1
132S00390

B

PP1V2_USBC_VDDIO 69 76 128
NOSTUFF
RF964 4.7K 5% 1/20W TK 0201
P0V805_ATC01_PGOOD 76

XWF961 SM NO_XNET_CONNECTION=1
129 PP3V8_AON_ATC_ISNS
VOLTAGE=3.8V MIN_NECK_WIDTH=0.1000 MIN_LINE_WIDTH=0.2000
CRITICAL CF962 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF963 10UF 20% 6.3V CER-X6S 0402-COMBO
PP3V8_ACT01_VDDFIXED_REG
CRITICAL CF964 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF965 10UF 20% 6.3V CER-X6S 0402-COMBO

XWF962 SM
P0V805_ATC01_SVR_PGND
VOLTAGE=0V NO_XNET_CONNECTION=1 PLACE_NEAR=UF960.8:2MM
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

152S00984
CRITICAL LF960 0.47UH-3.7A-0.034OHM
DIDT=TRUE SWITCH_NODE=TRUE PHJB16140H-SM
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

UF960 TPS628502 SOT583 353S02660
VIN EN MODE_SYNC PG COMP_FSET GND SW FB
76 74 IN ATC01_VDDFIXED_VR_EN
RF969 0 TK 1/20W 0% 0201
ATC01_VDDFIXED_VR_EN_R
P0V805_ATC01_SW
P0V805_ATC01_FB_RC
76 P0V805_ATC01_PGOOD
P0V805_ATC01_COMP_FSET
RF961 100K 1% 1/20W TK 0201
RF960 100K 1% 1/20W TK 0201
CF966 100PF 5% 50V C0G 0201
RF970 3.16K 1% 1/20W TK 0201
P0V805_ATC01_AGND 76
P0V805_ATC01_FB_TOP_R
RF965 10 5% 1/20W TK 0201
XWF964 SM NO_XNET_CONNECTION=1
XWF963 SM NO_XNET_CONNECTION=1
XWF960 SM VOLTAGE=0V NO_XNET_CONNECTION=1 PLACE_NEAR=UF960.8:2MM
76 P0V805_ATC01_AGND
<Rb> RF968 30.9K 0.1% 1/20W TK 0201
P0V805_ATC01_FB
<Ra> RF967 10K 0.1% 1/20W TK 0201
P0V805_ATC01_FB_R
RF966 665 TK 1% 1/20W 0201
CF961 3300PF 10% 10V X7R-CERM 0201
P0V805_ATC01_FB_TOP

PP0V805_USBC_FIXED
CRITICAL CF968 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF969 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF970 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF971 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF972 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF973 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF974 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF975 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF976 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF977 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF978 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF979 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF980 10UF 20% 6.3V CER-X6S 0402-COMBO
CRITICAL CF981 10UF 20% 6.3V CER-X6S 0402-COMBO
76 128

128 76 PP0V805_USBC_FIXED
RF971 10 5% 1/5W TK 0402
RF972 10 5% 1/5W TK 0402
RF973 10 5% 1/5W TK 0402
P0V805_ATC01_DSCHG
129 76 PP3V8_AON_ATC_ISNS
117S00095
RF974 100K 5% 1/20W TK 0201
QF960 SSM6N37FEAP SOT563 376S00078
76 74 IN ATC01_VDDFIXED_VR_EN
ATC01_P0V805_DSCHG_EN_RC

BOM_COST_GROUP=TBT

PAGE TITLE
USB-C: ATC01 REGULATORS

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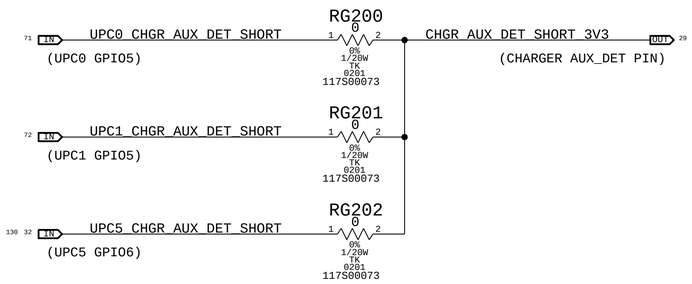
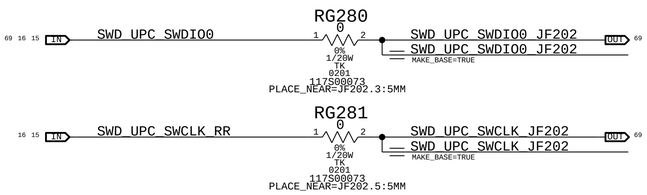
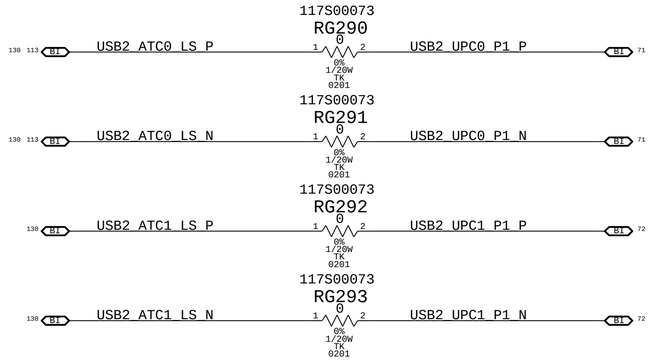
CHARGER AUX DET CONNECTIONS
<RDAR://70072178>
ALLOW ACE TO SEND A SIGNAL TO CHARGER
TO BLOCK SYSTEM CURRENT THROUGH ACE2 FETS DURING ACE2 SOFT START



SERIES R TO JF202



USB2 CMC PLACEHOLDERS <RDAR://88642736>

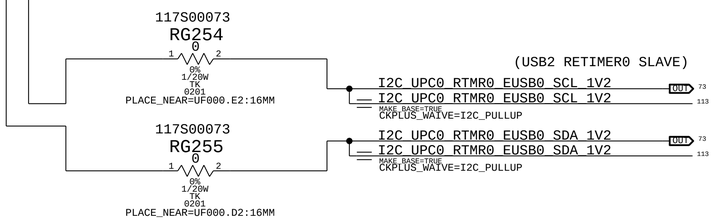


PORT 0 ACE/RTMR I2C

DEVICE	7-BIT
RT13 0	0X18
USB2 RTMR 0	0X21

(UPC0 MASTER)
(LEVEL SHIFTED FROM 3V3)

(ATC RETIMER0 SLAVE)

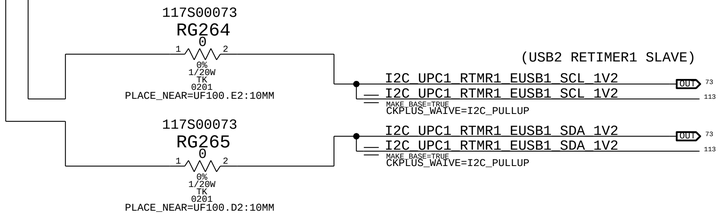


PORT 1 ACE/RTMR I2C

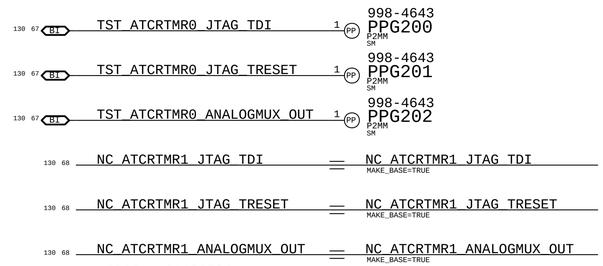
DEVICE	7-BIT
RT13 1	0X18
USB2 RTMR 1	0X21

(UPC1 MASTER)
(LEVEL SHIFTED FROM 3V3)

(ATC RETIMER1 SLAVE)

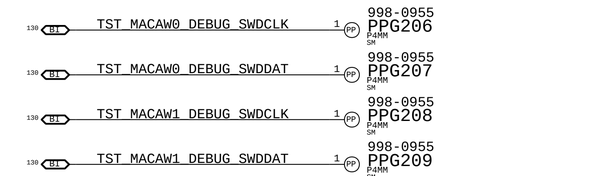


0.2MM PROBE POINTS FOR DEBUG ACCESS



<RDAR://91130524>

0.4MM PROBE POINTS FOR DEBUG ACCESS



BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C: PROJECT SUPPORT

Apple Inc.

DRAWING NUMBER 051-07754
SIZE D
REVISION 6.0.0
BRANCH dvt-1
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THIS PAGE NOT SYNCED (FOLLOWING X2371 WHICH ALSO HAD TO BREAK SYNC)
TO ADD CORRECT CONNECTOR RDAR://88448603

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0077	377S0183		DZH505	

HDMI CONNECTOR
THRU-HOLE
JH500
RCPT-HDMI-ACC-BLK-X1982
F-RT-TH

514S00360
SHLD PINS
OMIT_TABLE

155S0831
FLH500
600-OHM-25%-1.3A-0.15OHM
0603

377S0183
DZH505
5.5V-6.2PF
0201-THICKSTNCL

138S0683 CH512 1UF 10% 25V X5R 402
132S0288 CH511 0.1UF 10% 16V X5R-CERM 0201
132S0288 CH515 0.1UF 10% 16V X5R-CERM 0201

132S0288 CH514 0.1UF 10% 16V X5R-CERM 0201
131S0445 CH516 12PF 5% 25V NP0-C0G 0201
131S0439 CH517 3.0PF +/-0.1PF 25V NP0-C0G 0201
131S0198 CH518 1.8PF +/-0.1PF 25V C0G 201

138S0641
CH513
2.2UF
20%
10V
X5R-CERM
402
NOSTUFF

376S00636
QH502
NOSTUFF
NTZD3155C
SOT-563-HF
P-CHN

117S00095
RH524
100K
5%
1/20W
TK
0201
NOSTUFF

117S00090
RH523
10K
5%
1/20W
0201
NOSTUFF

117S00132
RH508
560
5%
1/20W
TK
0201
NOSTUFF

376S00636
QH502
NOSTUFF
NTZD3155C
SOT-563-HF
N-CHN

CEC ISOLATION FET INCLUDED FOR INITIAL HARDWARE, THOUGH LIKELY NOT REQUIRED

371S0695
DH507
NSR0620P2XXG
SOD-923-HF

RH528
0
0% 1/20W TK 0201
117S00073

376S00282
CRITICAL
QH500
NTNS4CS69N
XDFN

VTH=0.6-1.2V
376S1128 CHANGES TO 376S00282
PER <RDAR://59164333>

UH502
FPF2495C
CSP
CRITICAL
ON
VOUT
ISET
OCFLAGB
GND
VIN

353S01211
OVERCURRENT PROTECTION

PCA ENABLED
R_SET = 2.32K 1%
405 MA MIN
450 MA TYP
495 MA MAX
<RDAR://98840453>

118S00784
RH526
2.32K
1%
1/20W
TK
0201

117S00099
RH506
2.2K
5%
1/20W
TK
0201

117S00099
RH505
2.2K
5%
1/20W
TK
0201

TPH501
TP-P4

117S00087
RH527
4.7K
5%
1/20W
0201

LH504
FERR-470-OHM
155S0387
0201
CRITICAL

LH501
FERR-470-OHM
155S0387
0201
CRITICAL

LH502
FERR-470-OHM
155S0387
0201
CRITICAL

LH503
FERR-470-OHM
155S0387
0201
CRITICAL

NOSTUFF CH504 22PF 5% 25V C0G 0201

NOSTUFF CH505 18PF 5% 25V C0G 0201

NOSTUFF CH506 18PF 5% 25V C0G 0201

RH507
0
0% 1/20W
117S00073

RH509
33
5% 1/20W
117S00122

RH510
33
5% 1/20W
117S00122

RH511
0
0% 1/20W
117S00073

LH501-4 PRIMARY APN CHANGE: RDAR://92546959

377S00031 DZH503 ESD8011 X3DFN2-THICKSTNCL CRITICAL
377S00031 DZH502 ESD8011 X3DFN2-THICKSTNCL CRITICAL
377S00031 DZH501 ESD8011 X3DFN2-THICKSTNCL CRITICAL
377S00031 DZH500 ESD8011 X3DFN2-THICKSTNCL CRITICAL

132S0212 CH507 220PF 10% 16V X7R-CERM 201

376S0636
QH501
NTZD3155C
SOT-563-HF
P-CHN
CRITICAL

DATA_FILT CH508 0.1UF 10% 6.3V CERM-X5R 0201 132S0444
DATA_FILT RH512 100K 5% 1/20W TK 0201 117S00095
DATA_FILT RH513 10K 5% 1/20W TK 0201 117S00090
DATA_FILT CH509 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

PIND_PFET_EN

376S0636
QH501
NTZD3155C
SOT-563-HF
N-CHN
CRITICAL

DATA_FILT RH514 100K 5% 1/20W TK 0201 117S00095

VTH = 0.5V - 1V MAX

DP2HDMI_1.5G_FILT_EN	PIN DIODE	FILTER
LOW	UNBIASED	
HI	BIASED	

371S00062
DH504
X3DFN2-THICKSTNCL
NSR01L30MXT5G

117S00121
RH515
27K
5%
1/20W
TK
0201
NOSTUFF

CEC_FLT_PULL

CEC_FLT
NOSTUFF
RH516
10M
5%
1/20W
TK
0201
117S00146

371S0695
DH505
NSR0620P2XXG
SOD-923-HF

118S00398
RH517
3M
1%
1/20W
TK
0201-1
NOSTUFF

HDMI_CEC_PULL

HDMI_CEC
NOSTUFF
RH518
10M
5%
1/20W
TK
0201
117S00146

* ALL PINS OF IC'S, COMPONENTS, AND CONNECTORS ASSOCIATED WITH ANY HIGH-SPEED NET HAS PROPERTY: GND_VOID=TRUE TO VOID GND PLANE UNDERNEATH.

BOM_COST_GROUP=HDMI

PAGE TITLE: HDMI: CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-07754
SIZE: D
REVISION: 6.0.0
BRANCH: dvt-1
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*** OK2INTEGRATE***

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8	7	6	5	4	3	2	1

CL FILT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S00850	8	IND,0.5NH,+/-0.1NH,0.85A,0.080HM,0201	LH600,LH601,LH603,LH604,LH606,LH607,LH609,LH610	HDMI_CL_FILT:YES
117S00073	8	RES,TK,0.0OHM,1,1/20W,0201,HIGHFREQ	LH600,LH601,LH603,LH604,LH606,LH607,LH609,LH610	HDMI_CL_FILT:NO

BOM_COST_GROUP=HDMI

PAGE TITLE: HDMI: DESENSE FILTERS

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REVISION: 6.0.0

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*** IN PROGRESS ***

OMIT_TABLE

UH700
PS190-A1
BGA
338S00957

PP3V3_DP2HDMI
VOLTAGE=3.3V

PP1V2_DP2HDMI
VOLTAGE=1.2V

PP0V95_DP2HDMI_VDDTX
VOLTAGE=0.95V

PP0V95_DP2HDMI_VDDRX
VOLTAGE=0.95V

PP0V95_DP2HDMI_VDDA
VOLTAGE=0.95V

PACK_IGNORE=TRUE
PACK_OPTION=HDMI14UF:THICK

PACK_OPTION=HDMI14UF:NORM

SW GPIO TPS PER <RDAR://74536924>,<RDAR://79172907>,<RDAR://77622534>

NOTE: PMU AND SAK MUST BE OD (VDD 1V8) FOR RESET TO HAVE 1V2 PU

BOMOPTION=COBRAPART:1

BOMOPTION=COBRAPART:0

DESKTOPS WITH >1 COBRA:USE COBRAPART:1 TO DIFFERENTIATE WITH I2C ADDRESS

PORTABLES: COBRAPART:0

VIEW YOUR SOC ARCHITECTURE FOR I2C HOOKUP

MUST BE HOOKED UP TO SOC

NET/TP NOT USED ON POR PROGRAMS

CKPLUS_WAIVE=SINGLE_NODENET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00772	1	IC,COBRA,PS190,DP2 TO HDMI,A0,BGA120	UH700	CRITICAL	COBRA-A0
338S00957	1	IC,COBRA,PS190,DP2 TO HDMI,A1,BGA120	UH700	CRITICAL	COBRA-A1_CGF2
998-29948	1	IC,COBRA,A1,DP TO HDMI CNVTR,DEV,BGA120	UH700	CRITICAL	COBRA-A1_CGF1

BOM_COST_GROUP=HDMI

PAGE TITLE
HDMI: COBRA

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*** IN PROGRESS ***

LPDP AC Caps

From SOC

To HDMI

LPDP_DP2HDMI_DATA_C_N<0>	CH820 0.1UF	132S0444	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<0>
LPDP_DP2HDMI_DATA_C_P<0>	CH821 0.1UF	132S0444	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<0>
LPDP_DP2HDMI_DATA_C_N<1>	CH822 0.1UF	132S0444	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<1>
LPDP_DP2HDMI_DATA_C_P<1>	CH823 0.1UF	132S0444	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<1>
LPDP_DP2HDMI_DATA_C_N<2>	CH824 0.1UF	132S0444	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<2>
LPDP_DP2HDMI_DATA_C_P<2>	CH825 0.1UF	132S0444	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<2>
LPDP_DP2HDMI_DATA_C_N<3>	CH826 0.1UF	132S0444	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_N<3>
LPDP_DP2HDMI_DATA_C_P<3>	CH827 0.1UF	132S0444	GND_VOID=TRUE 10% 6.3V CERM-X5R 0201	DPRX_DATA_P<3>
LPDP_DP2HDMI_AUX_C_N	CH828 0.1UF	132S0444	10% 6.3V CERM-X5R 0201	DPRX_AUX_N
LPDP_DP2HDMI_AUX_C_P	CH829 0.1UF	132S0444	10% 6.3V CERM-X5R 0201	DPRX_AUX_P

DP2HDMI_RESET_L → RH801 0 (0% 1/20W TK 0201 117S00073) → DP2HDMI_RESET_R_L

THIS SHORTS PMU TO SAK CONTROL

HDMI ROM BOM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0915	1	IC,SRL SPI FLASH ROM,4MBIT,50MHZ,USON8	UH701	HDMI_ROM:512
335S00133	1	IC,SPI SERIAL FLASH,4MBITS,3.0V,USON8	UH701	HDMI_ROM:1M
341S02145	1	ROM,HDMI,CBR (V02.55.00) P1-A/B,X2293	UH701	HDMI_ROM:2_55
341S02214	1	ROM,HDMI (V02.59.00) PRE-EVT,X2267	UH701	HDMI_ROM:2_59

USE APN:341 ROM OPTIONS
APN:335 ARE BASE BLANK PARTS

LEVEL SHIFTERS

PP1V25_S2 → CH842 0.1UF (132S0444); NO_XNET_CONNECTION=1 → RH822 30K (118S00521)

PP3V3_AWAKESW_DP2HDMI → UH840 311S00337 SN74AXC1T45-S SOT-5X3 (VCCA VCCB, DIR, GND) → CH841 0.1UF (132S0444)

SPI_DP2HDMI_HOLD_L → A → B → SPI_DP2HDMI_HOLD_L_3V3

PP3V3_S2_LDO → CH802 0.1UF (132S0288)

UH802 SN74LVC1G07 SON (311S0536): HDMI_HPD_IN → HDMI_AOP_HPD_R; NC

PP1V25_S2 → RH803 30K (118S00521) NOSTUFF → RH804 100 (118S00250) → HDMI_HPD_AOP

PP1V25_S2 → CH801 0.1UF (132S0288); NO_XNET_CONNECTION=1 → RH815 30K (118S00521)

UH801 SN74AUP2G07 SON (311S00285): HDMI_CEC_AOP_TX → RH806 0 (117S00073) → AOP_HDMI_CEC_R; CEC_FLT_R → RH810 187 (118S00361) → CEC_FLT

NO_XNET_CONNECTION=1 → RH816 27K (117S00121)

AOP_HDMI_CEC_R → RH805 100 (118S00250) → HDMI_CEC_AOP_RX

CONNECT THIS NET TO 5V_S2_MAIN

PLACE THIS NEAR 5V_S2_MAIN.VR.OUTPUT
PLACE_NEAR=CH917:10mm
XWH801 SM
PP5V_S2_HOLD → PP5V_S2_HOLD_HDMI_LDO
VOLTAGE=5

THIS IS USED FOR CONTROLLING HDMI PORT POWER VIA THE PMU SYS ALIVE NET

USE THE BYPASS BOMOPTION OR PACK_OPTION TO STUFF AND-GATE CIRCUIT
USE THE HDMI_SAK:INSTALL PACK OPTION TO USE THE SAK

PACK_OPTION=HDMI_SAK:BYPASS
BOMOPTION=HDMI_SAK:BYPASS
PP1V8_S2 → CH805 0.1UF (132S0444)

UH805 SN74AUP1G08 USON (311S00306): PMU_SYS_ALIVE_1V8, DP2HDMI_PWR_EN_PMU → DP2HDMI_PWR_EN_R; NC

PACK_OPTION=HDMI_SAK:BYPASS
BOMOPTION=HDMI_SAK:BYPASS
RH807 0 (117S00073) → DP2HDMI_PWR_EN_ANDGATE-OUTPUT

RH808 0 (117S00073) NOSTUFF
PACK_OPTION=HDMI_SAK:BYPASS

INTEGRATORS NEED TO UPDATE UPSTREAM
PMU GPIO NETNAMES TO ACCOMODATE THIS ENABLE NET

SAK BYPASS OPTIONS (INCLUDING RESET ABOVE)
THESE REQUIRE UH805 OR RH809 TO BE STUFFED

DP2HDMI_PWR_EN_ANDGATE-OUTPUT → RH811 0 (117S00073) → P0V95_HDMI_EN
CH807 0.1UF (132S0444) PACK_OPTION=HDMI_SAK:BYPASS BOMOPTION=HDMI_SAK:BYPASS

RH812 0 (117S00073): P1V2_HDMI_PWR_EN
CH808 0.1UF (132S0444) PACK_OPTION=HDMI_SAK:BYPASS BOMOPTION=HDMI_SAK:BYPASS

RH813 0 (117S00073): P3V3_HDMI_PWR_EN
CH809 0.1UF (132S0444) PACK_OPTION=HDMI_SAK:BYPASS BOMOPTION=HDMI_SAK:BYPASS

THIS SAK IS USED FOR COBRA POWER SEQUENCING

***PLEASE REFER TO NOTE1 ON CSA2 FOR PROPER SIGNAL NAMING OF "PP1V8_HDMI_PWR_SEQ"

PP1V8_S2 → CH806 0.1UF (132S0444)

UH806 SLG4AP45256 STQFN 343S00528 (VDD, GND): PACK_OPTION=HDMI_SAK:INSTALL

PMU_SYS_ALIVE_1V8	SYS_ACTIVE	DISCHARGE_EN	P0V95_DSCHG_EN_RC
DP2HDMI_PWR_EN_PMU	HDMI_ENABLE	PP0V95V_EN	P0V95_HDMI_EN
NC_UH805_5	NC	PP1V2_EN	P1V2_HDMI_PWR_EN
NC_UH805_11	NC	PP3V3_EN	P3V3_HDMI_PWR_EN
		RESETB	DP2HDMI_RESET_R_L
		RESETB_2	NC_UH805_6

SAK HAS AND GATE BUILT IN

RH908/RH909 intended for potential
resistor divider need after AND gate

BOM_COST_GROUP=HDMI

PAGE TITLE: HDMI: Project Support 1

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DRAWING NUMBER: 051-07754 SIZE: D
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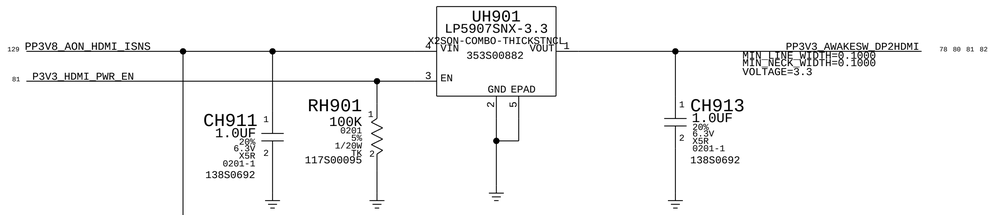
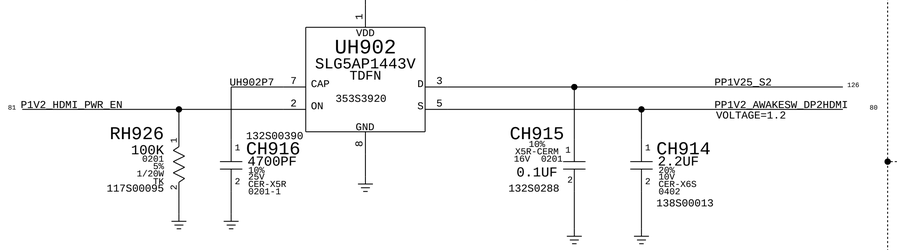
3.3V LDO

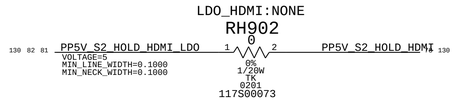


1.2V LOAD SW

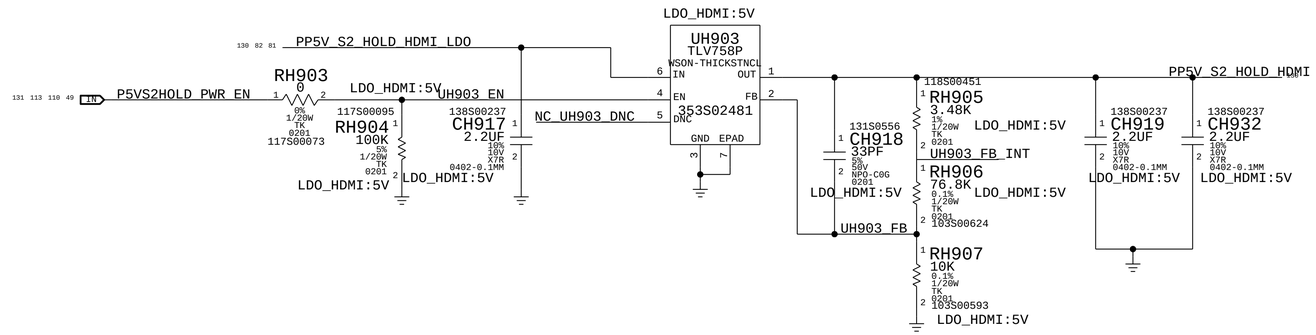


THIS IS USED FOR LONGER 5V POWER PATHS TO ENSURE GOOD 5V REGULATION

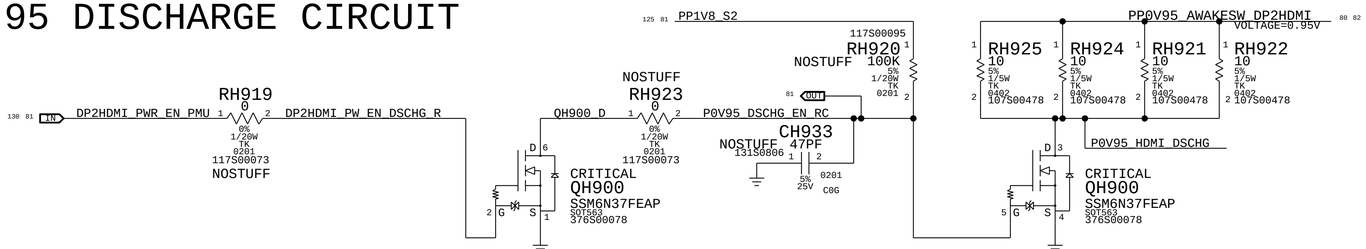
Enable BOMOPTION LDO_HDMI:NONE to disable the LDO use



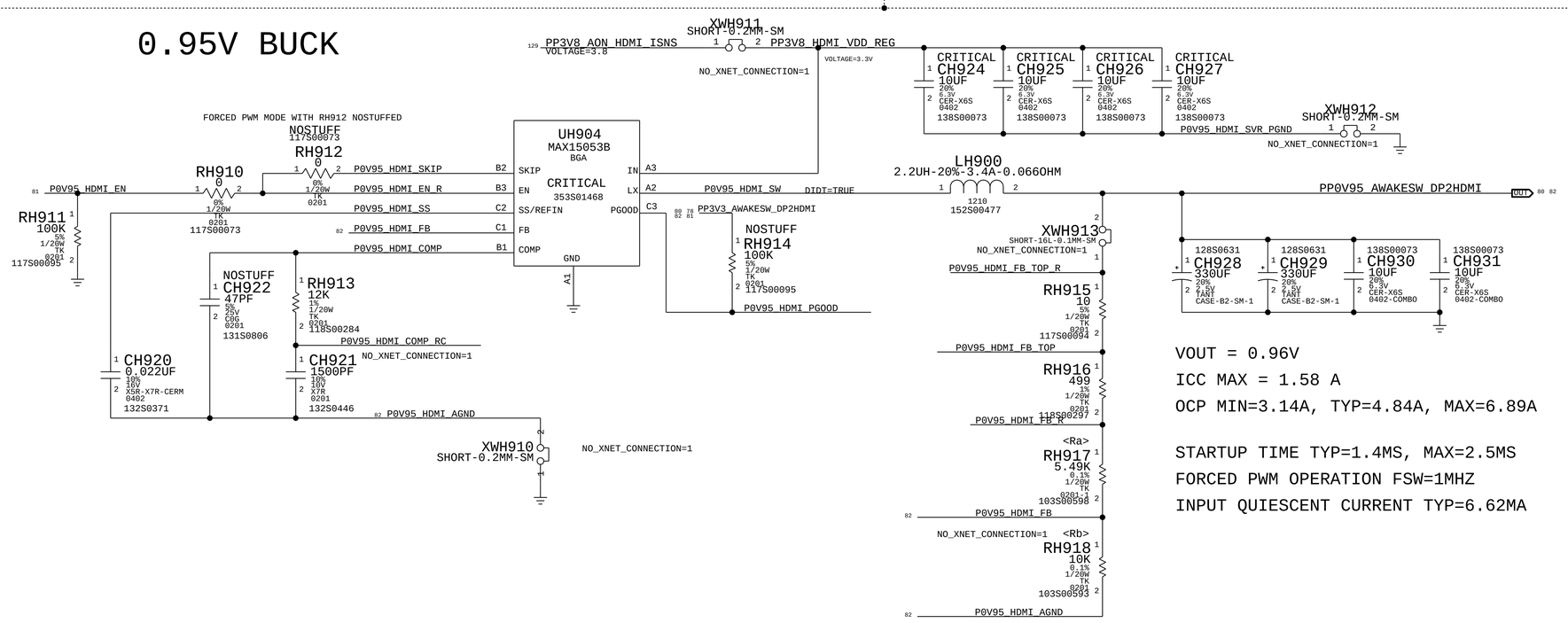
Enable BOMOPTION LDO_HDMI:5V to test HDMI 5V limit to 5.3V



0.95 DISCHARGE CIRCUIT



0.95V BUCK



VOUT = 0.96V

ICC MAX = 1.58 A

OCP MIN=3.14A, TYP=4.84A, MAX=6.89A

STARTUP TIME TYP=1.4MS, MAX=2.5MS

FORCED PWM OPERATION FSW=1MHZ

INPUT QUIESCENT CURRENT TYP=6.62MA

PAGE TITLE: HDMI: Project Support 2

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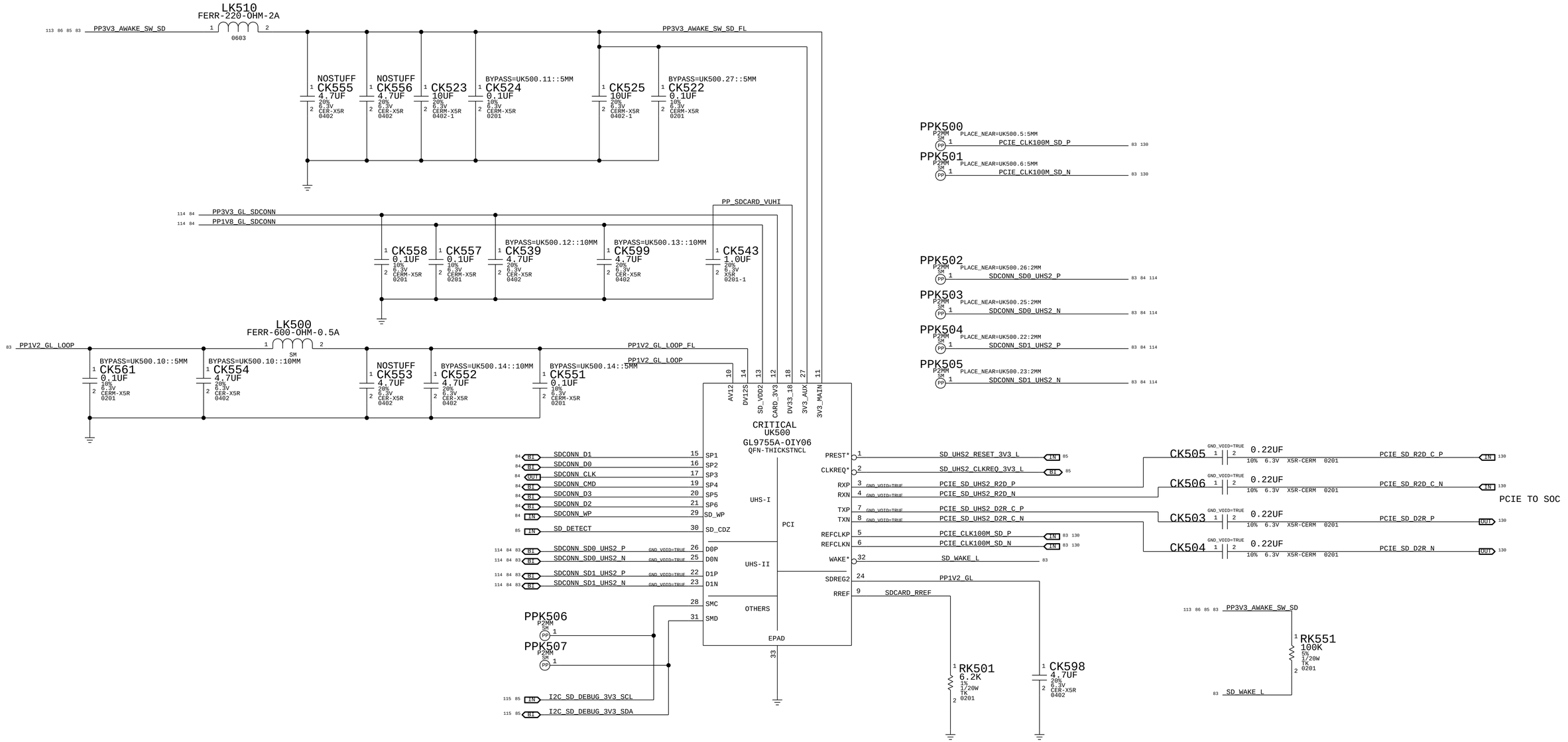

PAGE TITLE
SDCARD CONTROLLER

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SD CARD CONNECTOR
514-00196

CONN. FOR J314 USED AS REF. ONLY
CHECK CONN. FOR YOUR SPECIFIC PROJECT
INTEGRATORS, PLEASE HAVE SEPARATE BOM TABLE FOR JK600

THE BYPASS CAPS
SHOULD BE PLACED AS CLOSE AS POSSIBLE
TO THE PINS OF THE CONNECTOR

OMIT_TABLE
JK600
RCPT-BLK-SHIFT-SD-X1982
F-RT-TH

	SD MODE	PCIE MODE
1	CD/DAT3	PERST*
2	CMD	NU
3	VSS1	VSS1
4	VDD	VDD1
5	CLK	NU
6	VSS2	VSS2
7	DAT0	REFCLK+
8	DAT1	REFCLK-
9	DAT2	CLKREQ*
10	NU	VSS3
11	NU	PCIE TX+
12	NU	PCIE TX-
13	NU	VSS4
14	NU	VDD2
15	NU	PCIE RX-
16	NU	PCIE RX+
17	NU	VSS5
18	NU	VDD3
19	WP SWITCH	WP SWITCH
20	INS DET SW	INS DET SW
21	SHIELD	
22	SHIELD	
23	SHIELD	
24	SHIELD	
25	SHIELD	
26	SHIELD	
27	SHIELD	
28	SHIELD	
29	SHIELD	
30	SHIELD	
31	SHIELD	

BOM_COST_GROUP=SDCARD

PAGE TITLE: SDCARD CONNECTOR

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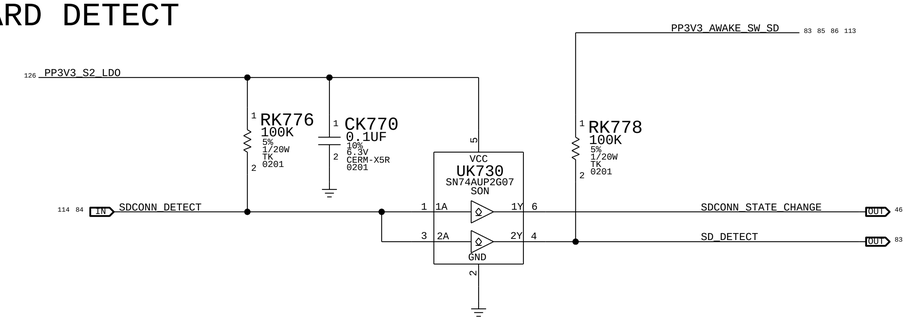
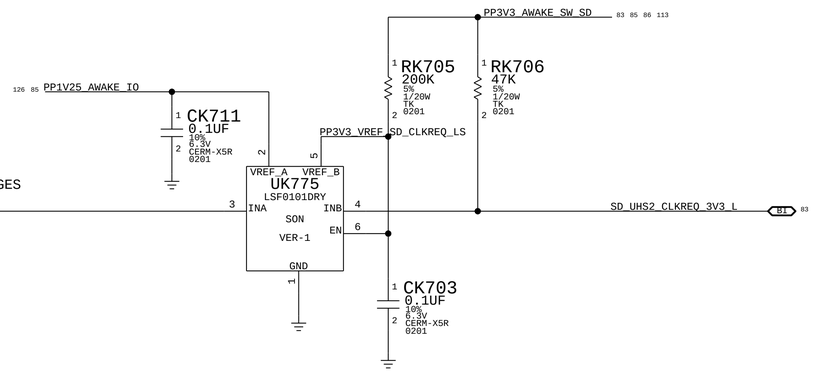
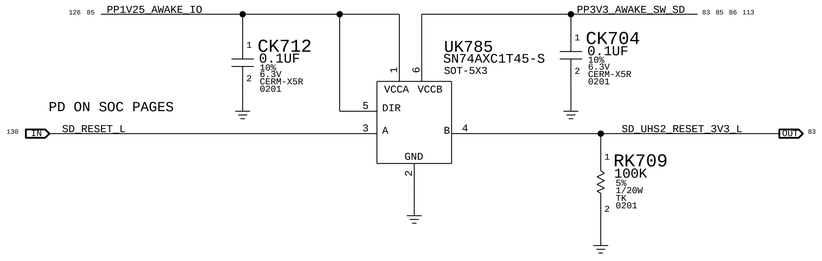
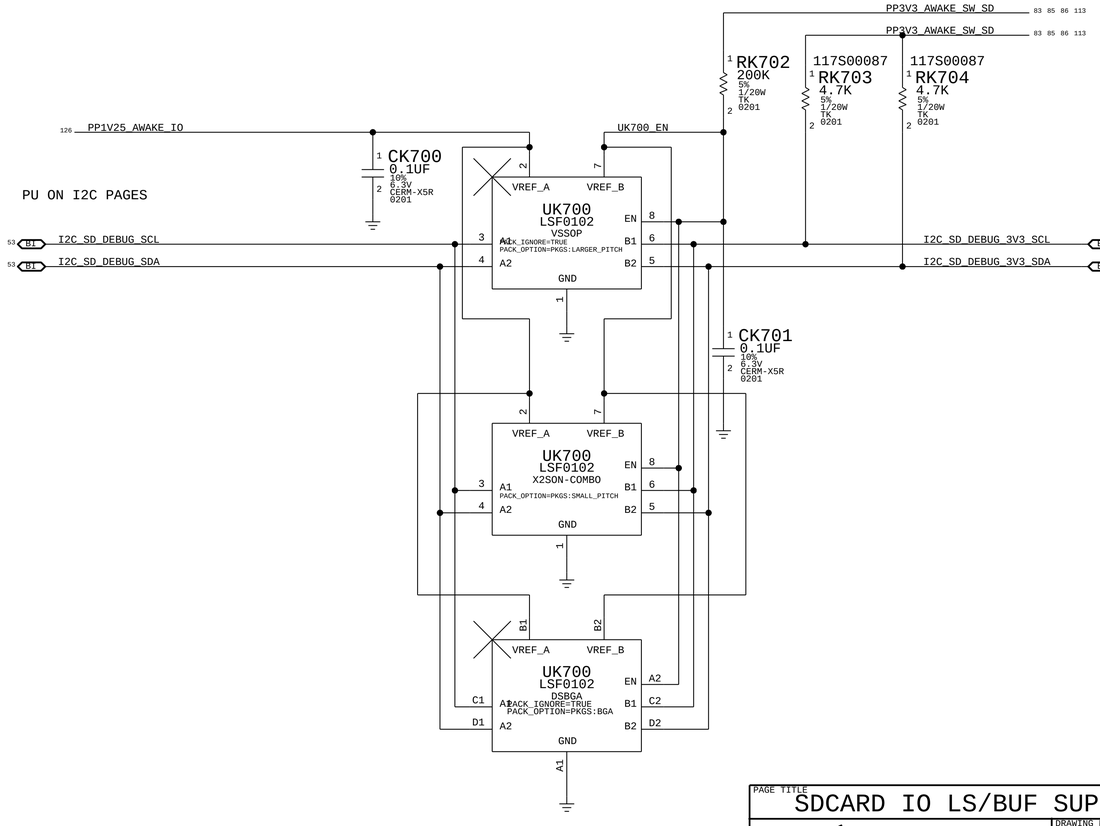
CARD DETECT



CONTROLLER IO







BOM_COST_GROUP=SDCARD

PAGE TITLE
SDCARD IO LS/BUF SUPPORT

Apple Inc.

DRAWING NUMBER 051-07754 SIZE D
REVISION 6.0.0
BRANCH dvt-1
PAGE 197 OF 999
SHEET 85 OF 147

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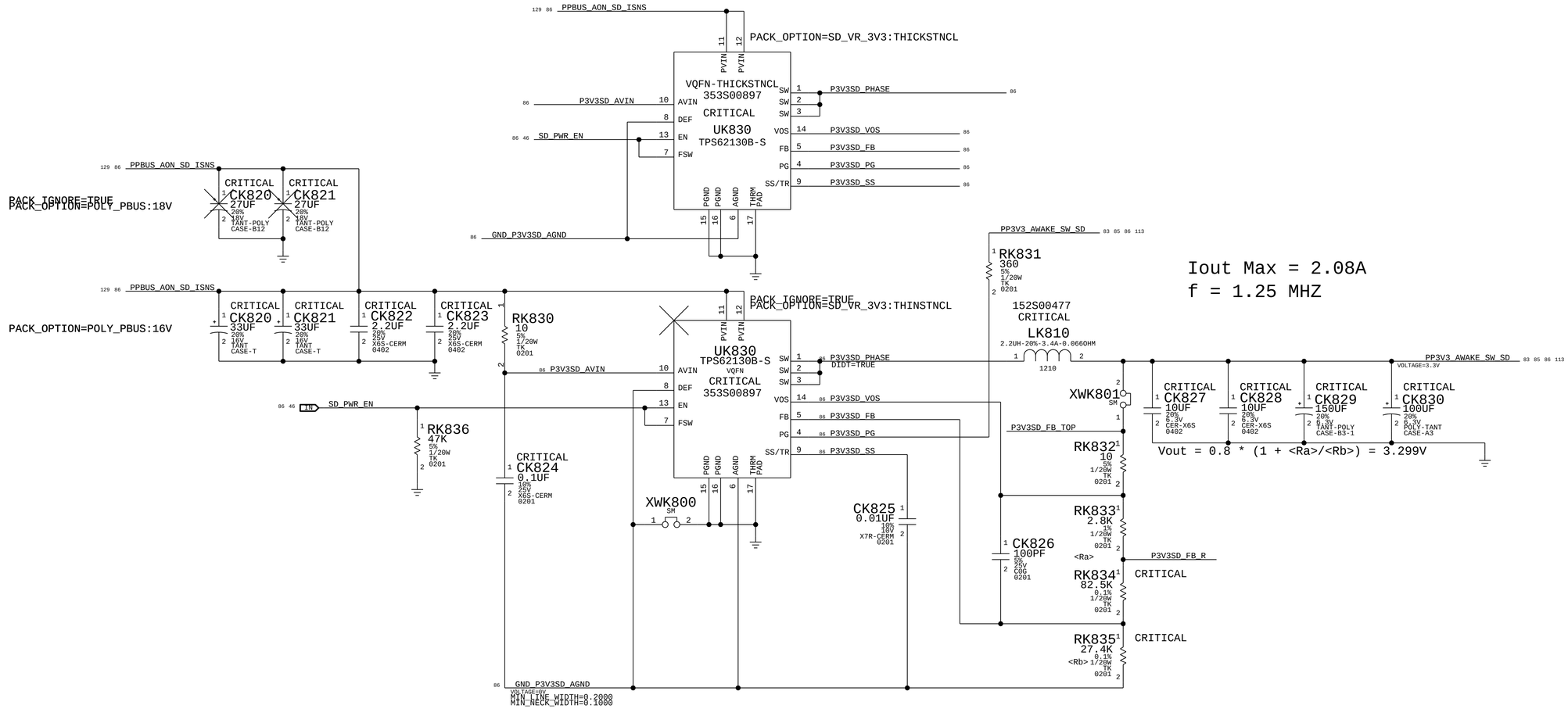

PAGE TITLE: SDCARD POWER SUPPORT

Apple Inc.

DRAWING NUMBER: 051-07754 | SIZE: D

REVISION: 6.0.0

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*** OK2INTEGRATE ***

FOR SYSTEM INTEGRATION INFORMATION OF WILLAMETTE REFER TO
RDAR://PROBLEM/72432057

WILLAMETTE WIFI/BT MODULE

PLACE_NEAR=UL000.48:4MM
PLACE_NEAR=UL000.48:3MM
PLACE_NEAR=UL000.48:3MM
PP3V8_AON_WLBT_ISNS 123 129
CL005 10UF 20% 10V X5R-CERM 0402-8
CL030 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL020 12PF 5% 25V NP0-C0G 0201
VBAT

PLACE_NEAR=UL000.37:4MM
PLACE_NEAR=UL000.37:3MM
PLACE_NEAR=UL000.37:3MM
PP3V8_AON_WLBT_ISNS 123 129
CL006 10UF 20% 10V X5R-CERM 0402-8
CL031 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL021 12PF 5% 25V NP0-C0G 0201
2GFEM_C0

PLACE_NEAR=UL000.79:4MM
PLACE_NEAR=UL000.79:3MM
PLACE_NEAR=UL000.79:3MM
PP3V8_AON_WLBT_ISNS 123 129
CL007 10UF 20% 10V X5R-CERM 0402-8
CL032 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL022 12PF 5% 25V NP0-C0G 0201
2GFEM_C1

PLACE_NEAR=UL000.12:4MM
PLACE_NEAR=UL000.12:3MM
PLACE_NEAR=UL000.12:3MM
PP3V8_AON_WLBT_ISNS 123 129
CL008 10UF 20% 10V X5R-CERM 0402-8
CL033 3PF +/-0.1PF 25V C0G 0201
CRITICAL
CL023 12PF 5% 25V NP0-C0G 0201
5GFEM

PLACE_NEAR=UL000.31:5MM
PLACE_NEAR=UL000.31:5MM
PP1V8_S2_WLBT_ISNS 123 129
CL010 0.1UF 10% 6.3V CERM-X5R 0201
CRITICAL
CL024 12PF 5% 25V NP0-C0G 0201
2GFEM_C0

PLACE_NEAR=UL000.86:5MM
PLACE_NEAR=UL000.86:5MM
PP1V8_S2_WLBT_ISNS 123 129
CL011 10UF 20% 10V X5R-CERM 0402-8
CRITICAL
CL025 12PF 5% 25V NP0-C0G 0201
2GFEM_C1

PLACE_NEAR=UL000.22:3MM
PLACE_NEAR=UL000.22:4MM
PP1V8_S2_WLBT_ISNS 123 129
CL012 0.1UF 10% 6.3V CERM-X5R 0201
CL034 3PF +/-0.1PF 25V C0G 0201
5GFEM_C0

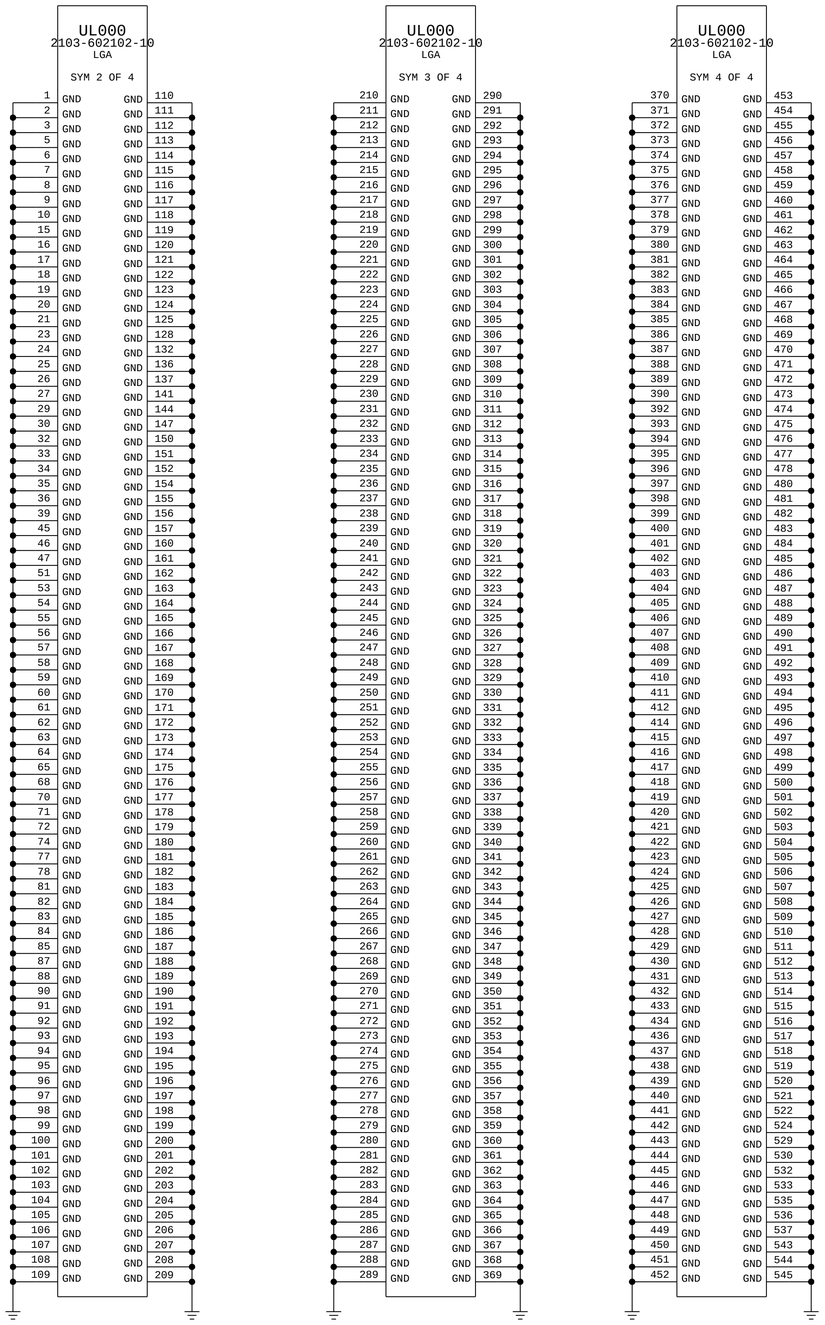
PLACE_NEAR=UL000.4:4MM
PLACE_NEAR=UL000.4:3MM
PP1V8_S2_WLBT_ISNS 123 129
CL013 0.1UF 10% 6.3V CERM-X5R 0201
CL035 3PF +/-0.1PF 25V C0G 0201
5GFEM_C1

PP1V8_S2_WLBT_ISNS 129 123 87
PP3V8_AON_WLBT_ISNS 129 123 87
PP1V25_S2 107
PLACE_NEAR=UL000.51:4MM
CL014 0.1UF 10% 6.3V CERM-X5R 0201

| | | |

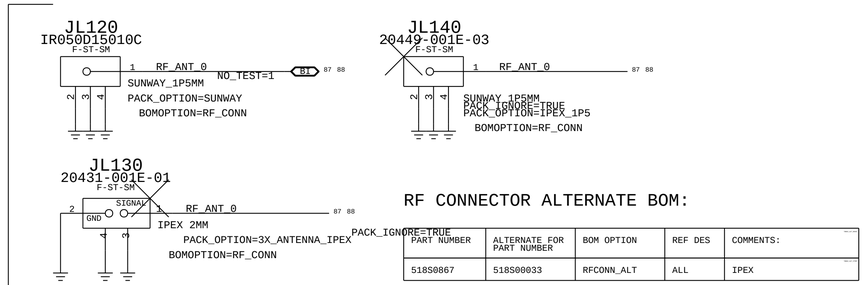
*** OK2INTEGRATE ***

WILLAMETTE WIFI/BT MODULE GND



ANTENNA CONNECTORS

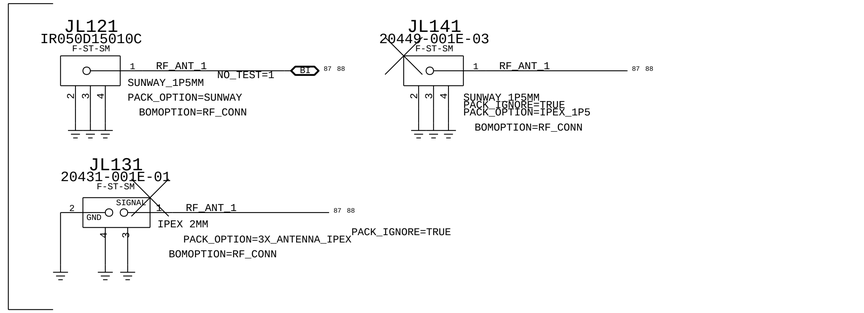
2G_C0
5G_C0
BT_C0



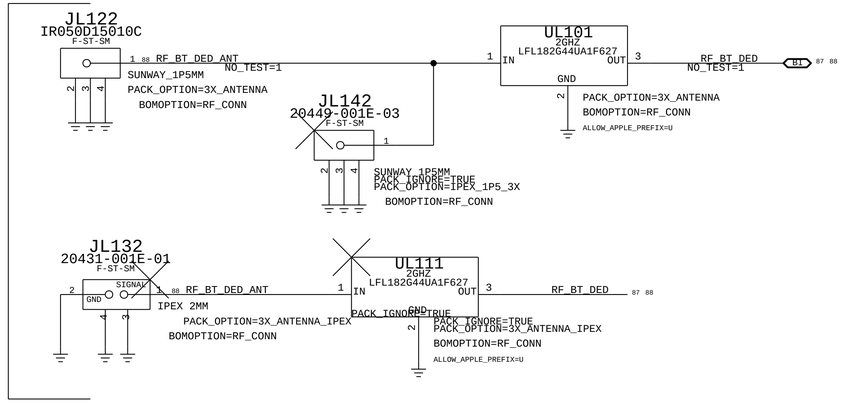
RF CONNECTOR ALTERNATE BOM:

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
518S0867	518S00033	RFCONN_ALT	ALL	IPEX

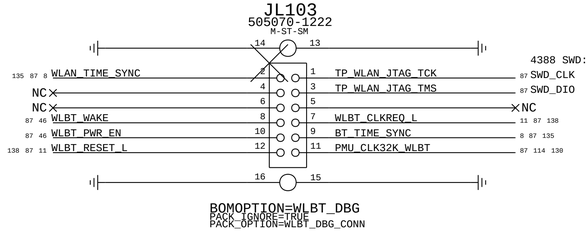
2G_C1
5G_C1
BT_C1



BT_C1_DED



WLBT DEBUG CONNECTOR



BOM_COST_GROUP=WIRELESS

PAGE TITLE
WIFI/BT: ANTENNA and GND

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DRAWING NUMBER 051-07754 | SIZE D
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A NAND0 S5E0 Control

UN000
MK2-H1.3MM
BGA
SYM 2 OF 4
OMIT_TABLE
998-24627

91 IN NAND0_CLK24M_0 → N11 CLK_IN
130 IN NAND0_RESET0_L → J6 RESET*
91 90 89 IN NAND0_JTAG_TRST_L → F7 TRST* (INT PD)

138 91 11 IN PCIE_CLK100M_NAND0_0_P → T6 PCIE_REFCLK_P
138 91 11 IN PCIE_CLK100M_NAND0_0_N → U6 PCIE_REFCLK_N
91 OUT NAND0_CLKREQ0_R_L → P6 PCIE_CLKREQ*

PCIE AC caps - place as close as possible to NAND

138 11 IN PCIE_NAND0_R2D_C_P<0> → CN003 0.22UF → PCIE_NAND0_R2D_P<0> → U8 PCIE_RX0_P
138 11 IN PCIE_NAND0_R2D_C_N<0> → CN004 0.22UF → PCIE_NAND0_R2D_N<0> → T8 PCIE_RX0_N
138 11 OUT PCIE_NAND0_D2R_P<0> ← CN001 0.22UF ← PCIE_NAND0_D2R_C_P<0> ← U10 PCIE_TX0_P
138 11 OUT PCIE_NAND0_D2R_N<0> ← CN002 0.22UF ← PCIE_NAND0_D2R_C_N<0> ← T10 PCIE_TX0_N

GND_VOID=TRUE
10% 6.3V X5R-CERM 0201

91 90 11 138 IN NAND0_PCIE_RESET_L → F10 EXT_NCE/PERST*

91 NAND0_S5E0_PCIE_RESREF → N10 PCIE_RESREF

CN085 10PF 5% 25V C0G 0201
RN004 200 0.1% 1/20W TK 0201-2
PLACE_NEAR=UN000.K5:15MM
RN005 300 1% 1/20W TK 0201
PLACE_NEAR=UN000.M11:15MM
RN006 300 1% 1/20W TK 0201

91 NAND0_S5E0_ZQ_1 → K5 ZQ_1
91 NAND0_S5E0_ZQ_0 → M11 ZQ_0

(INT PU) EXT_D0/BOOT0 G8 NAND0_LPB_L → IN 46 90 91
(INT PD) EXT_D1/BOOT1 H9 NAND_BFH → IN 7 90 91 134
EXT_D2/BOOT2/SPINAND_SCLK F8 NAND0_BOOT2 → 89 90 91
EXT_D3/SPINAND_MISO/SWD_UID0 E8 NAND0_S5E0_SWD_UID0 → 89 91
EXT_D4/SPI_CS G9
EXT_D5/SPINAND_MOSI/SWD_UID1 E9 NAND0_S5E0_SWD_UID1 → 89 91
EXT_D6/BOOT3 F9
EXT_D7/SPF* G10 NAND0_PFN_L → IN 90 91
(INT PU) EXT_DQS/BCM* E10 NAND0_BCM_L → IN 89 90

(INT PU) EXT_NRE/JTAG_TMS E6 SWD_NAND0_S5E0_SWDIO → IN 15 91
(INT PU) EXT_NWE/JTAG_TCK F6 SWD_NAND0_S5E0_SWCLK → IN 15 91
EXT_RNB/JTAG_TDO G6 NAND0_S5E0_JTAG_TDO → OUT 90 91
(INT PU) EXT_CLE/JTAG_TDI G7 TP_NAND0_S5E0_JTAG_TDI → IN 91
(INT PD) EXT_ALE/JTAG_SEL E7 NAND0_JTAG_SEL → IN 89 90 91
DROOP* N4 TP_NAND0_S5E0_DROOP_L → 133
WP* E5 NAND0_WP_L → IN 89 90 91

ANI0_VREF K11 TP_NAND0_S5E0_ANI0_VREF 91
ANI1_VREF M5 TP_NAND0_S5E0_ANI1_VREF 91

B NAND0 S5E0 Bulk Capacitance

PP2V58_AWAKE_NAND_VCC
CN020 20UF 20% 4V CERM 0402
CN022 2.2UF 20% 10V X5R 0201
CN023 2.2UF 20% 10V X5R 0201
CN024 2.2UF 20% 10V X5R 0201
CN025 2.2UF 20% 10V X5R 0201

PP1V25_AWAKE_NAND_VCCQ
CN030 4.3UF 20% 4V CERM 0402-THICKSTNCL
CN034 2.2UF 20% 10V X5R 0201
CN035 2.2UF 20% 10V X5R 0201
CN036 2.2UF 20% 10V X5R 0201
CN037 2.2UF 20% 10V X5R 0201
CN038 2.2UF 20% 10V X5R 0201
CN039 2.2UF 20% 10V X5R 0201
CN03A 2.2UF 20% 10V X5R 0201
CN032 20UF 20% 10V X5R 0402

FLN000 10OHM-50%-1A-0.05OHM 0201
PP1V25_AWAKE_NAND_VCCQ → PP1V2_NAND0_S5E0_PCI_AVDD_H 89 VOLTAGE=1.2V
PLACE_NEAR=UN000.P9:11.5MM
CN045 4.7UF 20% 4V CER-X5R 0201
CN044 0.1UF 10% 6.3V CERM-X5R 0201

RN010 2 1/20W 1% TK 0201
PP1V25_AWAKE_NAND_VCCQ → PP1V2_NAND0_S5E0_AVDD1X_PLL 89 VOLTAGE=1.2V
PLACE_NEAR=UN000.N6:11.5MM
CN047 2.2UF 20% 10V X5R 0201
CN046 0.1UF 10% 6.3V CERM-X5R 0201

PP0V88_AWAKE_NAND_VDD
CN010 20UF 20% 10V X5R 0402
CN011 20UF 20% 10V X5R 0402
CN012 2.2UF 20% 10V X5R 0201
CN013 2.2UF 20% 10V X5R 0201
CN014 2.2UF 20% 10V X5R 0201
CN015 0.1UF 10% 6.3V CERM-X5R 0201
CN016 0.1UF 10% 6.3V CERM-X5R 0201
CN017 0.1UF 10% 6.3V CERM-X5R 0201

FLN001 10OHM-50%-1A-0.05OHM 0201
PP0V88_AWAKE_NAND_VDD → PP0V9_NAND0_S5E0_VDD_PLL 89 91
PLACE_NEAR=FLN001.2:5MM
PLACE_NEAR=UN000.M6:11.5MM
VOLTAGE=0.9V
CN083 4.7UF 20% 2V CER-X5R 0201

The inductance from CN047, CN046, CN045, CN044 to their S5E pins shall be less than 1100pH

C NAND0 S5E0 Bulk Miscellaneous

Spec recommends to tie BCM, WP directly to 1.2V rail

PP1V25_AWAKE_NAND_VCCQ
RN001 0 1/20W 0% TK 0201 NAND0_BCM_L 89 90
RN007 0 1/20W 0% TK 0201 NAND0_WP_L 89 90 91

Spec recommends to tie Boot2 directly to Gnd

91 90 89 NAND0_BOOT2 — RN021 0 1/20W 0% TK 0201
91 90 89 NAND0_JTAG_SEL — RN002 47K 1/20W 1% TK 0201
91 90 89 NAND0_JTAG_TRST_L — RN000 47K 1/20W 1% TK 0201
91 89 NAND0_S5E0_SWD_UID0 — RN008 47K 1/20W 1% TK 0201
91 89 NAND0_S5E0_SWD_UID1 — RN009 47K 1/20W 1% TK 0201

PCB designers should add stiching vias for RFU/RFU_2 NC pins

UN000
MK2-H1.3MM
BGA
SYM 3 OF 4
OMIT_TABLE
998-24627

NC_UN000_C5 C5 RFU_2
NC_UN000_C6 C6 RFU_2
NC_UN000_C7 C7 RFU_2
NC_UN000_C8 C8 RFU_2
NC_UN000_C9 C9 RFU_2
NC_UN000_D4 D4 RFU_2
NC_UN000_D5 D5 RFU_2
NC_UN000_D6 D6 RFU_2
NC_UN000_D7 D7 RFU_2
NC_UN000_D8 D8 RFU_2
NC_UN000_D9 D9 RFU_2
NC_UN000_D10 D10 RFU_2
NC_UN000_D11 D11 RFU_2
NC_UN000_D12 D12 RFU_2

NC Y11
RFU_2 C10 NC_UN000_C10
RFU_2 C11 NC_UN000_C11
RFU H10 NC_UN000_H10
RFU J10 NC_UN000_J10
RFU K6 NC_UN000_K6
RFU K10 NC_UN000_K10
RFU L5 NC_UN000_L5
RFU L6 NC_UN000_L6
RFU L10 NC_UN000_L10
RFU L11 NC_UN000_L11
RFU M10 NC_UN000_M10

D NAND0 S5E0 Power/Gnd

UN000
MK2-H1.3MM
BGA
SYM 1 OF 4
OMIT_TABLE
998-24627

PP2V58_AWAKE_NAND_VCC → E4 E12 F4 F12 T4 T12 U4 U12 VCC (VCC)

PP1V25_AWAKE_NAND_VCCQ → G5 G11 H5 H11 P5 P11 R5 R11 VDDIO_1 (VCCQ_IO)

89 PP1V2_NAND0_S5E0_PCI_AVDD_H → P9 P10 PCIE_AVDD_H
89 PP1V2_NAND0_S5E0_AVDD1X_PLL → N6 AVDD1X_PLL

PP1V25_AWAKE_NAND_VCCQ → G12 G4 H4 H12 K4 M12 P4 P12 R4 R12 VDDIO_2_L_ANI (VCCQ_ANI)
K12 L4 L12 M4 VDDIO_2_DP

126 89 PP0V88_AWAKE_NAND_VDD → J7 J9 K7 K9 M7 M9 N7 N9 VDD (VDD)
P7 R7 R9 PCIE_VDD

91 89 PP0V9_NAND0_S5E0_VDD_PLL → M6 VDD_PLL

91 TP_NAND0_S5E0_VPP → E11 VPP
H6 VQPS

UN000
MK2-H1.3MM
BGA
SYM 4 OF 4
OMIT_TABLE
998-24627

A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 B1 B2 B3 B4 B12 B13 B14 B15 C1 C2 C3 C13 C14 C15 D1 D2 D14 D15 E1 E2 E14 E15 F1 F2 F14 F15 G1 G2 G14 G15 H1 H2 H14 H15 J1 J2 J14 J15 K1 K2 K14 K15 L1 L2 L14 L15 M1 M2 M14 M15 N1 N2 N14 VSS/DUMMY

VSS B5 B6 B7 B8 B9 B10 B11 C4 C12 D3 D13 E3 E13 F3 F5 F11 F13 G3 G13 H3 H7 H8 H13 J3 J4 J5 J8 J11 J12 J13 K3 K8 K13 L3 L7 L8 L9 L13 M3 M8 M13 N3 N5 N8 N12 N13 P3 P8 P13 R3 R6 R8 R10 R13 T3 T5 T7 T9 T11 T13 U3 U5 U7 U9 U11 U13 V4 V5 V6 V7 V8 V9 V10 V11 V12 (VSS)

BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD0 S5E MK2 <0>

Apple Inc.

DRAWING NUMBER 051-07754
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A NAND0 S5E1 Control

UN100
MK2-H1.3MM
BGA
SYM 2 OF 4
OMIT_TABLE
998-24627

NAND0_CLK24M_1 → CLK_IN (N11)
NAND0_RESET1_L → RESET* (J6)
NAND0_JTAG_TRST_L → TRST* (INT PD) (F7)
PCIE_CLK100M_NAND0_1_P → PCIE_REFCLK_P (T6)
PCIE_CLK100M_NAND0_1_N → PCIE_REFCLK_N (U6)
NAND0_CLKREQ1_R_L → PCIE_CLKREQ* (P6)

PCIE AC caps - place as close as possible to NAND

SSD_2L CN103 0.22UF GND_VOID=TRUE
PCIE_NAND0_R2D_C_P<1> → PCIE_NAND0_R2D_P<1> → PCIE_RX0_P (U8)
SSD_2L CN104 0.22UF GND_VOID=TRUE
PCIE_NAND0_R2D_C_N<1> → PCIE_NAND0_R2D_N<1> → PCIE_RX0_N (T8)
SSD_2L CN101 0.22UF GND_VOID=TRUE
PCIE_NAND0_D2R_P<1> → PCIE_NAND0_D2R_C_P<1> → PCIE_TX0_P (U10)
SSD_2L CN102 0.22UF GND_VOID=TRUE
PCIE_NAND0_D2R_N<1> → PCIE_NAND0_D2R_C_N<1> → PCIE_TX0_N (T10)
NAND0_PCIE_RESET_L → EXT_NCE/PERST* (F10)

NAND0_S5E1_PCIE_RESREF → PCIE_RESREF (N10)

SSD_2L CN185 10PF 5% 25V C0G 0201
SSD_2L RN104 200 0.1% 1/20W TK 0201-2
PLACE_NEAR=UN100.K5:15MM
SSD_2L RN105 300 1% 1/20W TK 0201
NAND0_S5E1_ZQ_1 → ZQ_1 (K5)
NAND0_S5E1_ZQ_0 → ZQ_0 (M11)
PLACE_NEAR=UN100.M11:15MM
SSD_2L RN106 300 1% 1/20W TK 0201
SSD_2L

(INT PU) EXT_D0/BOOT0 G8 NAND0_LPB_L
(INT PD) EXT_D1/BOOT1 H9 NAND_BFH
EXT_D2/BOOT2/SPINAND_SCLK F8 NAND0_BOOT2
EXT_D3/SPINAND_MISO/SWD_UID0 E8 NAND0_S5E1_SWD_UID0
EXT_D4/SPI_CS G9
EXT_D5/SPINAND_MOSI/SWD_UID1 E9 NAND0_S5E1_SWD_UID1
EXT_D6/BOOT3 F9
EXT_D7/SPF* G10 NAND0_PFN_L
(INT PU) EXT_DQS/BCM* E10 NAND0_BCM_L
(INT PU) EXT_NRE/JTAG_TMS E6 SWD_NAND0_S5E1_SWDIO
(INT PU) EXT_NWE/JTAG_TCK F6 SWD_NAND0_S5E1_SWCLK
EXT_RNB/JTAG_TDO G6 TP_NAND0_S5E1_JTAG_TDO
(INT PU) EXT_CLE/JTAG_TDI G7 NAND0_S5E0_JTAG_TDO
(INT PD) EXT_ALE/JTAG_SEL E7 NAND0_JTAG_SEL
DROOP* N4 TP_NAND0_S5E1_DROOP_L
WP* E5 NAND0_WP_L
ANI0_VREF K11 TP_NAND0_S5E1_ANI0_VREF
ANI1_VREF M5 TP_NAND0_S5E1_ANI1_VREF

B NAND0 S5E1 Bulk Capacitance

PP2V58_AWAKE_NAND_VCC
SSD_2L CN120 20UF 20% 10V X5R 0402
SSD_2L CN122 2.2UF 20% 10V X5R 0201
SSD_2L CN123 2.2UF 20% 10V X5R 0201
SSD_2L CN124 2.2UF 20% 10V X5R 0201
SSD_2L CN125 2.2UF 20% 10V X5R 0201
SSD_2L FLN100 10OHM-50%-1A-0.05OHM 0201
PP1V25_AWAKE_NAND_VCCQ
PLACE_NEAR=UN100.P9:11.5MM
PP1V2_NAND0_S5E1_PCI_AVDD_H VOLTAGE=1.2V
SSD_2L CN145 4.7UF 20% 10V CER-X5R 0201
SSD_2L CN144 0.1UF 10% 6.3V CERM-X5R 0201
SSD_2L RN110 2 1/20W 1% TK 0201
PP1V25_AWAKE_NAND_VCCQ
PLACE_NEAR=UN100.N6:11.5MM
PP1V2_NAND0_S5E1_AVDD1X_PLL VOLTAGE=1.2V
SSD_2L CN147 2.2UF 20% 10V X5R 0201
SSD_2L CN146 0.1UF 10% 6.3V CERM-X5R 0201

PP1V25_AWAKE_NAND_VCCQ
SSD_2L CN130 4.3UF 20% 4V CERM 0402-THICKSTNCL
SSD_2L CN134 2.2UF 20% 10V X5R 0201
SSD_2L CN135 2.2UF 20% 10V X5R 0201
SSD_2L CN136 2.2UF 20% 10V X5R 0201
SSD_2L CN137 2.2UF 20% 10V X5R 0201
SSD_2L CN138 2.2UF 20% 10V X5R 0201
SSD_2L CN139 2.2UF 20% 10V X5R 0201
SSD_2L CN13A 2.2UF 20% 10V X5R 0201
SSD_2L CN132 20UF 20% 10V X5R 0402

PP0V88_AWAKE_NAND_VDD
SSD_2L CN110 20UF 20% 10V X5R 0402
SSD_2L CN111 20UF 20% 10V X5R 0402
SSD_2L CN112 2.2UF 20% 10V X5R 0201
SSD_2L CN113 2.2UF 20% 10V X5R 0201
SSD_2L CN114 2.2UF 20% 10V X5R 0201
SSD_2L CN115 0.1UF 10% 6.3V CERM-X5R 0201
SSD_2L CN116 0.1UF 10% 6.3V CERM-X5R 0201
SSD_2L CN117 0.1UF 10% 6.3V CERM-X5R 0201
SSD_2L FLN101 10OHM-50%-1A-0.05OHM 0201
PP0V88_AWAKE_NAND_VDD
PLACE_NEAR=FLN101.2:5MM
PP0V9_NAND0_S5E1_VDD_PLL VOLTAGE=0.9V
PLACE_NEAR=UN100.M6:11.5MM
SSD_2L CN183 4.7UF 20% 6.3V CER-X5R 0201

The inductance from CN147, CN146, CN145, CN144 to their S5E pins shall be less than 1100pH

C NAND0 S5E1 Bulk Miscellaneous

PP1V25_AWAKE_NAND_VCCQ
SSD_2L RN108 47K 1/20W 1% TK 0201
NAND0_S5E1_SWD_UID0
SSD_2L RN109 47K 1/20W 1% TK 0201
NAND0_S5E1_SWD_UID1
SSD_2L

PCB designers should add stiching vias for RFU/RFU_2 NC pins

UN100
MK2-H1.3MM
BGA
SYM 3 OF 4
OMIT_TABLE
998-24627

NC_UN100_C5 C5 RFU_2
NC_UN100_C6 C6 RFU_2
NC_UN100_C7 C7 RFU_2
NC_UN100_C8 C8 RFU_2
NC_UN100_C9 C9 RFU_2
NC_UN100_D4 D4 RFU_2
NC_UN100_D5 D5 RFU_2
NC_UN100_D6 D6 RFU_2
NC_UN100_D7 D7 RFU_2
NC_UN100_D8 D8 RFU_2
NC_UN100_D9 D9 RFU_2
NC_UN100_D10 D10 RFU_2
NC_UN100_D11 D11 RFU_2
NC_UN100_D12 D12 RFU_2

NC Y11
RFU_2 C10 NC_UN100_C10
RFU_2 C11 NC_UN100_C11
RFU H10 NC_UN100_H10
RFU J10 NC_UN100_J10
RFU K6 NC_UN100_K6
RFU K10 NC_UN100_K10
RFU L5 NC_UN100_L5
RFU L6 NC_UN100_L6
RFU L10 NC_UN100_L10
RFU L11 NC_UN100_L11
RFU M10 NC_UN100_M10

D NAND0 S5E1 Power/Gnd

UN100
MK2-H1.3MM
BGA
SYM 1 OF 4
OMIT_TABLE
998-24627

PP2V58_AWAKE_NAND_VCC → VCC (VCC): E4, E12, F4, F12, T4, T12, U4, U12
PP1V25_AWAKE_NAND_VCCQ → VDDIO_1 (VCCQ_IO): G5, G11, H5, H11, P5, P11, R5, R11
PP1V2_NAND0_S5E1_PCI_AVDD_H → PCIE_AVDD_H: P9, P10
PP1V2_NAND0_S5E1_AVDD1X_PLL → AVDD1X_PLL: N6
PP1V25_AWAKE_NAND_VCCQ → VDDIO_2_L_ANI (VCCQ_ANI): G12, G4, H4, H12, K4, M12, P4, P12, R4, R12
VDDIO_2_DP: K12, L4, L12, M4
PP0V88_AWAKE_NAND_VDD → VDD (VDD): J7, J9, K7, K9, M7, M9, N7, N9
PCIE_VDD: P7, R7, R9
PP0V9_NAND0_S5E1_VDD_PLL → VDD_PLL: M6
TP_NAND0_S5E1_VPP → VPP: E11
VQPS: H6

VSS: B5, B6, B7, B8, B9, B10, B11, C4, C12, D3, D13, E3, E13, F3, F5, F11, F13, G3, G13, H3, H7, H8, H13, J3, J4, J5, J8, J11, J12, J13, K3, K8, K13, L3, L7, L8, L9, L13, M3, M8, M13, N3, N5, N8, N12, N13, P3, P8, P13, R3, R6, R8, R10, R13, T3, T5, T7, T9, T11, T13, U3, U5, U7, U9, U11, U13, V4, V5, V6, V7, V8, V9, V10, V11, V12

UN100
MK2-H1.3MM
BGA
SYM 4 OF 4
OMIT_TABLE
998-24627

A1 VSS/DUMMY VSS/DUMMY N15
A2 VSS/DUMMY VSS/DUMMY P1
A3 VSS/DUMMY VSS/DUMMY P2
A4 VSS/DUMMY VSS/DUMMY P14
A5 VSS/DUMMY VSS/DUMMY P15
A6 VSS/DUMMY VSS/DUMMY R1
A7 VSS/DUMMY VSS/DUMMY R2
A8 VSS/DUMMY VSS/DUMMY R14
A9 VSS/DUMMY VSS/DUMMY R15
A10 VSS/DUMMY VSS/DUMMY T1
A11 VSS/DUMMY VSS/DUMMY T2
A12 VSS/DUMMY VSS/DUMMY T14
A13 VSS/DUMMY VSS/DUMMY T15
A14 VSS/DUMMY VSS/DUMMY U1
A15 VSS/DUMMY VSS/DUMMY U2
B1 VSS/DUMMY VSS/DUMMY U14
B2 VSS/DUMMY VSS/DUMMY U15
B3 VSS/DUMMY VSS/DUMMY V1
B4 VSS/DUMMY VSS/DUMMY V2
B12 VSS/DUMMY VSS/DUMMY V3
B13 VSS/DUMMY VSS/DUMMY V13
B14 VSS/DUMMY VSS/DUMMY V14
B15 VSS/DUMMY VSS/DUMMY V15
C1 VSS/DUMMY VSS/DUMMY W1
C2 VSS/DUMMY VSS/DUMMY W2
C3 VSS/DUMMY VSS/DUMMY W3
C13 VSS/DUMMY VSS/DUMMY W4
C14 VSS/DUMMY VSS/DUMMY W5
C15 VSS/DUMMY VSS/DUMMY W6
D1 VSS/DUMMY VSS/DUMMY W7
D2 VSS/DUMMY VSS/DUMMY W8
D14 VSS/DUMMY VSS/DUMMY W9
D15 VSS/DUMMY VSS/DUMMY W10
E1 VSS/DUMMY VSS/DUMMY W11
E2 VSS/DUMMY VSS/DUMMY W12
E14 VSS/DUMMY VSS/DUMMY W13
E15 VSS/DUMMY VSS/DUMMY W14
F1 VSS/DUMMY VSS/DUMMY W15
F2 VSS/DUMMY VSS/DUMMY Y1
F14 VSS/DUMMY VSS/DUMMY Y2
F15 VSS/DUMMY VSS/DUMMY Y3
G1 VSS/DUMMY VSS/DUMMY Y4
G2 VSS/DUMMY VSS/DUMMY Y5
G14 VSS/DUMMY VSS/DUMMY Y6
G15 VSS/DUMMY VSS/DUMMY Y7
H1 VSS/DUMMY VSS/DUMMY Y8
H2 VSS/DUMMY VSS/DUMMY Y9
H14 VSS/DUMMY VSS/DUMMY Y10
H15 VSS/DUMMY VSS/DUMMY Y12
J1 VSS/DUMMY VSS/DUMMY Y13
J2 VSS/DUMMY VSS/DUMMY Y14
J14 VSS/DUMMY VSS/DUMMY Y15
J15 VSS/DUMMY VSS/DUMMY AA1
K1 VSS/DUMMY VSS/DUMMY AA2
K2 VSS/DUMMY VSS/DUMMY AA3
K14 VSS/DUMMY VSS/DUMMY AA4
K15 VSS/DUMMY VSS/DUMMY AA5
L1 VSS/DUMMY VSS/DUMMY AA6
L2 VSS/DUMMY VSS/DUMMY AA7
L14 VSS/DUMMY VSS/DUMMY AA8
L15 VSS/DUMMY VSS/DUMMY AA9
M1 VSS/DUMMY VSS/DUMMY AA10
M2 VSS/DUMMY VSS/DUMMY AA11
M14 VSS/DUMMY VSS/DUMMY AA12
M15 VSS/DUMMY VSS/DUMMY AA13
N1 VSS/DUMMY VSS/DUMMY AA14
N2 VSS/DUMMY VSS/DUMMY AA15
N14 VSS/DUMMY

BOM_COST_GROUP=SSD

PAGE TITLE: STORAGE: SSD0 S5E MK2 <1>

Apple Inc.

DRAWING NUMBER: 051-07754
SIZE: D
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8	7	6	5	4	3	2	1

89	IN	PP0V9_NAND0_S5E0_VDD_PLL	TOP 1	TP	TPP001	TP-P4	
90	IN	PP0V9_NAND0_S5E1_VDD_PLL	TOP 1	TP	TPP002	TP-P4	
90 89 46	IN	NAND0_LPB_L	TOP 1	TP	TPP003	TP-P4	
134 90 89 7	IN	NAND_BFH	TOP 1	TP	TPP004	TP-P4	
90 89	IN	NAND0_BOOT2	TOP 1	TP	TPP005	TP-P4	
89	IN	NAND0_S5E0_SWD_UID0	TOP 1	TP	TPP006	TP-P4	
90	IN	NAND0_S5E1_SWD_UID0	TOP 1	TP	TPP007	TP-P4	
89	IN	NAND0_S5E0_SWD_UID1	TOP 1	TP	TPP008	TP-P4	
90	IN	NAND0_S5E1_SWD_UID1	TOP 1	TP	TPP009	TP-P4	
91 90 89	IN	NAND0_PFN_L	TOP 1	TP	TPP010	TP-P4	
138 90 89 11	IN	NAND0_PCIE_RESET_L	TOP 1	TP	TPP011	TP-P4	
90 89	IN	NAND0_S5E0_JTAG_TDO	TOP 1	TP	TPP014	TP-P4	
89	IN	TP_NAND0_S5E0_JTAG_TDI	TOP 1	TP	TPP015	TP-P4	
130	IN	TP_NAND0_S5E1_JTAG_TDO	TOP 1	TP	TPP016	TP-P4	
90 89	IN	NAND0_JTAG_SEL	TOP 1	TP	TPP017	TP-P4	
90 89	IN	NAND0_WP_L	TOP 1	TP	TPP018	TP-P4	
138 91 11	IN	NAND0_CLKREQ0_L	TOP 1	TP	TPP019	TP-P4	
138 91 11	IN	NAND0_CLKREQ1_L	TOP 1	TP	TPP020	TP-P4	
89	IN	NAND0_S5E0_PCIE_RESREF	TOP 1	TP	TPP021	TP-P4	
90	IN	NAND0_S5E1_PCIE_RESREF	TOP 1	TP	TPP022	TP-P4	
134 130	IN	NAND0_RESET0_L	TOP 1	TP	TPP023	TP-P4	
134 130	IN	NAND0_RESET1_L	TOP 1	TP	TPP037	TP-P4	
90	IN	NAND0_S5E1_ZQ_0	TOP 1	TP	TPP024	TP-P4	
89	IN	NAND0_S5E0_ZQ_0	TOP 1	TP	TPP025	TP-P4	
89	IN	NAND0_S5E0_ZQ_1	TOP 1	TP	TPP026	TP-P4	
90	IN	NAND0_S5E1_ZQ_1	TOP 1	TP	TPP027	TP-P4	
90 89	IN	NAND0_JTAG_TRST_L	TOP 1	TP	TPP028	TP-P4	
89	IN	TP_NAND0_S5E0_ANI1_VREF	TOP 1	TP	TPP029	TP-P4	
89	IN	TP_NAND0_S5E0_ANI0_VREF	TOP 1	TP	TPP030	TP-P4	
90	IN	TP_NAND0_S5E1_ANI1_VREF	TOP 1	TP	TPP031	TP-P4	
90	IN	TP_NAND0_S5E1_ANI0_VREF	TOP 1	TP	TPP032	TP-P4	
89 15	IN	SWD_NAND0_S5E0_SWDIO	TOP 1	TP	TPP033	TP-P4	
89 15	IN	SWD_NAND0_S5E0_SWCLK	TOP 1	TP	TPP034	TP-P4	
90 15	IN	SWD_NAND0_S5E1_SWDIO	TOP 1	TP	TPP035	TP-P4	
90 15	IN	SWD_NAND0_S5E1_SWCLK	TOP 1	TP	TPP036	TP-P4	
89	IN	TP_NAND0_S5E0_VPP	1	TP	TPP038	TP-P4	
90	IN	TP_NAND0_S5E1_VPP	1	TP	TPP039	TP-P4	
91 89	IN	NAND0_CLK24M_0	1	TP	TPP040	TP-P4	
91 90	IN	NAND0_CLK24M_1	1	TP	TPP041	TP-P4	

RP000
33
5%
1/20W
TK
0201
PLACE_NEAR=U0600.AH51:25MM

134 7 IN NAND0_CLK24M0_R — 1 — 2 — NAND0_CLK24M_0 OUT 89 91

NOSTUFF
RP005
47K
1%
1/20W
TK
0201

RP001
33
5%
1/20W
TK
0201
PLACE_NEAR=U0600.AG51:25MM

134 7 IN NAND0_CLK24M1_R — 1 — 2 — NAND0_CLK24M_1 OUT 90 91

NOSTUFF
RP006
47K
1%
1/20W
TK
0201

138 89 11		PCIE_CLK100M_NAND0_0_N	1	A	TPP090	TP-P4	998-4704
138 89 11		PCIE_CLK100M_NAND0_0_P	1	A	TPP091	TP-P4	998-4704
138 90 11		PCIE_CLK100M_NAND0_1_N	1	A	TPP092	TP-P4	998-4704
138 90 11		PCIE_CLK100M_NAND0_1_P	1	A	TPP093	TP-P4	998-4704

RP003
0
0%
1/20W
TK
0201

138 91 11 IN NAND0_CLKREQ0_L — 1 — 2 — NAND0_CLKREQ0_R_L OUT 89

SSD_2L
RP004
0
0%
1/20W
TK
0201

138 91 11 IN NAND0_CLKREQ1_L — 1 — 2 — NAND0_CLKREQ1_R_L OUT 90

RP002
0
0%
1/20W
TK
0201

113 47 46 45 IN PMU_SYS_ALIVE — 1 — 2 — NAND0_PFN_L OUT 89 90 91

BOM_COST_GROUP=SSD

PAGE TITLE
STORAGE: SSD SUPPORT

Apple Inc.

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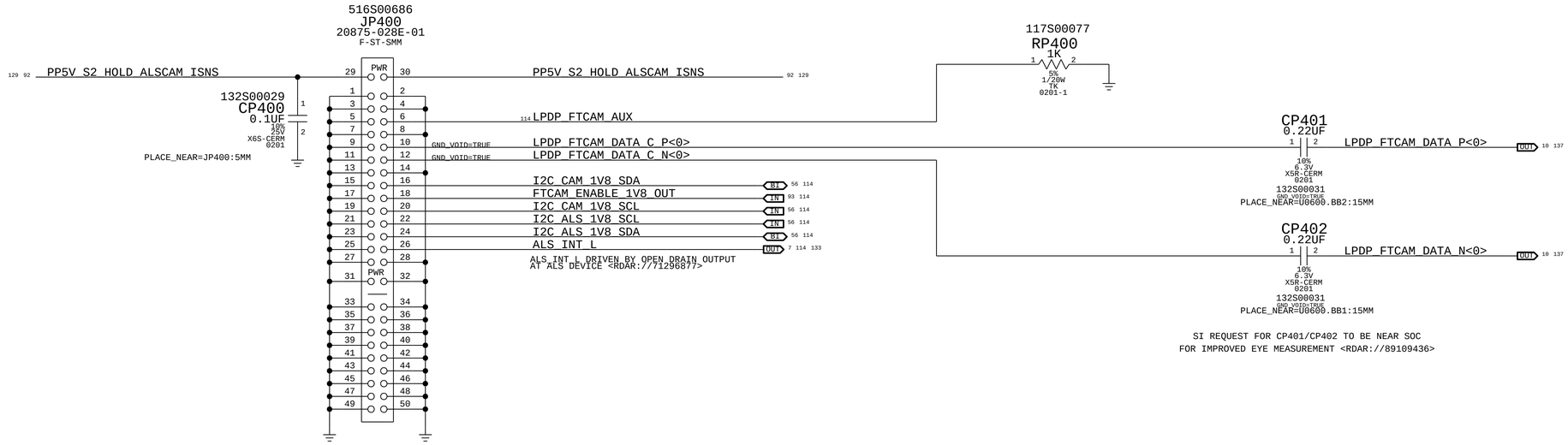
CAMERA FLEX CONNECTOR FROM X2724 MLB_S



BOM_COST_GROUP=CAMERA

PAGE TITLE
CAMERA: FLEX CONNECTOR

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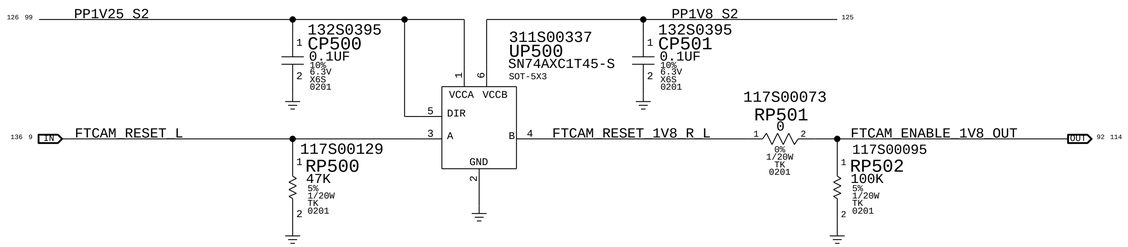

BOM_COST_GROUP=CAMERA

PAGE TITLE	CAMERA: SUPPORT
	Apple Inc.
DRAWING NUMBER	051-07754
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ZERO OHM USEAGE DEPENDENT ON <RDAR://71288682>

CP620 0.1UF	LPDP_INT_DATA_C_N<3>	IN	LPDP_INT_DATA_L_N<3>	RP620 0	LPDP_INT_DATA_N<3>	OUT
CP621 0.1UF	LPDP_INT_DATA_C_P<3>	IN	LPDP_INT_DATA_L_P<3>	RP621 0	LPDP_INT_DATA_P<3>	OUT
CP612 0.1UF	LPDP_INT_DATA_C_N<2>	IN	LPDP_INT_DATA_L_N<2>	RP612 0	LPDP_INT_DATA_N<2>	OUT
CP613 0.1UF	LPDP_INT_DATA_C_P<2>	IN	LPDP_INT_DATA_L_P<2>	RP613 0	LPDP_INT_DATA_P<2>	OUT
CP614 0.1UF	LPDP_INT_DATA_C_N<1>	IN	LPDP_INT_DATA_L_N<1>	RP614 0	LPDP_INT_DATA_N<1>	OUT
CP615 0.1UF	LPDP_INT_DATA_C_P<1>	IN	LPDP_INT_DATA_L_P<1>	RP615 0	LPDP_INT_DATA_P<1>	OUT
CP616 0.1UF	LPDP_INT_DATA_C_N<0>	IN	LPDP_INT_DATA_L_N<0>	RP616 0	LPDP_INT_DATA_N<0>	OUT
CP617 0.1UF	LPDP_INT_DATA_C_P<0>	IN	LPDP_INT_DATA_L_P<0>	RP617 0	LPDP_INT_DATA_P<0>	OUT
CP618 0.1UF	LPDP_INT_AUX_C_N	IN	LPDP_INT_AUX_L_N	RP618 0	LPDP_INT_AUX_N	OUT
CP619 0.1UF	LPDP_INT_AUX_C_P	IN	LPDP_INT_AUX_L_P	RP619 0	LPDP_INT_AUX_P	OUT

All 0.1UF: 10% 16V X5R-CERM 0201, GND_VOID=TRUE. All 0: 0% 1/20W TK 0201, GND_VOID=TRUE.

NOSTUFF RP601 1M 5% 1/20W TK 0201

NOSTUFF RP602 1M 5% 1/20W TK 0201

516S00682
JP600
20875-034E-01
F-ST-SMM

		35	PWR	36		
		1	SIGNAL	2		
LPDP_INT_DATA_N<3>	GND_VOID=TRUE	3		4	PP1V8_S2	125
LPDP_INT_DATA_P<3>	GND_VOID=TRUE	5		6	I2C_DISP_TEMP_1V8_SCL	IN 54 113
		7		8	I2C_DISP_TEMP_1V8_SDA	BI 54 113
LPDP_INT_DATA_N<2>	GND_VOID=TRUE	9		10		
LPDP_INT_DATA_P<2>	GND_VOID=TRUE	11		12		
		13		14	UART_TCON_D2R_1V8	94 113
LPDP_INT_DATA_N<1>	GND_VOID=TRUE	15		16		
LPDP_INT_DATA_P<1>	GND_VOID=TRUE	17		18	SWD NOT NEEDED ON MLB	
		19		20		
LPDP_INT_DATA_N<0>	GND_VOID=TRUE	21		22	SPI_TCON_CS_L	IN 8 113 135
LPDP_INT_DATA_P<0>	GND_VOID=TRUE	23		24	SPI_TCON_MOSI_CONN	94 113
		25		26	SPI_TCON_MISO_CONN	94 113
LPDP_INT_AUX_N	GND_VOID=TRUE	27		28	SPI_TCON_CLK_CONN	94 113
LPDP_INT_AUX_P	GND_VOID=TRUE	29		30		
		31		32	EDP_PANEL_1V8_EN	IN 95 113
		33		34	LPDP_INT_HPD	OUT 10 16 113 137
			PWR		HPD NEEDS TO HAVE A 47K PD ON SOC SIDE	
PP3V8_AWAKESW_TCON_ISNS		37		38	PP3V8_AWAKESW_TCON_ISNS	94 129
			GND			
		39		40		
		41		42		
		43		44		
		45		46		
		47		48		
		49		50		
		51		52		
		53		54		
		55		56		

PLACEHOLDER RC FILTERS <RDAR://71288765>

SPI_TCON_MISO_CONN	RP633 0	SPI_TCON_MISO OUT 8 135
SPI_TCON_MOSI_CONN	RP632 0	SPI_TCON_MOSI IN 14
SPI_TCON_CLK_CONN	RP631 0	SPI_TCON_CLK IN 14

All 0: 0% 1/20W TK 0201

NOSTUFF CP631 12PF 5% 50V C0G-CERM 0201

NOSTUFF CP632 12PF 5% 50V C0G-CERM 0201

NOSTUFF CP633 12PF 5% 50V C0G-CERM 0201

PP1V25_AWAKE_IO

DBG_TCON_UART CP6A0 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

DBG_TCON_UART 311S00246 UP6A0 SN74AUP1G17 SON

UART_TCON_D2R_1V8 → DBG_TCON_UART RP6A0 100K 5% 1/20W TK 0201 117S00095

UART_TCON_D2R → OUT 7 134

NC

BOM_COST_GROUP=DISPLAY

PAGE TITLE	DISPLAY CONNECTOR
	Apple Inc.
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*** OK2INTEGRATE ***

125 PP3V8_AON

CP730 1.0UF 20% 6.3V X5R 0201-1

CRITICAL

UP730 TLV758P WSON-THICKSTNCL

IN 6 | OUT 1 | EN 4 | FB 2 | DNC 5 | NC | GND 3 | EPAD 7

3V29 FEED TO BACKLIGHT

PP3V29_BCON_AWAKESW

RP732 49.9K 1% 1/20W TK 0201

FB_BLKT_2D

RP731 10K 1% 1/20W TK 0201

VOUT = VFB * (1 + R1/R2)
VOUT = 0.55 * (1 + 49.9/10)
VOUT = 3.2945

CP731 0.1UF 10% 10V X5R-CERM 0201

CP732 10UF 20% 16V X5R-CERM 0402-7

NOSTUFF
RP730 0 0% 1/16W TK 0402

CP710 1.0UF 20% 6.3V X5R 0201-1

126 PP1V8_AON

BYPASS=UP710::4MM
CP770 0.1UF 10% 10V X5R-CERM 0201

CRITICAL

UP701 SLG5AP1564V STDFN

VDD 1 | ON 2 | D 3 | S 5 | PG 7 NC | GND 8

3V8 FEED TO MDB

PP3V8_AWAKESW_TCON 128

CP718 0.1UF 10% 10V X5R-CERM 0201

CP719 10UF 20% 16V X5R-CERM 0402-7

UP710 SLG4AP44015 STQFN

VDD 1 | GND 9

46 IN LCD_PWR_EN → LCD_EN_IN 2

130 81 47 IN PMU_SYS_ALIVE_1V8 → SYS_ALIVE 3

NC 5 NC | NC 6 NC | NC 7 NC | NC 8 NC | NC 12 NC | NC 14 NC

LCD_EN_OUT 11 → EDP_PANEL_1V8_EN OUT 94 113

PANEL_3V8_EN 4 → EDP_PANEL_PWR_EN

BLC_1V29_EN 13 → EDP_BKLT_1V29_EN OUT 91

CONTROLS 1.29V LDO IN PMIC

PANEL_DISCHARGE 10 → EDP_PANEL_DISCHARGE

RP700 300 5% 1/16W TK 0402

PPPANEL_PANEL_DISCHARGE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=4V

DMN2250UFB DFN1006-3 QP700

RP701 100K 5% 1/20W TK 0201

BOM_COST_GROUP=DISPLAY

PAGE TITLE: DISPLAY POWER SEQUENCER

Apple Inc.

DRAWING NUMBER: 051-07754 | SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

PAGE: 237 OF 999

SHEET: 95 OF 147

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*** OK2INTEGRATE***

CP800 AND CP801 MUST BE MIRRORED

CP834 AND CP835 MUST BE MIRRORED

RP850 0.01 MF 1W 0.5% 0612-1-COMBO

PPBUS_AON_BKLT_ISNS → RP850 → PPLUXE_INPUT_R_V VOLTAGE=13.1V

NOSTUFF CP800 10UF 20% 16V CER-X6S 0603

NOSTUFF CP801 10UF 20% 16V CER-X6S 0603

128S00009 CAPDERATE CP802 33UF 20% 16V TANT CASE-T POLY-TANT PACK_OPTION=POLY_PBUS:16V PACK_OPTION=POLY_PBUS:16V

128S00009 CAPDERATE CP803 33UF 20% 16V TANT CASE-T POLY-TANT

128S00107 CAPDERATE CP802 27UF 20% 18V TANT-POLY CASE-B12 POLY-TANT PACK_IGNORE=TRUE PACK_OPTION=POLY_PBUS:18V PACK_OPTION=POLY_PBUS:18V

128S00107 CAPDERATE CP803 27UF 20% 18V TANT-POLY CASE-B12 POLY-TANT

LUXE_ISH_P — RP801 0 0% 1/20W TK 0201 — LUXE_ISH_R_P

LUXE_ISH_N — RP802 0 0% 1/20W TK 0201 — LUXE_ISH_R_N

QP800 BSZ099N06LS5 PG-TSDSON-COMBO-1 CRITICAL

QP801 BSZ099N06LS5 PG-TSDSON-COMBO-1 CRITICAL

QP802 BSZ099N06LS5 PG-TSDSON-COMBO-1 CRITICAL

QP803 BSZ099N06LS5 PG-TSDSON-COMBO-1 CRITICAL

4LUXE_UG1 — RP832 2.49 1% 1/16W TK 0402

LUXE_UG2 4 — RP833 2.49 1% 1/16W TK 0402

4LUXE_LG1 — RP831 2.49 1% 1/16W TK 0402

LUXE_LG2 4 — RP830 2.49 1% 1/16W TK 0402

LP800 2.2UH-20%-8.0A-0.0501OHM PIMS052T-SM

PPLUXE_LX1 VOLTAGE=10V SWITCH_NODE=TRUE GATE_NODE=TRUE DIDT=TRUE

PPLUXE_LX2 VOLTAGE=10V SWITCH_NODE=TRUE GATE_NODE=TRUE DIDT=TRUE

PPLUXE_LG1_S VOLTAGE=1V

PPVOUT_LUXE_XW VOLTAGE=15V

XWP801 SM — PPVOUT_LUXE VOLTAGE=15V

CP830 10UF 20% 25V TANT CASE-T-SM POLY-TANT

CP831 10UF 20% 25V TANT CASE-T-SM POLY-TANT

CP832 10UF 20% 25V TANT CASE-T-SM POLY-TANT

CP833 10UF 20% 25V TANT CASE-T-SM POLY-TANT

CP834 0.1UF 20% 50V C0G 1206

CP835 0.1UF 20% 50V C0G 1206

RP803 0 0% 1/20W TK 0201 — LUXE_ISL_R_P / LUXE_ISL_P

RP809 0.01 0.5% 1W MF 0612-1-COMBO

RP804 0 0% 1/20W TK 0201 — LUXE_ISL_R_N / LUXE_ISL_N

CP823 0.1UF 10% 25V X5R 402 — LUXE_BT_C1

CP822 0.1UF 10% 25V X5R 402 — LUXE_BT_C2

RP820 4.32K 1% 1/16W TK 0402 — LUXE_COMP_R

CP820 0.022UF 20% 16V X7R-CERM 0402

CP821 56PF 5% 50V CERM 0402 — LUXE_AGND

LUXE_COMP

RP860 100K 5% 1/20W TK 0201 — LUXE_FAULT

PP1V25_AWAKE_IO

PP5V_S2_HOLD

RP881 0 0% 1/20W TK 0201 — BKLT_BOOST_THROTTLE_L / BKLT_BOOST_THROTTLE_R_L (OUT)

OD SIGNAL.
47K PU IS ON THE BCON CONNECTOR PAGE

PVOUT_LUXE_R

RP880 0 0% 1/20W TK 0201

CP880 12PF 5% 50V C0G-CERM 0201 NOSTUFF — LUXE_AGND

RP805 10 5% 1/16W TK 0402

CP870 2.2UF 20% 25V X5R-CERM 0402-1

PLACE_NEAR=UP800.C2:5MM

UP800 RAA209100B WLCSP OMIT_TABLE

C5, C2	VGD		
F2	C_VDD	LUXE_C_VDD VOLTAGE=2.5V	
F3	VDDA	PP5V_S2_HOLD_LUXE_VDDA VOLTAGE=5V	
E2	VIN	PPBUS_AON_BKLT_ISNS	
F6	VDDIO	PP1V25_AWAKE_IO	
D2	FAULT		
B2	BT_C1		
A1	UG1		
A2	LX1		
A3	LG1		
A4	LG2		
A5	LX2		
A6	UG2		
B5	BT_C2		
E6	COMP		
C6	THROTTLE		
D6	FB		
B4, B3	PGND		
D4	DGND		
E3, B6, B1	AGND	LUXE_AGND VOLTAGE=0V	
D5	VPROG_TEST		
E5	SCL		
E4	SDA		
F5	SCLK		
F4	SDATA		
D3	EN		
C3	BYP		
C4	TEST		
E1	ISH_P		
F1	ISH_N		
C1	ISL_P		
D1	ISL_N		

XWP800 SM — PGND, DGND, AGND

CP810 2.2UF 20% 25V X5R-CERM 0402-1

CP811 2.2UF 20% 25V X5R-CERM 0402-1

CP812 2.2UF 20% 25V X5R-CERM 0402-1

LUXE_AGND

RP840 100K 5% 1/20W TK 0201 NOSTUFF — LUXE_VPROG_TEST

RP842 100K 1/20W TK 5% 0201

RP841 100K 1/20W 5% TK 0201

RP870 10K 5% 1/20W TK 0201 — LUXE_AGND

RP871 10K 5% 1/20W TK 0201 — LUXE_BYP

RP872 10K 5% 1/20W TK 0201 — LUXE_TEST

I2C_LUXE_DEBUG_SCL (IN)

I2C_LUXE_DEBUG_SDA (BI)

SPMI_DISP_BKLT_CLK (IN)

SPMI_DISP_BKLT_DATA (BI)

BL_PWR_EN (IN) — RP873 0 1/20W 0% TK 0201 — BL_PWR_EN_R

LUXE_AGND

NOSTUFF CP813 33PF 5% 25V NP0-C0G 0201

NOSTUFF CP814 33PF 5% 25V NP0-C0G 0201

NOSTUFF CP815 100PF 5% 50V C0G 0402

NOSTUFF CP816 100PF 5% 50V C0G 0402

CP817 100PF 5% 50V C0G 0402

CP818 100PF 5% 50V C0G 0402

LUXE_AGND

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S02811	1	IC,RAA209100,A1,BUCK-BOOST CTRLR,WLCSP36	UP800	

BOM_COST_GROUP=DISPLAY

PAGE TITLE: LUXE LCD Backlight Driver

Apple Inc.

DRAWING NUMBER: 051-07754 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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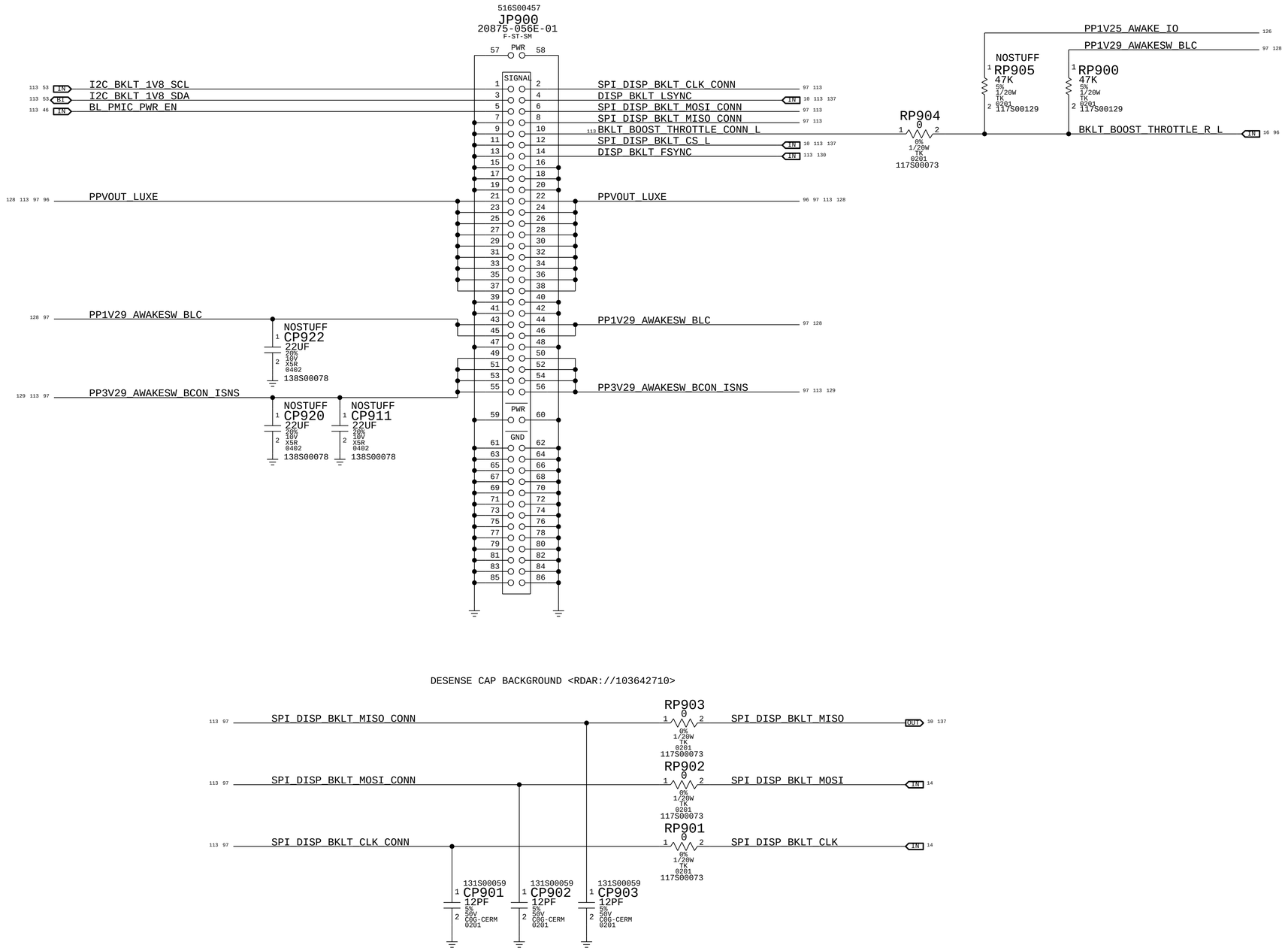

BOM_COST_GROUP=DISPLAY

PAGE TITLE: BCON CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-07754 | SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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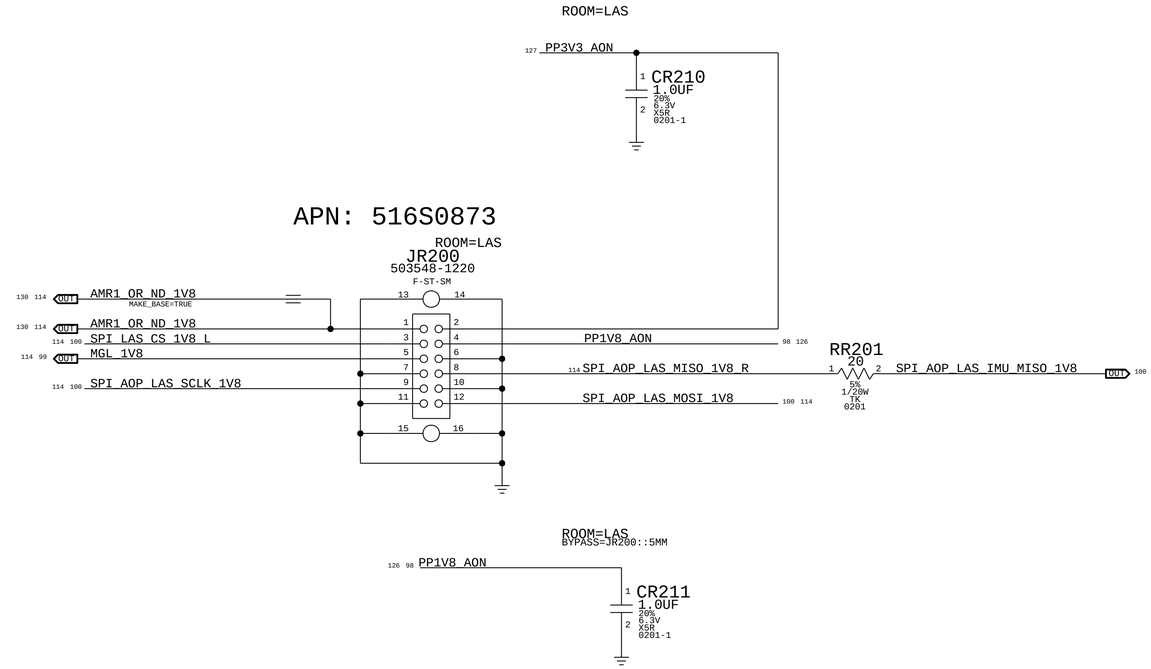
*** OK2INTEGRATE ***



CURRENT PER RAIL

RAIL	TYPICAL	PEAK
1.2 S2	22UA	1.2MA
1.8 AON	30UA	8 MA
3.3 AON	1UA	10 MA

BOM_COST_GROUP=SOC

PAGE TITLE
SECDIS: LID ANGLE SENSOR

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DRAWING NUMBER 051-07754 SIZE D
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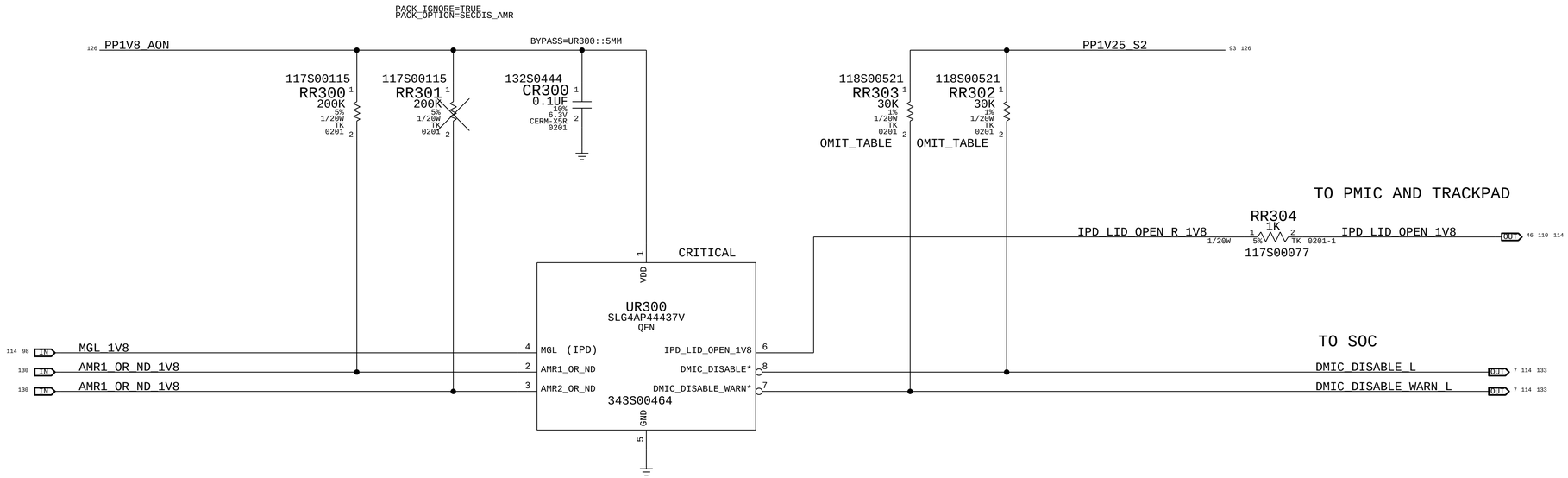
*** OK2INTEGRATE ***

LID SECDIS LOGIC



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00129	1	RES,TK,47K OHM,5%,1/20W,0201	RR302,RR303	CRITICAL	REFSECDIS_SOC_PU:47K
118S00521	1	RES,TK,30K OHM,1%,1/20W,0201	RR302,RR303	CRITICAL	REFSECDIS_SOC_PU:30K

BOM_COST_GROUP=SOC

PAGE TITLE
SECDIS: SAK

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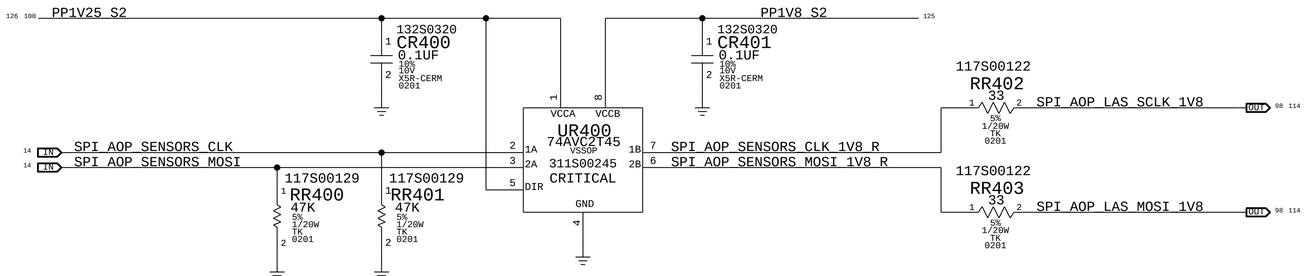
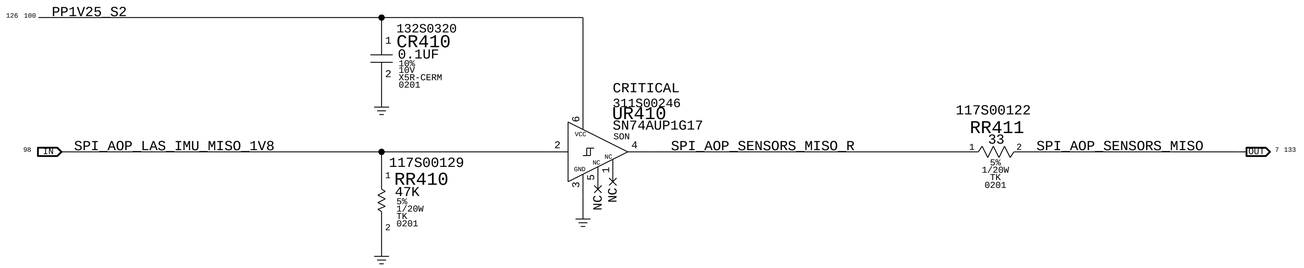
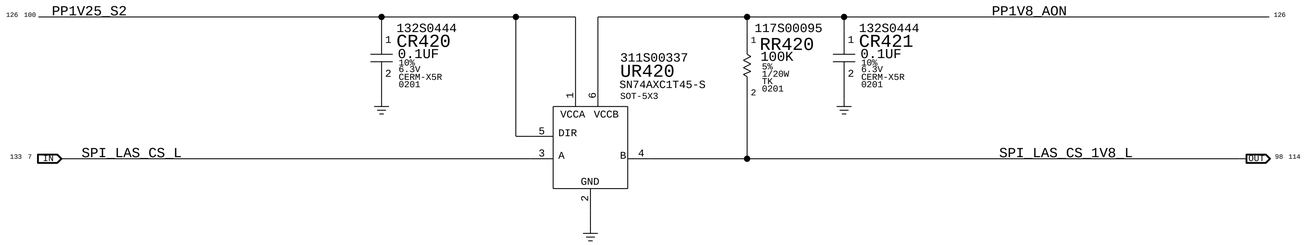
LAS SPI LEVEL SHIFTERS







BOM_COST_GROUP=SOC

PAGE TITLE: SECDIS: SUPPORT

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REVISION: 6.0.0
BRANCH: dvt-1
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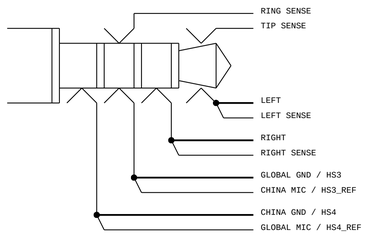
*** OK2INTEGRATE ***

CARLOW CODEC I2C ADDRESS	
ADDR PIN	ADDRESS
0R TO GND	0X48
100K TO GND	0X49
100K TO VDDIO	0X4A
0R TO VDDIO	0X4B <--

AUDIO JACK PINOUT



TO / FROM
AUDIO JACK
CONNECTOR

NOTES:

- SEE TEST POINT SIGNALS & LOCATIONS ON REF DESIGN PAGE 1

- THE FOLLOWING SIGNALS SHOULD HAVE A LOW DCR PATH:
  - VP SUPPLY
  - VCP SUPPLY
  - AUDIO_JACK_LEFT/RIGHT_OUT
  - AUDIO_JACK_GB/CH_GND

- GB_MIC SIGNAL CONNECTS TO CH_GND AT A/J CONNECTOR.
  CH_MIC SIGNAL CONNECTS TO GB_GND AT A/J CONNECTOR.

- VP SUPPLY RAIL ACCEPTS 3.0V TO 5.25V AND NEEDS TO
  COME UP FIRST AND TURN OFF LAST (NEED TO STAY UP
  WHEN THE OTHER RAILS GO DOWN)
  VP CURRENT CONSUMPTION WITH PART IN LOWEST POWER STATE:
  3.1UA (1V8 OFF, RST# LOW)
  TBD (1V8 ON, RST# LOW)
  37UA (1V8 OFF, RST# HIGH)

CARLOW B0 SILICON

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO JACK CODEC

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*** OK2INTEGRATE ***

AMP A

PP1V8_AWAKE
PP1V25_AWAKE_IO
SPKRAMP_A_DREG
CR600 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR600.E5:5MM)
CR601 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR600.F3:5MM)
CR602 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR600.C2:5MM)

UR600 SN012776B0B DSBGA — TAWANG B0B — SPKRAMP_A

DREG	C2	
SCL	F2	I2C_SPKRAMP_L_CODEC_SCL
SDA	F1	I2C_SPKRAMP_L_CODEC_SDA
ADDR	D4	SPKRAMP_A_ADDR
SBCLK	E1	TDM_SPKRAMP_L_BCLK
FSYNC	D2	TDM_SPKRAMP_L_FSYNC
SDIN	E2	TDM_SPKRAMP_L_R2D
SDOUT	D1	TDM_SPKRAMP_L_D2R
ICC	F5	SPKRAMP_ABC_ICC
BYP_EN	D3	TP_SPKRAMP_A_LV_EN
IRQ*	E3	SPKRAMP_INT_L
SD*	F4	SPKRAMP_RESET_L
PVDD_SNS	C3	SPKRAMP_A_PVDD_SNS
VSNS_P	B1	SPKRAMP_A_VSENSEP
VSNS_N	A1	SPKRAMP_A_VSENSEN
BST_P	B2	SPKRAMP_A_BOOTP
OUT_P	B3	SPKRAMP_A_OUTP_R
OUT_P	A3	
OUT_N	B5	SPKRAMP_A_OUTN_R
OUT_N	A5	
BST_N	A2	SPKRAMP_A_BOOTN
AVDD	E5	
PVDD	C4	
PVDD	C5	
VBAT1S	D5	
IOVDD	F3	
GND	E4	
GND	C1	
PGND	B4	
PGND	A4	

SPKRAMP_A_BYPASS=UR600.B2:B3:10MM NO_XNET_CONNECTION=1

CR603 0.1UF 10% 25V X5R 0201 (SPKRAMP_A PLACE_NEAR=UR600.C5:5MM)
CR604 10UF 20% 25V X5R-CERM 0603 (SPKRAMP_A PLACE_NEAR=UR600.C5:10MM)
CR605 10UF 20% 25V X5R-CERM 0603 (SPKRAMP_A PLACE_NEAR=UR600.C5:10MM)
CR606 0.1UF 10% 25V X5R 0201 (SPKRAMP_A PLACE_NEAR=UR600.D5:5MM)
CR607 10UF 20% 10V X5R-CERM 0402-7 (SPKRAMP_A PLACE_NEAR=UR600.D5:10MM)

PP3V8_AON_SPKRAMP_LEFT_ISNS MAX CURRENT EDC = 1A (PER AMP)
PPBUS_SPKRAMP_LEFT_ISNS MAX CURRENT EDC = 4A (PER AMP)
XWR600 SHORT-18L-0.1MM-SM * SEE NOTE
SPKRAMP_A_PVDD_SNS
SPKRAMP_A_VSENSEP * SEE NOTE
SPKRAMP_A_VSENSEN

CR608 0.1UF 10% 25V X5R 0201 (SPKRAMP_A_BOOTP MIN_LINE_WIDTH=0.1000)
CR609 0.1UF 10% 25V X5R 0201 (SPKRAMP_A_BOOTN MIN_LINE_WIDTH=0.1000)
RR602 0 1% 1/16W TK 0603 1/5W (SPKRAMP_A_OUTP_R MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE) * SEE NOTE
RR603 0 1% 1/16W TK 0603 1/5W (SPKRAMP_A_OUTN_R MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE) * SEE NOTE
SPKRAMP_A_OUTP * SEE NOTE
SPKRAMP_A_OUTN * SEE NOTE
CR610 12PF 5% 25V CERM 0201 OMIT_TABLE
CR611 12PF 5% 25V CERM 0201 OMIT_TABLE

RR600 33 5% 1/20W TK 0201 (SPKRAMP_A TDM_SPKRAMP_A_D2R_R PLACE_NEAR=UR600.D1:10MM)
RR601 33 5% 1/20W TK 0201 (SPKRAMP_A SPKRAMP_A_ICC_R PLACE_NEAR=UR600.E5:10MM)

RR605 0 5% 1/20W TK 0201 (SPKRAMP_A_ADDR 0x70)
RR635 470 5% 1/20W TK 0201 (SPKRAMP_B_ADDR 0x72)
RR664 470 5% 1/20W TK 0201 (SPKRAMP_C_ADDR 0x74)

AMP B

PP1V8_AWAKE
PP1V25_AWAKE_IO
SPKRAMP_B_DREG
CR630 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR630.E5:5MM)
CR631 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR630.F3:5MM)
CR632 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR630.C2:5MM)

UR630 SN012776B0B DSBGA — TAWANG B0B — SPKRAMP_B

DREG	C2	
SCL	F2	I2C_SPKRAMP_L_CODEC_SCL
SDA	F1	I2C_SPKRAMP_L_CODEC_SDA
ADDR	D4	SPKRAMP_B_ADDR
SBCLK	E1	TDM_SPKRAMP_L_BCLK
FSYNC	D2	TDM_SPKRAMP_L_FSYNC
SDIN	E2	TDM_SPKRAMP_L_R2D
SDOUT	D1	TDM_SPKRAMP_L_D2R
ICC	F5	SPKRAMP_ABC_ICC
BYP_EN	D3	TP_SPKRAMP_B_LV_EN
IRQ*	E3	SPKRAMP_INT_L
SD*	F4	SPKRAMP_RESET_L
PVDD_SNS	C3	SPKRAMP_B_PVDD_SNS
VSNS_P	B1	SPKRAMP_B_VSENSEP
VSNS_N	A1	SPKRAMP_B_VSENSEN
BST_P	B2	SPKRAMP_B_BOOTP
OUT_P	B3	SPKRAMP_B_OUTP_R
OUT_P	A3	
OUT_N	B5	SPKRAMP_B_OUTN_R
OUT_N	A5	
BST_N	A2	SPKRAMP_B_BOOTN
AVDD	E5	
PVDD	C4	
PVDD	C5	
VBAT1S	D5	
IOVDD	F3	
GND	E4	
GND	C1	
PGND	B4	
PGND	A4	

SPKRAMP_B_BYPASS=UR630.B2:B3:10MM NO_XNET_CONNECTION=1

CR633 0.1UF 10% 25V X5R 0201 (SPKRAMP_B PLACE_NEAR=UR630.C5:5MM)
CR634 10UF 20% 25V X5R-CERM 0603 (SPKRAMP_B PLACE_NEAR=UR630.C5:10MM)
CR635 10UF 20% 25V X5R-CERM 0603 (SPKRAMP_B PLACE_NEAR=UR630.C5:10MM)
CR636 0.1UF 10% 25V X5R 0201 (SPKRAMP_B PLACE_NEAR=UR630.D5:5MM)
CR637 10UF 20% 10V X5R-CERM 0402-7 (SPKRAMP_B PLACE_NEAR=UR630.D5:10MM)

PP3V8_AON_SPKRAMP_LEFT_ISNS
PPBUS_SPKRAMP_LEFT_ISNS
XWR601 SHORT-16L-0.1MM-SM * SEE NOTE
SPKRAMP_B_PVDD_SNS
SPKRAMP_B_VSENSEP * SEE NOTE
SPKRAMP_B_VSENSEN

CR638 0.1UF 10% 25V X5R 0201 (SPKRAMP_B_BOOTP MIN_LINE_WIDTH=0.1000)
CR639 0.1UF 10% 25V X5R 0201 (SPKRAMP_B_BOOTN MIN_LINE_WIDTH=0.1000)
RR632 0 1% 1/16W TK 0603 1/5W (SPKRAMP_B_OUTP_R MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE) * SEE NOTE
RR633 0 1% 1/16W TK 0603 1/5W (SPKRAMP_B_OUTN_R MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE) * SEE NOTE
SPKRAMP_B_OUTP * SEE NOTE
SPKRAMP_B_OUTN * SEE NOTE
CR640 12PF 5% 25V CERM 0201 OMIT_TABLE
CR641 12PF 5% 25V CERM 0201 OMIT_TABLE

RR630 33 5% 1/20W TK 0201 (SPKRAMP_B TDM_SPKRAMP_B_D2R_R PLACE_NEAR=UR630.D1:10MM)
RR631 33 5% 1/20W TK 0201 (SPKRAMP_B SPKRAMP_B_ICC_R PLACE_NEAR=UR630.E5:10MM)

PP1V25_AWAKE_IO
NOSTUFF RR691 47K 5% 1/20W TK 0201
SPKRAMP_INT_L
SPKRAMP_RESET_L
RR692 47K 5% 1/20W TK 0201

THIS RESISTOR TIES ICC SIGNAL BETWEEN AMPS A,B,C AND AMPS D,E,F:
0R --> GLOBAL ICC (ABCDEF)
DNE --> LOCAL ICC (ABC, DEF)

SPKRAMP_ICC_GB
RR693 0 0% 1/20W TK 0201
SPKRAMP_ABC_ICC — SPKRAMP_DEF_ICC

AMP C

PP1V8_AWAKE
PP1V25_AWAKE_IO
SPKRAMP_C_DREG
CR660 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR600.E5:5MM)
CR661 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR600.F3:5MM)
CR662 1.0UF 20% 6.3V X5R 0201-1 (PLACE_NEAR=UR600.C2:5MM)

UR660 SN012776B0B DSBGA — TAWANG B0B — SPKRAMP_C

DREG	C2	
SCL	F2	I2C_SPKRAMP_L_CODEC_SCL
SDA	F1	I2C_SPKRAMP_L_CODEC_SDA
ADDR	D4	SPKRAMP_C_ADDR
SBCLK	E1	TDM_SPKRAMP_L_BCLK
FSYNC	D2	TDM_SPKRAMP_L_FSYNC
SDIN	E2	TDM_SPKRAMP_L_R2D
SDOUT	D1	TDM_SPKRAMP_L_D2R
ICC	F5	SPKRAMP_ABC_ICC
BYP_EN	D3	TP_SPKRAMP_C_LV_EN
IRQ*	E3	SPKRAMP_INT_L
SD*	F4	SPKRAMP_RESET_L
PVDD_SNS	C3	SPKRAMP_C_PVDD_SNS
VSNS_P	B1	SPKRAMP_C_VSENSEP
VSNS_N	A1	SPKRAMP_C_VSENSEN
BST_P	B2	SPKRAMP_C_BOOTP
OUT_P	B3	SPKRAMP_C_OUTP_R
OUT_P	A3	
OUT_N	B5	SPKRAMP_C_OUTN_R
OUT_N	A5	
BST_N	A2	SPKRAMP_C_BOOTN
AVDD	E5	
PVDD	C4	
PVDD	C5	
VBAT1S	D5	
IOVDD	F3	
GND	E4	
GND	C1	
PGND	B4	
PGND	A4	

SPKRAMP_C_BYPASS=UR660.B2:B3:10MM NO_XNET_CONNECTION=1

CR663 0.1UF 10% 25V X5R 0201 (SPKRAMP_C PLACE_NEAR=UR660.C5:5MM)
CR664 10UF 20% 25V X5R-CERM 0603 (SPKRAMP_C PLACE_NEAR=UR660.C5:10MM)
CR665 10UF 20% 25V X5R-CERM 0603 (SPKRAMP_C PLACE_NEAR=UR660.C5:10MM)
CR666 0.1UF 10% 25V X5R 0201 (SPKRAMP_C PLACE_NEAR=UR660.D5:5MM)
CR667 10UF 20% 10V X5R-CERM 0402-7 (SPKRAMP_C PLACE_NEAR=UR660.D5:10MM)

PP3V8_AON_SPKRAMP_LEFT_ISNS
PPBUS_SPKRAMP_LEFT_ISNS
XWR602 SHORT-18L-0.1MM-SM * SEE NOTE
SPKRAMP_C_PVDD_SNS
SPKRAMP_C_VSENSEP * SEE NOTE
SPKRAMP_C_VSENSEN

CR668 0.1UF 10% 25V X5R 0201 (SPKRAMP_C_BOOTP MIN_LINE_WIDTH=0.1000)
CR669 0.1UF 10% 25V X5R 0201 (SPKRAMP_C_BOOTN MIN_LINE_WIDTH=0.1000)
RR662 0 1% 1/16W TK 0603 1/5W (SPKRAMP_C_OUTP_R MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE) * SEE NOTE
RR663 0 1% 1/16W TK 0603 1/5W (SPKRAMP_C_OUTN_R MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000 SWITCH_NODE=TRUE) * SEE NOTE
SPKRAMP_C_OUTP * SEE NOTE
SPKRAMP_C_OUTN * SEE NOTE
CR670 12PF 5% 25V CERM 0201 OMIT_TABLE
CR671 12PF 5% 25V CERM 0201 OMIT_TABLE

RR660 33 5% 1/20W TK 0201 (SPKRAMP_C TDM_SPKRAMP_C_D2R_R PLACE_NEAR=UR660.D1:10MM)
RR661 33 5% 1/20W TK 0201 (SPKRAMP_C SPKRAMP_C_ICC_R PLACE_NEAR=UR660.E5:10MM)

NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO AMPLIFIERS (1/2)

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*** OK2INTEGRATE ***

AMP D

PP1V8_AWAKE
PP1V25_AWAKE_IO
PP3V8_AON_SPKRAMP_RIGHT_ISNS (MAX CURRENT EDC = 1A (PER AMP))
PPBUS_SPKRAMP_RIGHT_ISNS (MAX CURRENT EDC = 4A (PER AMP))

CR700 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_D PLACE_NEAR=UR700.E5:5MM
CR701 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_D PLACE_NEAR=UR700.F3:5MM
CR702 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_D PLACE_NEAR=UR700.C2:5MM
SPKRAMP_D_DREG

CR703 0.1UF 10% 25V X5R 0201 — SPKRAMP_D PLACE_NEAR=UR700.C5:5MM
CR704 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_D PLACE_NEAR=UR700.C5:10MM
CR705 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_D PLACE_NEAR=UR700.C5:10MM
CR706 0.1UF 10% 25V X5R 0201 — SPKRAMP_D PLACE_NEAR=UR700.D5:5MM
CR707 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_D PLACE_NEAR=UR700.D5:10MM

XWR700 SHORT-10L-0.1MM-SM * SEE NOTE

UR700 SN012776B0B DSBGA SPKRAMP_D TAWANG B0B

C2	DREG	PVDD_SNS	C3
F2	SCL	VSNS_P	B1
F1	SDA	VSNS_N	A1
D4	ADDR	BST_P	B2
E1	SBCLK	OUT_P	B3
D2	FSYNC	OUT_P	A3
E2	SDIN	OUT_N	B5
D1	SDOUT	OUT_N	A5
F5	ICC	BST_N	A2
D3	BYP_EN		
E3	IRQ*		
F4	SD*		
E5	AVDD		
C4	PVDD		
C5	PVDD		
D5	VBAT1S		
F3	IOVDD		
E4	GND		
C1	GND		
B4	PGND		
A4	PGND		

SPKRAMP_D_VSENSEP * SEE NOTE → SPKRAMP_D IN 104
SPKRAMP_D_VSENSEN → SPKRAMP_D IN 104
SPKRAMP_D_PVDD_SNS

SPKRAMP_D_BOOTP — CR708 0.1UF 10% 25V X5R 0201 — MIN_LINE_WIDTH=0.1000
SPKRAMP_D_OUTP_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE
SPKRAMP_D_OUTN_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE
SPKRAMP_D_BOOTN — CR709 0.1UF 10% 25V X5R 0201 — MIN_LINE_WIDTH=0.1000
SPKRAMP_D BYPASS=UR700.B2:B3:10MM NO_XNET_CONNECTION=1

RR702 0 1% 1/16W TK 0603 1/5W — SPKRAMP_D — MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, SWITCH_NODE=TRUE
RR703 0 1% 1/16W TK 0603 1/5W — SPKRAMP_D — MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, SWITCH_NODE=TRUE

SPKRAMP_D_OUTP * SEE NOTE → SPKRAMP_D OUT 104 114
SPKRAMP_D_OUTN * SEE NOTE → SPKRAMP_D OUT 104 114

CR710 12PF 5% 25V CERM 0201 — SPKRAMP_D — OMIT_TABLE
CR711 12PF 5% 25V CERM 0201 — SPKRAMP_D — OMIT_TABLE

SPKRAMP_D I2C_HDMI_SPKRAMP_R_SCL (IN) → F2 SCL
SPKRAMP_D I2C_HDMI_SPKRAMP_R_SDA (BI) → F1 SDA
SPKRAMP_D_ADDR → D4 ADDR
SPKRAMP_D TDM_SPKRAMP_R_BCLK (IN) → E1 SBCLK
SPKRAMP_D TDM_SPKRAMP_R_FSYNC (IN) → D2 FSYNC
SPKRAMP_D TDM_SPKRAMP_R_R2D (IN) → E2 SDIN
SPKRAMP_D TDM_SPKRAMP_R_D2R (OUT) ← RR700 33 5% 1/20W TK 0201 ← TDM_SPKRAMP_D_D2R_R PLACE_NEAR=UR700.D1:10MM
SPKRAMP_DEF_ICC_R ← RR701 33 5% 1/20W TK 0201 ← SPKRAMP_D_ICC_R PLACE_NEAR=UR700.F5:10MM
TP_SPKRAMP_D_LV_EN → D3 BYP_EN
SPKRAMP_D SPKRAMP_INT_L (OUT) → E3 IRQ*
SPKRAMP_D SPKRAMP_RESET_L (IN) → F4 SD*

PP1V8_AWAKE → RR705 2.2K 5% 1/20W TK 0201 → SPKRAMP_D_ADDR 0X76
PP1V8_AWAKE → RR734 2.2K 5% 1/20W TK 0201 → SPKRAMP_E_ADDR 0X78
PP1V8_AWAKE → RR765 10K 5% 1/20W TK 0201 → SPKRAMP_F_ADDR 0X7A

SPKRAMP_DEF_ICC → RR706 0 0% 1/20W TK 0201 → SPKRAMP_DEF_ICC_R
RR707 0 0% 1/20W TK 0201 NOSTUFF

RR706 TO REDUCE STUB LENGTH FOR LOCAL ICC OPERATION. RR707 PROVIDES THE OPTION TO GND FLOATING SPKRAMP_DEF_ICC TRACE

AMP E

PP1V8_AWAKE
PP1V25_AWAKE_IO
PP3V8_AON_SPKRAMP_RIGHT_ISNS
PPBUS_SPKRAMP_RIGHT_ISNS

CR730 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_E PLACE_NEAR=UR730.E5:5MM
CR731 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_E PLACE_NEAR=UR730.F3:5MM
CR732 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_E PLACE_NEAR=UR730.C2:5MM
SPKRAMP_E_DREG

CR733 0.1UF 10% 25V X5R 0201 — SPKRAMP_E PLACE_NEAR=UR730.C5:5MM
CR734 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_E PLACE_NEAR=UR730.C5:10MM
CR735 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_E PLACE_NEAR=UR730.C5:10MM
CR736 0.1UF 10% 25V X5R 0201 — SPKRAMP_E PLACE_NEAR=UR730.D5:5MM
CR737 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_E PLACE_NEAR=UR730.D5:10MM

XWR701 SHORT-10L-0.1MM-SM * SEE NOTE

UR730 SN012776B0B DSBGA SPKRAMP_E TAWANG B0B

C2	DREG	PVDD_SNS	C3
F2	SCL	VSNS_P	B1
F1	SDA	VSNS_N	A1
D4	ADDR	BST_P	B2
E1	SBCLK	OUT_P	B3
D2	FSYNC	OUT_P	A3
E2	SDIN	OUT_N	B5
D1	SDOUT	OUT_N	A5
F5	ICC	BST_N	A2
D3	BYP_EN		
E3	IRQ*		
F4	SD*		
E5	AVDD		
C4	PVDD		
C5	PVDD		
D5	VBAT1S		
F3	IOVDD		
E4	GND		
C1	GND		
B4	PGND		
A4	PGND		

SPKRAMP_E_VSENSEP * SEE NOTE → SPKRAMP_E IN 104
SPKRAMP_E_VSENSEN → SPKRAMP_E IN 104
SPKRAMP_E_PVDD_SNS

SPKRAMP_E_BOOTP — CR738 0.1UF 10% 25V X5R 0201 — MIN_LINE_WIDTH=0.1000
SPKRAMP_E_OUTP_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE
SPKRAMP_E_OUTN_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE
SPKRAMP_E_BOOTN — CR739 0.1UF 10% 25V X5R 0201 — MIN_LINE_WIDTH=0.1000
SPKRAMP_E BYPASS=UR730.B2:B3:10MM NO_XNET_CONNECTION=1

RR732 0 1% 1/16W TK 0603 1/5W — SPKRAMP_E — MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, SWITCH_NODE=TRUE
RR733 0 1% 1/16W TK 0603 1/5W — SPKRAMP_E — MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, SWITCH_NODE=TRUE

SPKRAMP_E_OUTP * SEE NOTE → SPKRAMP_E OUT 104 114
SPKRAMP_E_OUTN * SEE NOTE → SPKRAMP_E OUT 104 114

CR740 12PF 5% 25V CERM 0201 — SPKRAMP_E — OMIT_TABLE
CR741 12PF 5% 25V CERM 0201 — SPKRAMP_E — OMIT_TABLE

SPKRAMP_E I2C_HDMI_SPKRAMP_R_SCL (IN) → F2 SCL
SPKRAMP_E I2C_HDMI_SPKRAMP_R_SDA (BI) → F1 SDA
SPKRAMP_E_ADDR → D4 ADDR
SPKRAMP_E TDM_SPKRAMP_R_BCLK (IN) → E1 SBCLK
SPKRAMP_E TDM_SPKRAMP_R_FSYNC (IN) → D2 FSYNC
SPKRAMP_E TDM_SPKRAMP_R_R2D (IN) → E2 SDIN
SPKRAMP_E TDM_SPKRAMP_R_D2R (OUT) ← RR730 33 5% 1/20W TK 0201 ← TDM_SPKRAMP_E_D2R_R PLACE_NEAR=UR730.D1:10MM
SPKRAMP_DEF_ICC_R ← RR731 33 5% 1/20W TK 0201 ← SPKRAMP_E_ICC_R PLACE_NEAR=UR730.F5:10MM
TP_SPKRAMP_E_LV_EN → D3 BYP_EN
SPKRAMP_E SPKRAMP_INT_L (OUT) → E3 IRQ*
SPKRAMP_E SPKRAMP_RESET_L (IN) → F4 SD*

AMP F

PP1V8_AWAKE
PP1V25_AWAKE_IO
PP3V8_AON_SPKRAMP_RIGHT_ISNS
PPBUS_SPKRAMP_RIGHT_ISNS

CR760 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_F PLACE_NEAR=UR760.E5:5MM
CR761 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_F PLACE_NEAR=UR760.F3:5MM
CR762 1.0UF 20% 6.3V X5R 0201-1 — SPKRAMP_F PLACE_NEAR=UR760.C2:5MM
SPKRAMP_F_DREG

CR763 0.1UF 10% 25V X5R 0201 — SPKRAMP_F PLACE_NEAR=UR760.C5:5MM
CR764 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_F PLACE_NEAR=UR760.C5:10MM
CR765 10UF 20% 25V X5R-CERM 0603 — SPKRAMP_F PLACE_NEAR=UR760.C5:10MM
CR766 0.1UF 10% 25V X5R 0201 — SPKRAMP_F PLACE_NEAR=UR760.D5:5MM
CR767 10UF 20% 10V X5R-CERM 0402-7 — SPKRAMP_F PLACE_NEAR=UR760.D5:10MM

XWR702 SHORT-10L-0.1MM-SM * SEE NOTE

UR760 SN012776B0B DSBGA SPKRAMP_F TAWANG B0B

C2	DREG	PVDD_SNS	C3
F2	SCL	VSNS_P	B1
F1	SDA	VSNS_N	A1
D4	ADDR	BST_P	B2
E1	SBCLK	OUT_P	B3
D2	FSYNC	OUT_P	A3
E2	SDIN	OUT_N	B5
D1	SDOUT	OUT_N	A5
F5	ICC	BST_N	A2
D3	BYP_EN		
E3	IRQ*		
F4	SD*		
E5	AVDD		
C4	PVDD		
C5	PVDD		
D5	VBAT1S		
F3	IOVDD		
E4	GND		
C1	GND		
B4	PGND		
A4	PGND		

SPKRAMP_F_VSENSEP * SEE NOTE → SPKRAMP_F IN 104
SPKRAMP_F_VSENSEN → SPKRAMP_F IN 104
SPKRAMP_F_PVDD_SNS

SPKRAMP_F_BOOTP — CR768 0.1UF 10% 25V X5R 0201 — MIN_LINE_WIDTH=0.1000
SPKRAMP_F_OUTP_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE
SPKRAMP_F_OUTN_R — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1000, SWITCH_NODE=TRUE
SPKRAMP_F_BOOTN — CR769 0.1UF 10% 25V X5R 0201 — MIN_LINE_WIDTH=0.1000
SPKRAMP_F BYPASS=UR760.B2:B3:10MM NO_XNET_CONNECTION=1

RR762 0 1% 1/16W TK 0603 1/5W — SPKRAMP_F — MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, SWITCH_NODE=TRUE
RR763 0 1% 1/16W TK 0603 1/5W — SPKRAMP_F — MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000, SWITCH_NODE=TRUE

SPKRAMP_F_OUTP * SEE NOTE → SPKRAMP_F OUT 104 114
SPKRAMP_F_OUTN * SEE NOTE → SPKRAMP_F OUT 104 114

CR770 12PF 5% 25V CERM 0201 — SPKRAMP_F — OMIT_TABLE
CR771 12PF 5% 25V CERM 0201 — SPKRAMP_F — OMIT_TABLE

SPKRAMP_F I2C_HDMI_SPKRAMP_R_SCL (IN) → F2 SCL
SPKRAMP_F I2C_HDMI_SPKRAMP_R_SDA (BI) → F1 SDA
SPKRAMP_F_ADDR → D4 ADDR
SPKRAMP_F TDM_SPKRAMP_R_BCLK (IN) → E1 SBCLK
SPKRAMP_F TDM_SPKRAMP_R_FSYNC (IN) → D2 FSYNC
SPKRAMP_F TDM_SPKRAMP_R_R2D (IN) → E2 SDIN
SPKRAMP_F TDM_SPKRAMP_R_D2R (OUT) ← RR760 33 5% 1/20W TK 0201 ← TDM_SPKRAMP_F_D2R_R PLACE_NEAR=UR760.D1:10MM
SPKRAMP_DEF_ICC_R ← RR761 33 5% 1/20W TK 0201 ← SPKRAMP_F_ICC_R PLACE_NEAR=UR760.F5:10MM
TP_SPKRAMP_F_LV_EN → D3 BYP_EN
SPKRAMP_F SPKRAMP_INT_L (OUT) → E3 IRQ*
SPKRAMP_F SPKRAMP_RESET_L (IN) → F4 SD*

NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.

BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO AMPLIFIERS (2/2)

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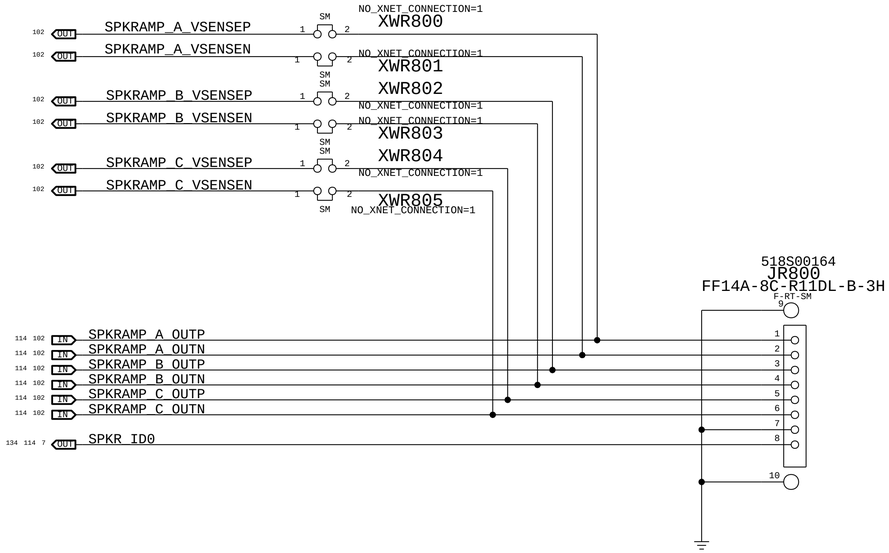
LEFT AUDIO SPEAKER CONNECTOR

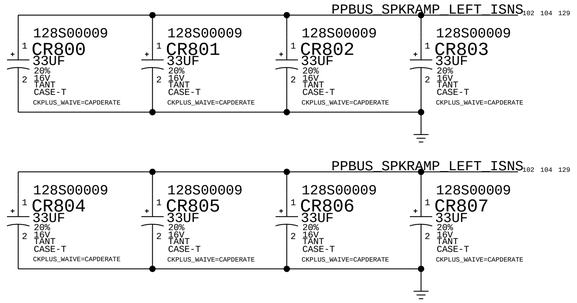
L WOOFER 1

L WOOFER 2

L TWEETER



LEFT AMPLIFIERS BULK CAPACITANCE

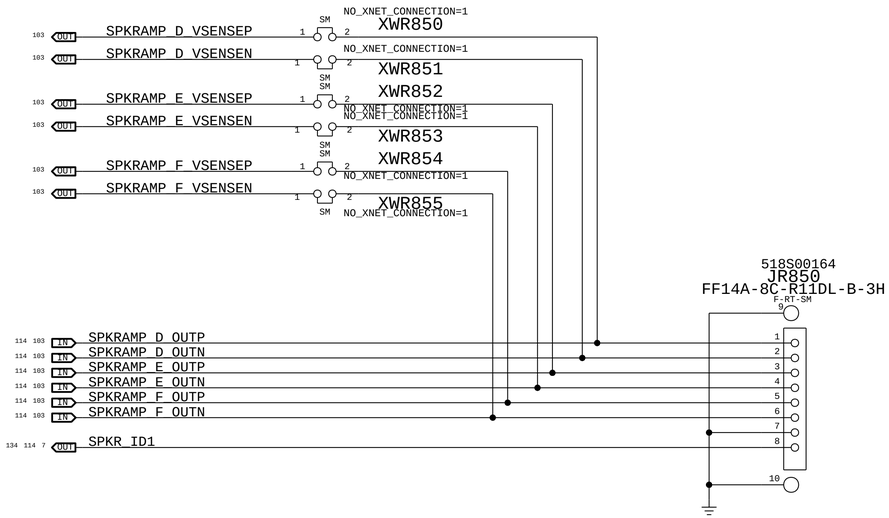


RIGHT AUDIO SPEAKER CONNECTOR

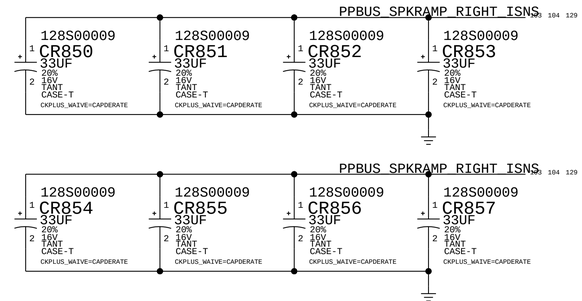
R WOOFER 1

R WOOFER 2

R TWEETER



RIGHT AMPLIFIERS BULK CAPACITANCE



BOM_COST_GROUP=AUDIO

PAGE TITLE
AUDIO CONNECTORS: AMPS

Apple Inc.

DRAWING NUMBER 051-07754 | SIZE D
REVISION 6.0.0
BRANCH dvt-1
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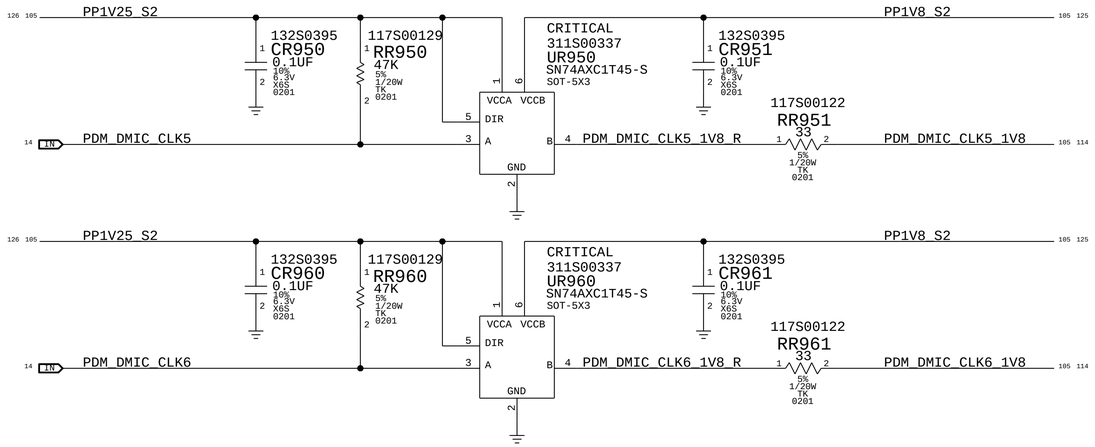
LEVEL SHIFTERS: DMIC CLOCK

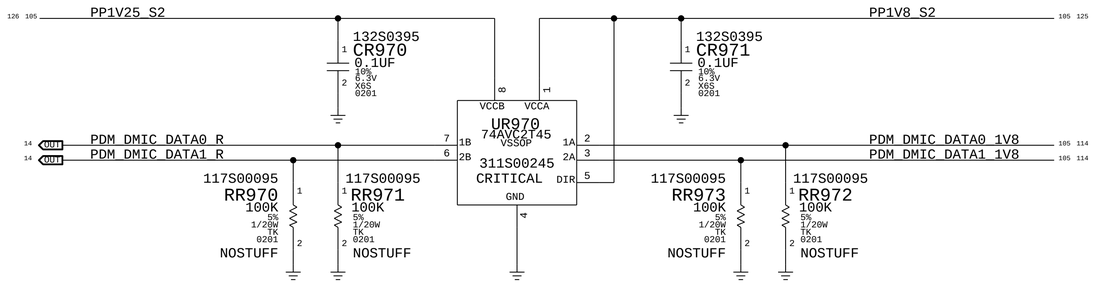
TWO SEPARATE SINGLE BIT LS FOR XTALK CONCERNS <RDAR://70058941>



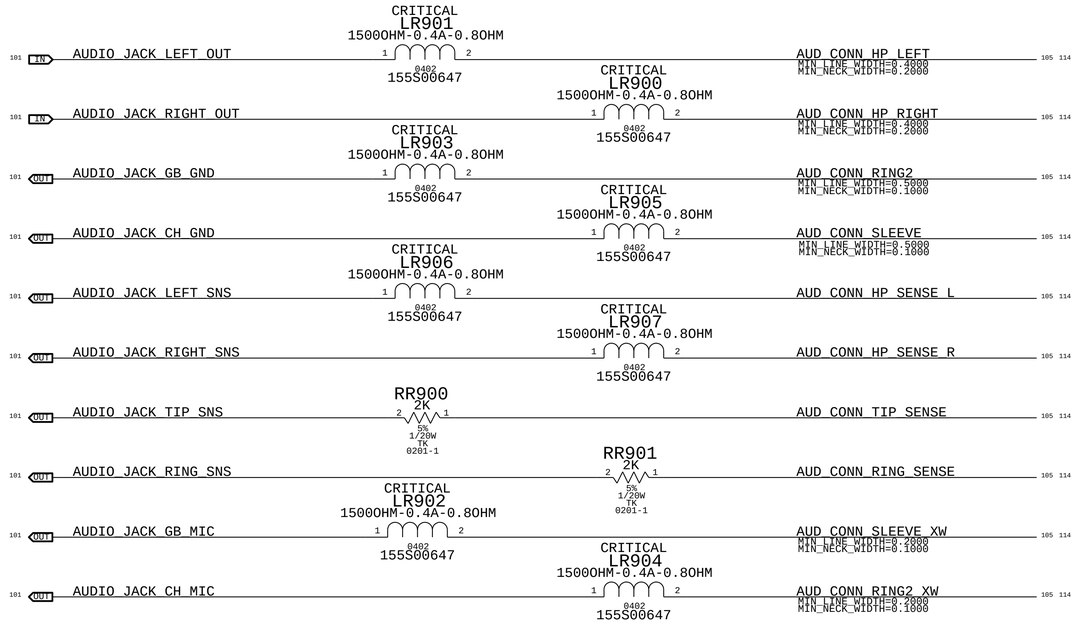
LEVEL SHIFTER: DMIC DATA

HIGH ON DIR IS A -> B

BOTH A AND B SIDE CAN BE ANY VOLTAGE FROM 0.8 TO 3.6

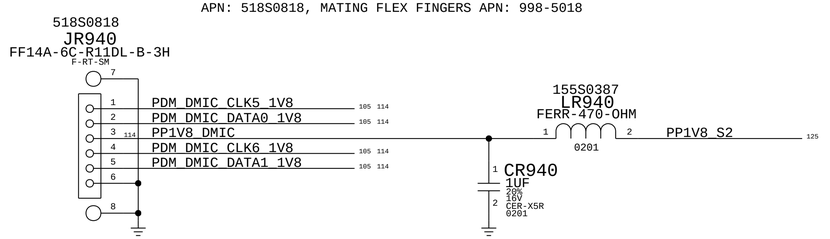


AJ FLEX FILTERS



DIGITAL MIC FLEX CONNECTOR

APN: 518S0818, MATING FLEX FINGERS APN: 998-5018

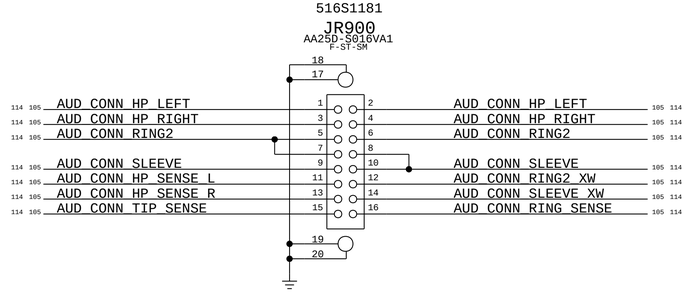


PDM DATA0 / CLK5
MIC1 (REAR MIC): DATA DRIVEN AFTER FALLING CLK EDGE
MIC2 (FRONT MIC): DATA DRIVE AFTER RISING CLK EDGE

PDM DATA1 / CLK6
MIC2 (OFFSET MIC): DATA DRIVE AFTER FALLING CLK EDGE

AUDIO JACK FLEX CONNECTOR

APN: 516S1181, MATING PLUG APN:516S1180
SAME AS J214



BOM_COST_GROUP=AUDIO

PAGE TITLE: AUDIO CONNECTORS: AJ & DMIC

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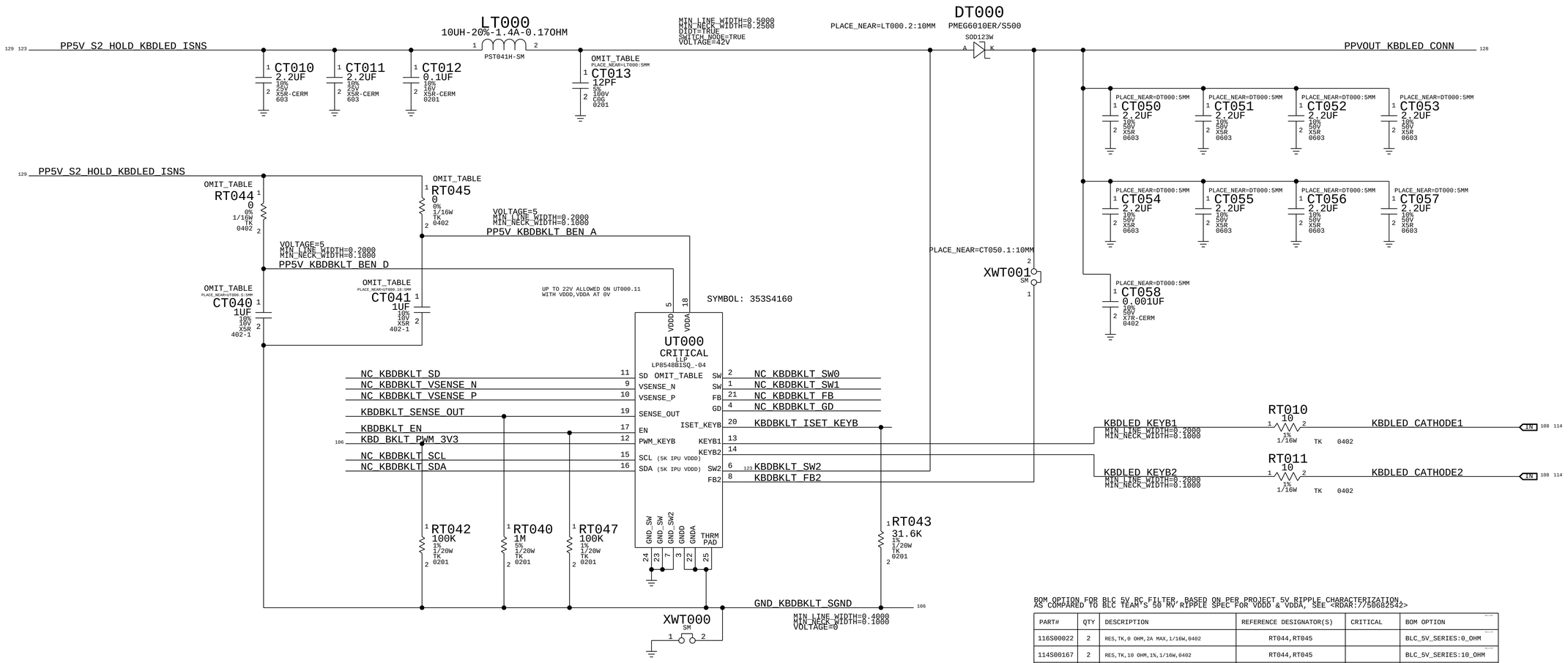
*** OK2INTEGRATE ***

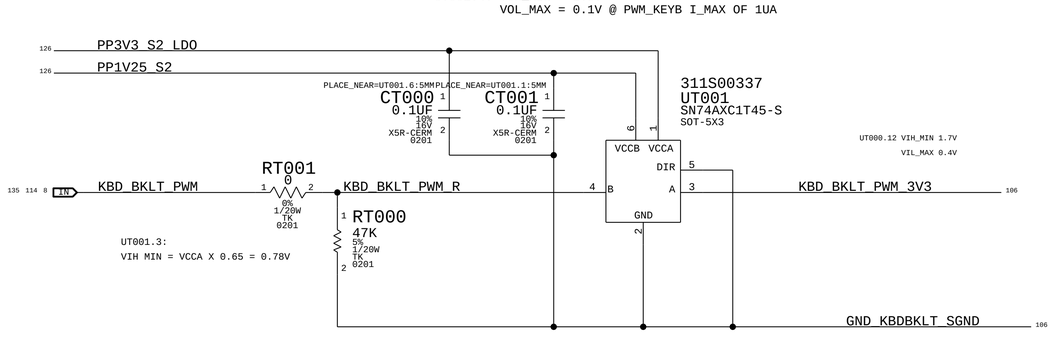
BEN IC: KEYBOARD LED DRIVER



BOM OPTION FOR BLC 5V RC FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION, AS COMPARED TO BLC TEAM'S 50 MV RIPPLE SPEC FOR VDDD & VDDA, SEE <RDAR:/750682542>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S00022	2	RES,TK,0 OHM,2A MAX,1/16W,0402	RT044,RT045		BLC_5V_SERIES:0_OHM
114S00167	2	RES,TK,10 OHM,1%,1/16W,0402	RT044,RT045		BLC_5V_SERIES:10_OHM
138S0614	2	CAP,CER,X5R,1UF,10%,10V,0402	CT040,CT041		BLC_5V_CAP:1_UF
138S00070	2	CAP,CER,X5R,4.7UF,20%,25V,0402	CT040,CT041		BLC_5V_CAP:4P7_UF

KEYBOARD BKLT PWM LEVEL-SHIFTER



BEN IC VERSION 4 VS 6 DEPENDS ON WHICH VERSION OF JERRY IC IS ON THE PANEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S01615	1	IC,LP8548B1-04,DC/DC CVTR,BST,AIDJ,QFN-24	UT000		BLC_BEN_IC:V4
353S01685	1	IC,LP8548B1-06,DC/DC CVTR,BST,QFN24	UT000		BLC_BEN_IC:V6

ALTERNATE PART FOR BEN IC VERSION 4

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S4160	353S01615	BLC_BEN_IC:V4	ALL	RECOMMENDED BY LOUISA

KEYBOARD SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5%,100V,0201	CT013		BLC_KBD_SW_NODE_DESENSE

BOM_COST_GROUP=DISPLAY

PAGE TITLE: BEN: KEYBD BKLT

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*** OK2PLACE ***

TO/FROM TRACKPAD

RT110 33 1% 1/20W TK 0201 — CKPLUS_WAIVE=I2C_PULLUP
IN I2C_KBD_SCL — IOXP_I2C_SCL
PLACE_NEAR=JT400.8:10MM
DZT110 5.5V-0.28PF 0201-THICKSTNCL

RT111 33 1% 1/20W TK 0201 — CKPLUS_WAIVE=I2C_PULLUP
BI I2C_KBD_SDA — IOXP_I2C_SDA
PLACE_NEAR=JT400.9:10MM
DZT111 5.5V-0.28PF 0201-THICKSTNCL

RT112 33 1% 1/20W TK 0201
OUT KBD_INT_L — IOXP2_INT_L
PLACE_NEAR=JT400.9:10MM
DZT112 5.5V-0.28PF 0201-THICKSTNCL

KEYBAORD IOX1

TIE TO SAME VOLTAGE AS TPAD CONTROLLER, EITHER 1V8 OR 3V3

PP3V3_S2_HOLD_KBD_ISNS
CT110 1.0UF 20% 6.3V X5R 0201-1 138S0692
CT112 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

ALL PLATFORMS CONNECT TO 1V8

PP1V825_S2_HOLD_KBD_ISNS
CT113 0.1UF 10% 6.3V CERM-X5R 0201 132S0444
CT114 10UF 20% 10V X5R-CERM 0402-7

IOX1 DOESN'T SEND THE INTERRUPT INSTEAD, IOX2 SENDS INT WHEN A KEY IS PRESSED

UT101 TCAL6416 WQFN-COMBO

IOXP1_INT_L	22	INT*
	18	ADDR
	19	SCL
	20	SDA
IOXP1_RESET_L	24	RESET*
	23	VCCI
	21	VCCP
	9	GND
	25	EPAD

CT111 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

311S0665
WRITE: 0X40
READ: 0X41
OMIT_TABLE

P00	1	KBD_DRIVE_Y0
P01	2	KBD_DRIVE_Y1
P02	3	KBD_DRIVE_Y2
P03	4	KBD_DRIVE_Y3
P04	5	KBD_DRIVE_Y4
P05	6	KBD_DRIVE_Y5
P06	7	KBD_DRIVE_Y6
P07	8	KBD_DRIVE_Y7
P10	10	KBD_DRIVE_Y8
P11	11	KBD_DRIVE_Y9
P12	12	KBD_DRIVE_Y10
P13	13	KBD_DRIVE_Y11
P14	14	NC
P15	15	KBD_ID_DETECT2
P16	16	KBD_LAYOUT_DETECT
P17	17	CAPSLOCK_LED_EN

ADD 4X NEW IO,Y8,Y9,Y10,Y11 FOR ALL 34-PIN KBD
CONNECT THE NEW IO FROM KBD ZIF CONN TO NEARBY ESD DIODES

KEYBAORD IOX2

TIE TO SAME VOLTAGE AS TPAD CONTROLLER, EITHER 1V8 OR 3V3

PP3V3_S2_HOLD_KBD_ISNS
RT121 100K 5% 1/20W TK 0201
CT120 1.0UF 20% 6.3V X5R 0201-1 138S0692
CT121 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

ALL PLATFORMS CONNECT TO 1V8

PP1V825_S2_HOLD_KBD_ISNS
CT122 0.1UF 10% 10V X5R-CERM 0201

UT102 TCAL6416 WQFN-COMBO

	22	INT*
IOXP2_ADDR	18	ADDR
	19	SCL
	20	SDA
IOXP2_RESET_L	24	RESET*
	23	VCCI
	21	VCCP
	9	GND
	25	EPAD

CT123 0.1UF 10% 6.3V CERM-X5R 0201 132S0444

311S0665
WRITE: 0X42
READ: 0X43
OMIT_TABLE

P00	1	KBD_SENSE_X0
P01	2	KBD_SENSE_X1
P02	3	KBD_SENSE_X2
P03	4	KBD_SENSE_X3
P04	5	KBD_SENSE_X4
P05	6	KBD_SENSE_X5
P06	7	KBD_SENSE_X6
P07	8	KBD_SENSE_X7
P10	10	KBD_SENSE_X8
P11	11	KBD_SENSE_X9
P12	12	KBD_SENSE_X10
P13	13	KBD_SENSE_X11
P14	14	KBD_SENSE_X12
P15	15	KBD_CONTROL_L
P16	16	KBD_LEFT_OPTION_L
P17	17	KBD_RIGHT_SHIFT_L

PP1V825_S2_HOLD_KBD_ISNS
RT130 10K 5% 1/20W TK 0201 — KBD_SENSE_X0
RT131 10K 5% 1/20W TK 0201 — KBD_SENSE_X1
RT132 10K 5% 1/20W TK 0201 — KBD_SENSE_X2
RT133 10K 5% 1/20W TK 0201 — KBD_SENSE_X3
RT134 10K 5% 1/20W TK 0201 — KBD_SENSE_X4
RT135 10K 5% 1/20W TK 0201 — KBD_SENSE_X5
RT136 10K 5% 1/20W TK 0201 — KBD_SENSE_X6
RT137 10K 5% 1/20W TK 0201 — KBD_SENSE_X7
RT138 10K 5% 1/20W TK 0201 — KBD_SENSE_X8
RT139 10K 5% 1/20W TK 0201 — KBD_SENSE_X9
RT140 10K 5% 1/20W TK 0201 — KBD_SENSE_X10
RT141 10K 5% 1/20W TK 0201 — KBD_SENSE_X11
RT142 10K 5% 1/20W TK 0201 — KBD_SENSE_X12
RT143 1K 1% 1/20W TK 0201 — IOXP2_ADDR

PP3V3_S2_HOLD_KBD_ISNS
RT120 10K 5% 1/20W TK 0201 — IOXP2_RESET_L
RT122 10K 5% 1/20W TK 0201 — IOXP1_RESET_L
RT123 1.3K 1% 1/20W TK 0201 — I2C_KBD_SCL
RT124 1.3K 1% 1/20W TK 0201 — I2C_KBD_SDA
RT125 100K 1% 1/20W TK 0201 — IOXP1_INT_L

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
311S0665	2	IC,16-BIT,I2C/SMBUS,I/O EXPANDER,HWQFN24	UT101,UT102	CRITICAL	

3V3 KBD CONN SERIES R

KBD DRI REQUEST, TO MEASURE CAPSLOCK LED CURRENT

PP3V3_AON — RT103 0 0% 1/20W TK 0201 — PP3V3_AON_KBD_CONN
TO KBD CONN AND ESD
MIN_NECK_WIDTH=0.1200
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.3

ID_DETECT SERIES R

KBD_LAYOUT_DETECT — RT117 1K 5% 1/20W TK 0201-1 — KBD_ID1
KBD_ID 1 PIN ON KBD CONNECTOR
ANSI: NO CONNECT
ISO: TIED HIGH TO PP1V8
JIS: TIED LOW TO GND

KBD_ID_DETECT2 — RT119 1K 5% 1/20W TK 0201-1 — KBD_ID2
KBD_ID 2 PIN ON KBD CONNECTOR
TIED LOW TO GND FOR 34-PIN KBD

3.3V RSLOC ISOLATION KEYS/ASIC RESET

PP3V3_AON
CT150 1.0UF 20% 6.3V X5R 0201-1 138S0692 — PLACE_NEAR=UT103.10:5MM
CT151 0.1UF 10% 6.3V CERM-X5R 0201 132S0444 — PLACE_NEAR=UT103.10:2MM

PP1V825_S2_HOLD_KBD_ISNS
117S00073 RT190 0 0% 1/20W TK 0201

UT103 SLG4AP45306 QFN-THICKSTNCL 343S00532
(2.97 < VDD < 3.63)
IN_X: VIH_MIN 2.0V VIL_MAX 0.8V 100K IPD
OUT_X: VOH_MIN 2.4V VOL_MAX 0.4V 12.5K IPU OE

OUT123_EN — OE
KBD_RIGHT_SHIFT_KEY — IN_1 — OUT_1 — KBD_RIGHT_SHIFT_L
KBD_LEFT_OPTION_KEY — IN_2 — OUT_2 — KBD_LEFT_OPTION_L
KBD_CONTROL_KEY — IN_3 — OUT_3 — KBD_CONTROL_L
OUT_ALL* — RT152 33 1% 1/20W TK 0201 — RSLOC_RST_L — PMU_RSLOC_RST_L
GND EPAD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S00879	353S00754		UT108	RDAR://32477358

USE SAME POWER RAIL AS TPAD 3V3 LDO INPUT

PP3V8_AON
CT180 1.0UF 20% 6.3V X5R 0201-1 138S0692
LP5907SNX-1.825 X2SON-COMBO-THICKSTNCL UT108
VIN 4 — VOUT 1 — PP1V825_S2_HOLD_KBDLDO
EN 3 — IPD_PWR_EN
GND EPAD 2 5
CT181 1.0UF 20% 6.3V X5R 0201-1 138S0692

THE LDO OUTPUT SUPPLY POWER OF KBD IO EXPANDER IO PIN.
EVENTUALLY SHOUULD BE CONNECTED TO PP1V8_S2_KBD

CAPSLOCK LED DRIVER

CONSTANT CURRENT LED DRIVER

NOTE: THIS CAN BE THE SAME RAIL AS THE CAPSLOCK LED (3V3_AON) OR A RAIL THAT COMES UP AFTER (3V3_S2)

PP3V3_S2_HOLD_KBD_ISNS
CT105 1.0UF 20% 6.3V X5R 0201-1 138S0692
UT105 FAN5622 SSOT23
VIN 3
CAPSLOCK_LED_EN — RT161 1K 5% 1/20W TK 0201-1 — CTRL 1
VIH_MIN 1.2V VIL_MAX 0.4V
LED_CTRL
LED_ISET — RT162 200K 5% 1/20W TK 0201 — ISET 5
<R_SET> RT160 19.1K 1% 1/20W TK 0201
GND 2
LED1 6 — R_SET 19.1K 15 MA SINK — RT118 1 1% 1/20W TK 0201 — KBD_CAP_CATHODE
LED2 4

BOM_COST_GROUP=KEYBOARD

PAGE TITLE: KEYBOARD IOX, SUPPORT

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DRAWING NUMBER: 051-07754
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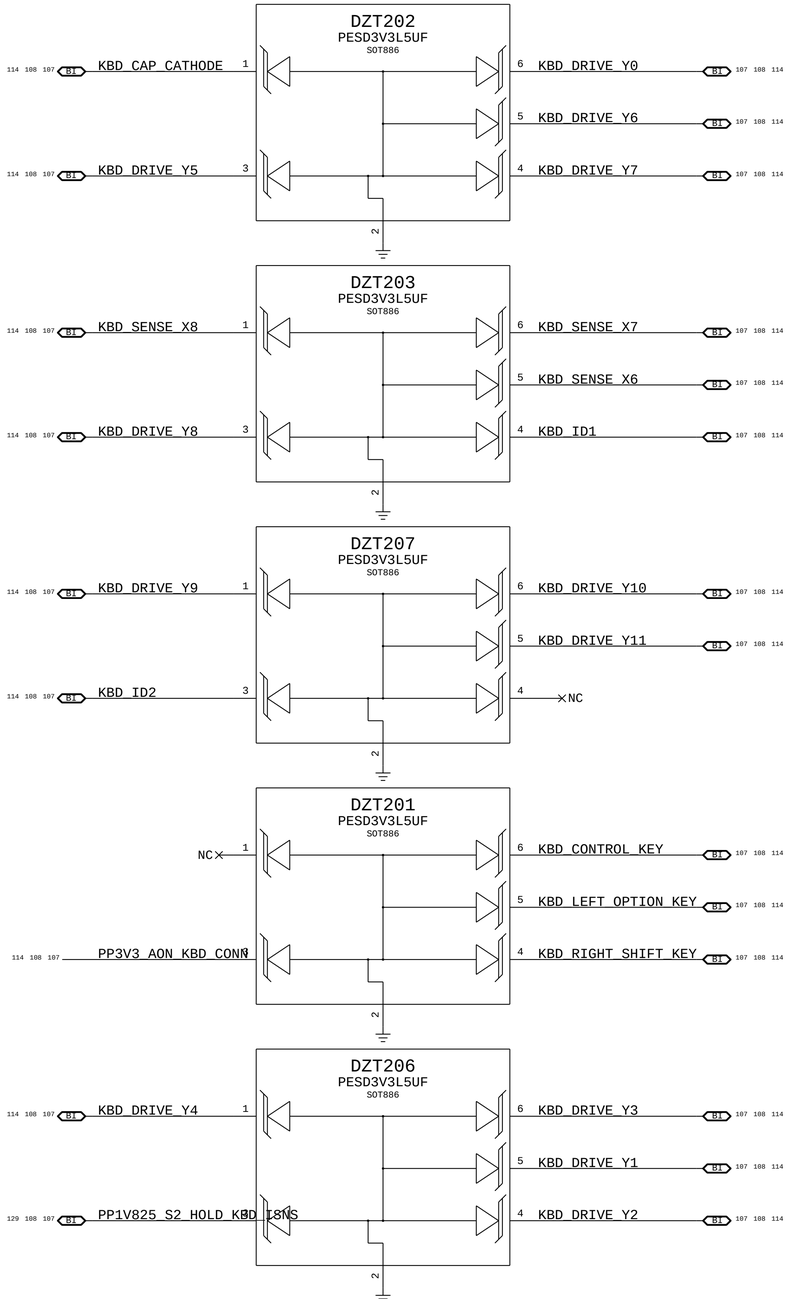
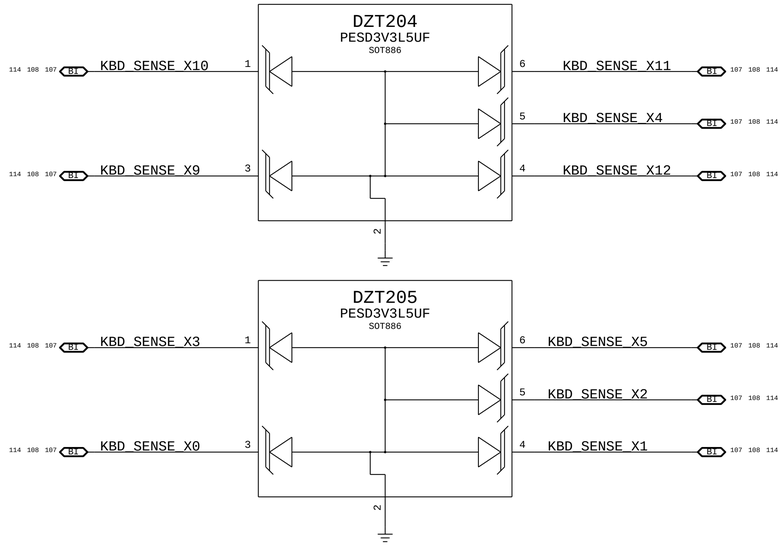
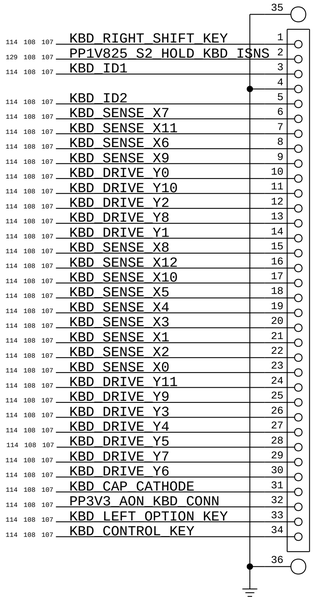
KEYBOARD ESD





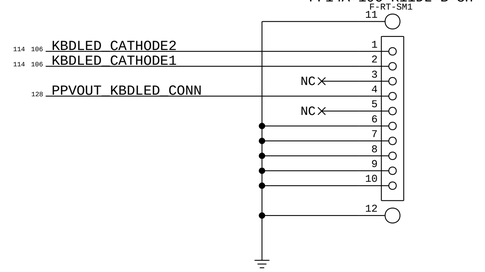
MEMBRANE POR 34 PIN ZIF CONNECTOR

518S00231
CRITICAL
JT200
FF14A-34C-R11DL-B-3H
F-RT-SM



KBD BKLT CONNECTOR

CRITICAL
518S00116
JT220
FF14A-10C-R11DL-B-3H
F-RT-SM1



BOM_COST_GROUP=KEYBOARD

PAGE TITLE
KEYBOARD SIGNAL CONNECTOR, ESD

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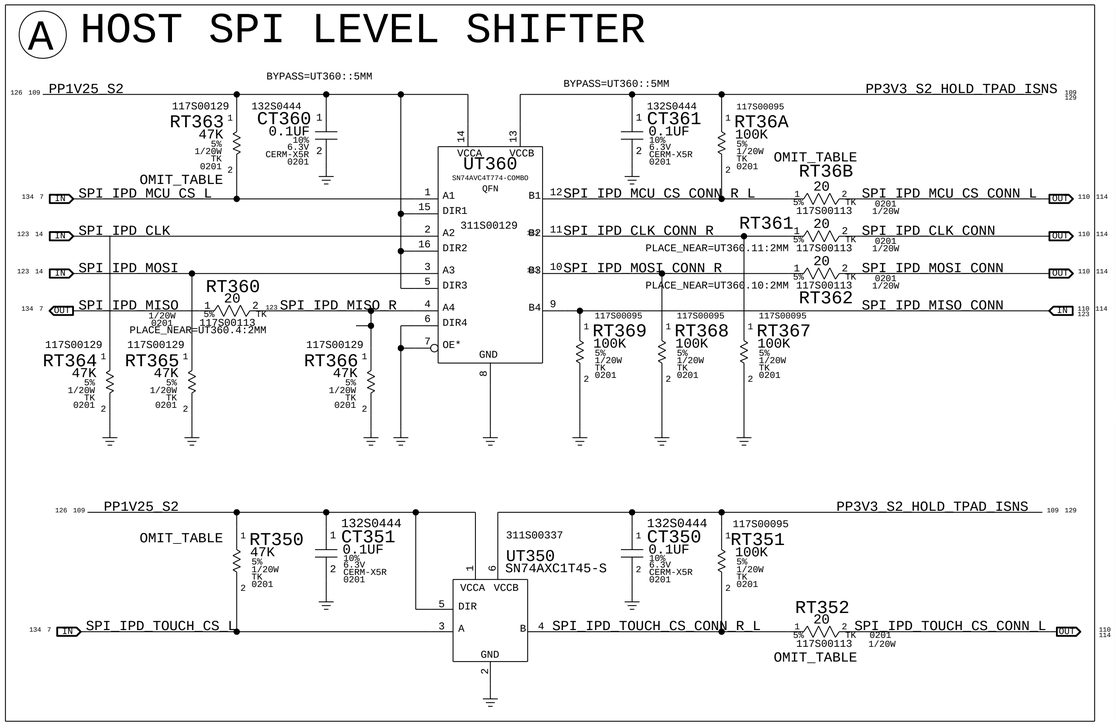
A HOST SPI LEVEL SHIFTER
BYPASS=UT360::5MM
PP1V25_S2
PP3V3_S2_HOLD_TPAD_ISNS
OMIT_TABLE
SPI_IPD_MCU_CS_L
SPI_IPD_CLK
SPI_IPD_MOSI
SPI_IPD_MISO
SPI_IPD_MISO_R
SPI_IPD_MCU_CS_CONN_R_L
SPI_IPD_CLK_CONN_R
SPI_IPD_MOSI_CONN_R
SPI_IPD_MISO_CONN
SPI_IPD_MCU_CS_CONN_L
SPI_IPD_CLK_CONN
SPI_IPD_MOSI_CONN
PLACE_NEAR=UT360.4:2MM
PLACE_NEAR=UT360.11:2MM
PLACE_NEAR=UT360.10:2MM
UT360
SN74AVC4T774-COMBO
QFN
RT360
RT361
RT362
RT363
RT364
RT365
RT366
RT367
RT368
RT369
RT36A
RT36B
CT360
CT361
311S00129
117S00113
117S00095
117S00129
132S0444
OMIT_TABLE
BYPASS=UT360::5MM
PP3V3_S2_HOLD_TPAD_ISNS
PP1V25_S2
SPI_IPD_TOUCH_CS_L
SPI_IPD_TOUCH_CS_CONN_R_L
SPI_IPD_TOUCH_CS_CONN_L
UT350
SN74AXC1T45-S
311S00337
RT350
RT351
RT352
CT350
CT351
B MCU INT L LS
BYPASS=UT340::3MM
IPD_MCU_INT_CONN_L
IPD_MCU_INT_L
PACK_OPTION=IPD_MCU_INT_WAKE_LS:SOT
PACK_IGNORE=TRUE
PACK_OPTION=IPD_MCU_INT_WAKE_LS:X2SON_THK
UT340
SN74AUP1G07
X2SON-THICKSTNCL
SOT1202
311S00332
311S00321
RT340
RT341
CT340
C WAKE L LS
RDAR://91304223
PACK_OPTION=IPD_WAKE_PU_EN
PP1V8_AON
BYPASS=UT3A0::3MM
IPD_WAKE_CONN_L
IPD_WAKE_L
UT3A0
RT3A0
RT3A1
CT3A0
D TOUCH INT L LS
IPD_TOUCH_INT_CONN_L
IPD_TOUCH_INT_L
BYPASS=UT370::3MM
UT370
SN74AUP1G17
SON
311S00246
RT370
RT371
CT370
E TOUCH CLK
PMU_CLK32K_IPD
PACK_OPTION=IPD_TOUCH_CLK_SRC:MLB
IPD_TOUCH_CLK_CONN
MAKE_BASE=TRUE
PACK_OPTION=IPD_TOUCH_CLK_SRC:TPAD
RT390
F MTP FUNC1 LS
PACK_OPTION=IPD_PACK_MTP_FUNC1_FLEX:PULLUP
PACK_IGNORE=TRUE
PACK_OPTION=IPD_PACK_MTP_FUNC1_FLEX:PULLDOWN
PP3V3_S2_HOLD_IPD_FUNC1
VOLTAGE=3.3V
IPD_MTP_FUNC_1
IPD_MTP_FUNC_1_CONN
PACK_OPTION=IPD_PACK_MTP_FUNC1_CIRCUIT
NOSTUFF
UT330
LSF0101DRY
311S00244
RT330
RT331
CT330
CT331
G RESET LEVEL SHIFTER
PP1V8_AON
IPD_MCU_RESET_L
IPD_TOUCH_RESET_L
IPD_MCU_RESET_CONN_L
IPD_TOUCH_RESET_CONN_L
MAKE_BASE=TRUE
PACK_OPTION=IPD_RESETS_LS:LVL_SHIFTER
PACK_OPTION=IPD_RESETS_LS:PASS_THRU
UT380
SN74AUP2G07
311S00285
RT380
RT382
RT383
CT380
I DEV SWD LEVEL SHIFTER
DEV_IPD
PP1V25_S2
PP3V3_S2_HOLD_TPAD_ISNS
PP3V3_S2_HOLD_IPD_SWD_DATA
VOLTAGE=3.3V
SWD_IPD_DATA_R
SWD_IPD_DATA_CONN
SWD_IPD_CLK_R
SWD_IPD_CLK_CONN
UT3C0
LSF0101DRY
311S00244
UT3B0
SN74AXC1T45-S
311S00337
RT3C0
RT3C1
RT3C2
RT3B0
RT3B1
CT3C0
CT3C1
CT3B0
CT3B1
J SYS AWAKE LS
IPD_SYS_AWAKE
IPD_SYS_AWAKE_CONN
UT320
SN74AXC1T45-S
SOT-5X3
311S00337
RT320
CT320
CT321
BOM_COST_GROUP=TRACKPAD
PAGE TITLE
TRACKPAD SUPPORT
Apple Inc.
DRAWING NUMBER
051-07754
SIZE
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REVISION
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TRACKPAD FLEX CONNECTOR

MATES WITH 518S00080 ON TRACKPAD FLEX

516S00187
JT400
DF40C-50DS-0.4V-51
F-ST-SM

114 55	BI	I2C_SMC_IPD_SDA_CONN	2	1	IPD_MCU_INT_CONN_L	OUT	109 110 114
114 55	IN	I2C_SMC_IPD_SCL_CONN	4	3	SPI_IPD_MOSI_CONN	IN	109 114
147 114 107	IN	I2C_KBD_SCL	6	5	SPI_IPD_MCU_CS_CONN_L	IN	109 114
147 114 107	BI	I2C_KBD_SDA	8	7	SPI_IPD_MISO_CONN	OUT	109 114 123
114 107	IN	KBD_INT_L	10	9	IPD_SYS_AWAKE_CONN	IN	109 114
114 109	IN	IPD_TOUCH_CLK_CONN	12	11	SPI_IPD_CLK_CONN	IN	109 114
114 109	IN	SPI_IPD_TOUCH_CS_CONN_L	14	13			
			16	15	IPD_MCU_RESET_CONN_L	IN	109 114
109	OUT	IPD_TOUCH_INT_CONN_L	18	17	PP5V_S2_HOLD_IPD_CONN		114
114 99 46	IN	IPD_LID_OPEN_1V8	20	19	IPD_TOUCH_RESET_CONN_L	IN	109 114
114 109	OUT	IPD_WAKE_CONN_L	22	21	PP3V3_S2_HOLD_TPAD_ISNS		110 129
129 110		PP3V3_S2_HOLD_TPAD_ISNS	24	23			
			26	25	SWD_IPD_DATA_CONN		109 114
			28	27	SWD_IPD_CLK_CONN		109 114
			30	29	IPD_MTP_FUNC_1_CONN		109 114
			32	31			
			34	33			
			36	35			
			38	37			
			40	39			
125		PPBUS_AON	42	41			
			44	43			
			46	45			
			48	47			
			50	49			

ACT_GND 114

XWT401
SHORT-1.0MM-SM
998-22786

114 110 109 IPD_MCU_INT_CONN_L

X3DFN2-THICKSTNCL
ESD8011
DZT400
377S00031

155S0317
LT400
FERR-120-OHM-1.5A
0402A

PP5V_S2_HOLD_TPAD_ISNS 129

132S0183
CT400
0.1UF
10%
25V
X5R
402

AND GATE FOR IPD_PWR_EN

<RDAR://73272102> AND GATE FOR IPD_PWR_EN AND 5VS2_EN

126 PP1V8_AON

PLACE_NEAR=UT480.6:5MM
CT481
0.1UF
10%
6.3V
CERM-X5R
0201
132S0444

311S00306
UT480
SN74AUP1G08
USON

131 113 82 49 IN P5VS2HOLD_PWR_EN (1.8V)

107 46 IN IPD_PWR_EN (1.8V)

VIH(MIN)=1.17V

NOSTUFF
RT481
0
5%
1/20W
SM
0201

117S00073

IPD_PWR_EN_GATE 110

3V3 TRACKPAD LDO

125 PP3V8_AON

CT410
1.0UF
20%
6.3V
X5R
0201-1
138S0692

RT410
0
5%
1/16W
SM
0402
116S00022

110 IPD_PWR_EN_GATE

IPD_PWR_EN_GATE_R

RT411
100K
1%
1/16W
TK
0402-1
114S00175

UT410
TLV70733PDQN
DQN-COMBO-THICKSTNCL
353S3332
CRITICAL
ALLOW_APPLE_PREFIX=U
IN OUT EN GND THRM PAD

PP3V3_S2_HOLD_IPD 128

CT411
1.0UF
20%
6.3V
X5R
0201-1
138S0692

BOM_COST_GROUP=TRACKPAD

PAGE TITLE: TRACKPAD CONNECTOR

Apple Inc.

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ISOLATE FROM OTHER COMPONENTS / NETS AS MUCH AS POSSIBLE

117S00073
RT504
0
0%
1/20W
TK
0201
PMU_ONOFF_L_CONN
PMU_ONOFF_L
CT504
100PF
5%
25V
C0G
0201

117S00073
RT570
0
0%
1/20W
TK
0201
SPI_TOUCHID_CLK_1V8_CONN
SPI_TOUCHID_CLK_1V8
CT572
56PF
5%
25V
NP0-C0G
0201

117S00073
RT580
0
0%
1/20W
TK
0201
SPI_TOUCHID_MOSI_1V8_CONN
SPI_TOUCHID_MOSI_1V8
CT582
56PF
5%
25V
NP0-C0G
0201

117S00073
RT540
0
0%
1/20W
TK
0201
SPI_TOUCHID_MISO_1V8_CONN
SPI_TOUCHID_MISO_1V8
CT541
56PF
5%
25V
NP0-C0G
0201

117S00073
RT503
0
0%
1/20W
TK
0201
TOUCHID_BOOST_EN_CONN
TOUCHID_BOOST_EN
CT503
100PF
5%
25V
C0G
0201

516S00203
JT500
505066-1222
F-ST-SM1
PMU_ONOFF_L_CONN
SPI_TOUCHID_MOSI_1V8_CONN
SPI_TOUCHID_CLK_1V8_CONN
PP1V8_TOUCHID_FILT_CONN
PP3V0_TOUCHID_FILT_CONN
TOUCHID_BOOST_EN_CONN
TOUCHID_INT_1V8_CONN
SPI_TOUCHID_MISO_1V8_CONN
PP16V0_TOUCHID_FILT_CONN
PP3V0_TOUCHID_FILT_CONN

PP1V25_S2
CT520
0.1UF
10%
10V
X5R-CERM
0201
311S00245
UT520
74AVC2T45
VSSOP
VCCA
VCCB
DIR
GND
CT521
0.1UF
10%
10V
X5R-CERM
0201
PP1V8_TOUCHID
SPI_TOUCHID_MOSI
SPI_TOUCHID_CLK
SPI_TOUCHID_MOSI_1V8_R
SPI_TOUCHID_CLK_1V8_R
RT517
47K
1%
1/20W
TK
0201
NOSTUFF
RT518
47K
1%
1/20W
TK
0201
NOSTUFF
RT515
33
5%
1/20W
TK
0201
PLACE_NEAR=UT520:5MM
SPI_TOUCHID_MOSI_1V8
RT516
33
5%
1/20W
TK
0201
PLACE_NEAR=UT520:5MM
SPI_TOUCHID_CLK_1V8

PP1V25_S2
CT540
0.1UF
10%
10V
X5R-CERM
0201
311S00246
UT540
SN74AUP1G17
SON
SPI_TOUCHID_MISO_1V8
SPI_TOUCHID_MISO
RT541
100K
5%
1/20W
TK
0201
NC

BOM_COST_GROUP=TOUCHID

SYNC_MASTER=PATRICK_X2482_MLB	SYNC_DATE=02/04/2022
PAGE TITLE	TOUCHID CONN
Apple Inc.	DRAWING NUMBER 051-07754 SIZE D
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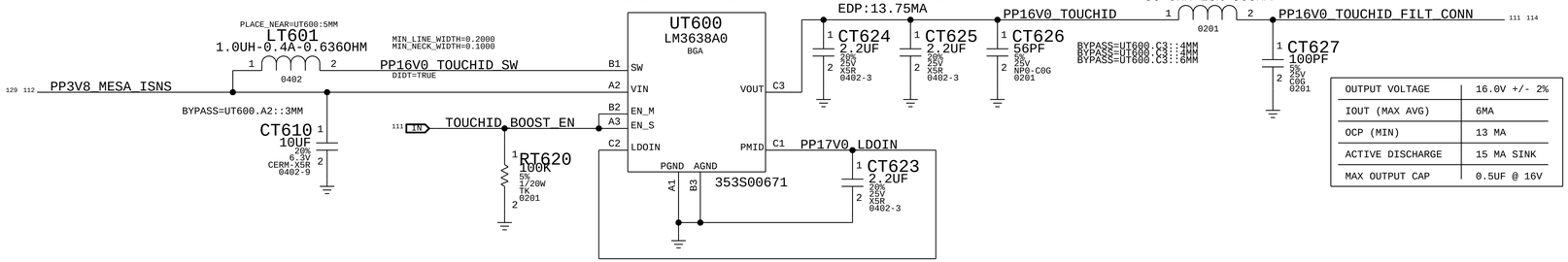
TOUCHID POWER SEQUENCING REQUIREMENTS
POWER ON: 1V8 -> 3V3 -> 16V0

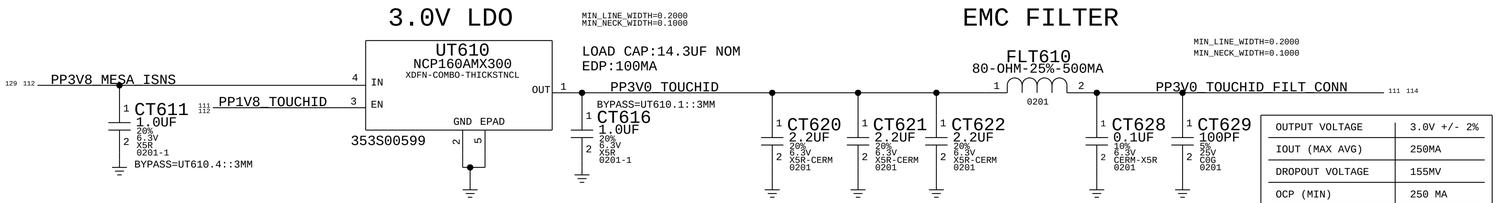
16V BOOST



EMC FILTER

OUTPUT VOLTAGE	16.0V +/- 2%
IOUT (MAX AVG)	6MA
OCP (MIN)	13 MA
ACTIVE DISCHARGE	15 MA SINK
MAX OUTPUT CAP	0.5UF @ 16V

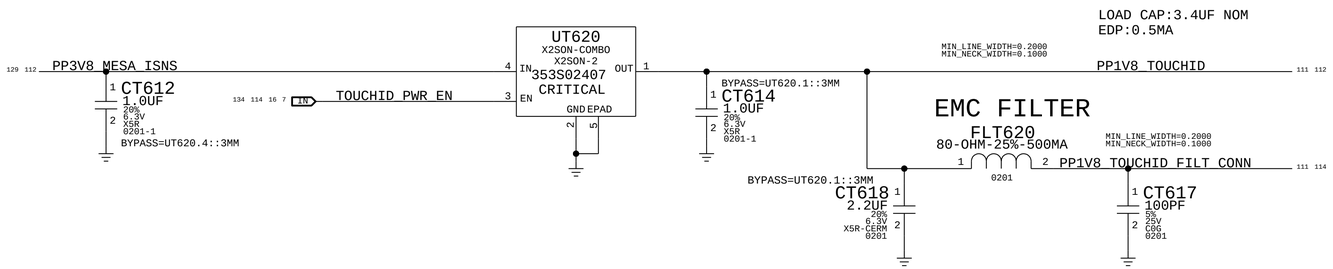
3.0V LDO



EMC FILTER

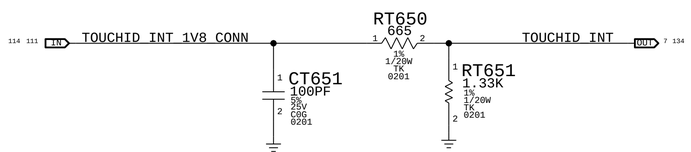
OUTPUT VOLTAGE	3.0V +/- 2%
IOUT (MAX AVG)	250MA
DROPOUT VOLTAGE	155MV
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP

1.825V LDO



EMC FILTER

OUTPUT VOLTAGE	1.825 V +/- 2%
IOUT (MAX AVG)	250 MA
DROPOUT VOLTAGE	75MV TYP @ 100MA
OCP (MIN)	250 MA
ACTIVE DISCHARGE	280 OHM TYP
MIN OUTPUT CAP	1.0 UF



BOM_COST_GROUP=TOUCHID

PAGE TITLE: TOUCHID SUPPORT

Apple Inc.

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DFU/DEBUG

133 7	SMC_FIXTURE_MODE_L	TOP	TPU6R0 TP-P4
71 66	USBC0_USB_TOP_P	TOP	TPU6R1 TP-P4
71 66	USBC0_USB_TOP_N	TOP	TPU6R2 TP-P4
130 77	USB2_ATC0_LS_N	TOP	TPU6R3 TP-P4
130 77	USB2_ATC0_LS_P	TOP	TPU6R4 TP-P4
71 69 67	ATCRTMR0_FORCE_DFU	TRUE	
73 70	SOC_DOCK_CONNECT_DBG_UPC	TRUE	
132 119 70 6	SOC_DFU_STATUS	TRUE	
132 130 6	SOC_DOCK_CONNECT	TRUE	
132 116 70 48 6	SOC_FORCE_DFU	TRUE	
116	PP1V25_S2_DFU_BTN_R	TRUE	
74 71 69	UPC0_ATCRTMR01_PWR_EN	TRUE	
74 72 69	UPC1_ATCRTMR01_PWR_EN	TRUE	
74 71 69	ATCRTMR0_RESET_L	TOP	TPU6S1 TP-P4
133 54 7	I2C_SMC_UPC_SCL	TRUE	
133 54 7	I2C_SMC_UPC_SDA	TRUE	
70 14	SWD_SOC_SWCLK	TRUE	
70 14	SWD_SOC_SWDIO	TRUE	
134 70 7	UART_DEBUGPRT_D2R	TRUE	
134 70 7	UART_DEBUGPRT_R2D	TRUE	
69 48 6	PMU_ACTIVE_READY	TRUE	
116 111 47 46	PMU_ONOFF_L	TRUE	
116 107 48 47 46	PMU_RSLOC_RST_L	TRUE	
91 47 46 45	PMU_SYS_ALIVE	TRUE	
48 6	SOC_SOCHOT_L	TRUE	
116 48 6	PMU_RESET_L	TRUE	
116 46 45	MPMU_SHDN	TRUE	
34 30 29 28	P3V8AON_PWR_EN	TRUE	
131 110 82 49	P5VS2HOLD_PWR_EN	TRUE	
135 52 8	I2C_UPC_SCL	TRUE	
135 52 8	I2C_UPC_SDA	TRUE	
130	USB_ATC0_DBG_LS_P	TRUE	
130	USB_ATC0_DBG_LS_N	TRUE	
132 6	SOC_KIS_DFU_SELECT	TRUE	
130 74 67	ATCRTMR0_RESET_1V2_L	TRUE	
73 70	SOC_DOCK_CONNECT_DUAL_KIS	TRUE	
71 69	UPC0_SER_DBG	TRUE	
72 69	UPC1_SER_DBG	TRUE	
77	I2C_UPC0_RTMR0_EUSB0_SCL_1V2	TRUE	
77	I2C_UPC0_RTMR0_EUSB0_SDA_1V2	TRUE	
77	I2C_UPC1_RTMR1_EUSB1_SCL_1V2	TRUE	
77	I2C_UPC1_RTMR1_EUSB1_SDA_1V2	TRUE	

BATTERY

125	PPVBAT_AON	TOP	TPU600 TP-P4
		TOP	TPU601 TP-P4
		TOP	TPU602 TP-P4
		TOP	TPU603 TP-P4
		TOP	TPU604 TP-P4
		TOP	TPU605 TP-P4
		TOP	TPU606 TP-P4
		TOP	TPU607 TP-P4
		TOP	TPU608 TP-P4
		TOP	TPU609 TP-P4
		TOP	TPU610 TP-P4
		TOP	TPU611 TP-P4
		TOP	TPU612 TP-P4
		TOP	TPU613 TP-P4
		TOP	TPU614 TP-P4
		TOP	TPU615 TP-P4
		TOP	TPU616 TP-P4
54 28	SMBUS_BATT_SDA	TRUE	
54 28	SMBUS_BATT_SCL	TRUE	
28	SYS_DETECT_L	TRUE	
117 28	SYS_DETECT	TRUE	
	GND	TOP	TPU617 TP-P4

CHARGER

125	PPDCIN_USBC_AON	TOP	TPU618 TP-P4
		TOP	TPU619 TP-P4
		TOP	TPU620 TP-P4
		TOP	TPU621 TP-P4
		TOP	TPU622 TP-P4
		TOP	TPU623 TP-P4
		TOP	TPU624 TP-P4
		TOP	TPU625 TP-P4
		TOP	TPU626 TP-P4
		TOP	TPU627 TP-P4
		TOP	TPU628 TP-P4
123 29	PPDCIN_AON_CHGR_R	TRUE	
130 32 31	PPVBUS_USBC5	TOP	TPU630 TP-P4
		TOP	TPU631 TP-P4
		TOP	TPU632 TP-P4
		TOP	TPU633 TP-P4
		TOP	TPU634 TP-P4
		TOP	TPU635 TP-P4
		TOP	TPU636 TP-P4
		TOP	TPU637 TP-P4
		TOP	TPU638 TP-P4
		TOP	TPU639 TP-P4
	GND	TOP	TPU640 TP-P4
		TOP	TPU641 TP-P4
		TOP	TPU642 TP-P4
		TOP	TPU643 TP-P4
		TOP	TPU644 TP-P4
		TOP	TPU645 TP-P4
		TOP	TPU646 TP-P4
		TOP	TPU647 TP-P4
		TOP	TPU648 TP-P4
		TOP	TPU649 TP-P4
		TOP	TPU650 TP-P4
54 29	SMBUS_CHGR_1V8_SDA	TRUE	
54 29	SMBUS_CHGR_1V8_SCL	TRUE	
29	TP_CHGR_SMC_RST_L	TRUE	
29	TP_CHGR_EN_VR1	TRUE	
29	TP_CHGR_CBC_ON	TRUE	
47 29 28	CHGR_RST_IN	TRUE	
133 30 7	CHGR_INT_L	TRUE	
130 46	CHGR_AUX_OK	TRUE	

POWER RAILS

125	PPBUS_AON	TOP	TPU651 TP-P4
		TOP	TPU652 TP-P4
		TOP	TPU653 TP-P4
		TOP	TPU654 TP-P4
		TOP	TPU655 TP-P4
		TOP	TPU656 TP-P4
		TOP	TPU657 TP-P4
		TOP	TPU658 TP-P4
		TOP	TPU659 TP-P4
		TOP	TPU660 TP-P4
		TOP	TPU661 TP-P4
125	PP3V8_AON	TOP	TPU664 TP-P4
		TOP	TPU665 TP-P4
125	PP0V779_S1_SRAM	TRUE	
126	PP2V58_AWAKE_NAND_VCC	TRUE	
125	PPVDD_S1_DISP	TRUE	
125	PPVDD_S1_VDDQL	TRUE	
125	PP0V88_S1	TRUE	
126	PP1V12_S2SW_AMPH	TRUE	
126	PP0V72_S2_VDD_LOW	TRUE	
127	PP1V8_AON_SPMU	TRUE	
127	PP1V2_AON_SPMU	TRUE	
127	PP0V8_S1_VDD_FIXED	TRUE	
127	PP3V3_S2SW_SNS	TRUE	
126	PP1V8_AWAKE_SPMU_GPIO	TRUE	
126	PP1V25_AWAKE_NAND_VCCQ	TRUE	
126	PP0V88_AWAKE_NAND_VDD	TRUE	
125	PPVDD_AWAKE_PCPU	TRUE	
125	PPVDD_AWAKE_GPU	TRUE	
126	PPVDD_S1_SOC	TRUE	
125	PP1V8_S2	TOP	TPU662 TP-P4
		TOP	TPU663 TP-P4
125	PPVDD_S2SW_VDD2H	TRUE	
125	PPVDD_AWAKE_CPU_SRAM	TRUE	
125	PPVDD_S1_DCS	TRUE	
125	PPVDD_AWAKE_ECPU	TRUE	
126	PP1V25_S2	TRUE	
126	PP1V8_AWAKE	TRUE	
126	PP1V25_AWAKE_IO	TRUE	
126	PP1V8_AON	TRUE	
126	PP3V3_S2_LDO	TRUE	
127	PP1V2_AWAKE_PLL	TRUE	
127	PP1V8_AON_MPMU	TRUE	
127	PP1V2_AON_MPMU	TRUE	
127	PP3V3_AON	TRUE	
127	PP0V855_S2SW_CIO	TRUE	
127	PP1V2_S2_CIO	TRUE	
128	PP1V2_USBC_VDDIO	TRUE	
128	PP0V855_USBC_CIO	TRUE	
128	PP0V805_USBC_FIXED	TRUE	
71 70 69	PP3V3_UPC0_LDO	TRUE	
125 123 29	PPVBAT_AON_CHGR_REG	TOP	TPU670 TP-P4
		TOP	TPU671 TP-P4
		TOP	TPU672 TP-P4
29	PPVBAT_AON_CHGR_R	TRUE	
128	PP5V_S2_HOLD	TOP	TPU676 TP-P4
		TOP	TPU677 TP-P4
128	PP1V8_S2SW	TRUE	
125	PP5V_AON	TRUE	
127	PP1V5_LDOINT_MPMU	TRUE	
127	PP1V5_LDOINT_SPMU	TRUE	
127	PP5V_MPMU_BSTLQ	TRUE	
127	PP5V_SPMU_BSTLQ	TRUE	
86 85 83	PP3V3_AWAKE_SW_SD	TRUE	
128	PP3V29_BCON_AWAKESW	TRUE	
128 123	PP5V_S2_UPC	TRUE	
128	PP1V29_AWAKESW_BLC	TRUE	
72 70 69	PP3V3_UPC1_LDO	TRUE	
33 32	PP3V3_UPC5_LDO	TRUE	
128	PP1V825_S2_HOLD_KBDLDO	TRUE	
129	PP3V8_AWAKESW_TCON_ISNS	TRUE	

FAN

65	FAN_0_PWM_5V	TRUE
65	FAN_0_TACH	TRUE
65	TP_FAN_0_OTP1	TRUE
65	TP_FAN_0_OTP2	TRUE
	GND	TOP TPU680 TP-P4
	GND	TOP TPU681 TP-P4
	GND	TOP TPU682 TP-P4
	GND	TOP TPU683 TP-P4

USBC

71 66	PPVBUS_USBC0	TOP	TPU690 TP-P4
		TOP	TPU691 TP-P4
		TOP	TPU692 TP-P4
		TOP	TPU693 TP-P4
	GND	TOP	TPU694 TP-P4
72 69 66	PPVBUS_USBC1	TOP	TPU695 TP-P4
		TOP	TPU696 TP-P4
		TOP	TPU697 TP-P4
		TOP	TPU698 TP-P4
	GND	TOP	TPU699 TP-P4
		TOP	TPU6A0 TP-P4
		TOP	TPU6A1 TP-P4
	GND	TOP	TPU6A2 TP-P4
		TOP	TPU6A3 TP-P4
		TOP	TPU6A4 TP-P4
		TOP	TPU6A5 TP-P4
71 66	USBC0_SBU1	TOP	TPU6T0 TP-P4
71 66	USBC0_SBU2	TOP	TPU6T1 TP-P4
70 66	USBC0_CC1_CONN	TOP	TPU6T2 TP-P4
70 66	USBC0_CC2_CONN	TOP	TPU6T3 TP-P4
32 31	USBC5_CC1	TOP	TPU6T4 TP-P4
66	TP_USBC0_PP20V	TOP	TPU6T5 TP-P4
70 66	USBC1_CC1_CONN	TOP	TPU6T6 TP-P4
70 66	USBC1_CC2_CONN	TOP	TPU6T7 TP-P4
72 66	USBC1_SBU1	TOP	TPU6T8 TP-P4
72 66	USBC1_SBU2	TOP	TPU6T9 TP-P4
66	TP_USBC1_PP20V	TOP	TPU6V0 TP-P4
69	PPHV_INT0_AONSW	TOP	TPU6V1 TP-P4
71	PP1V5_UPC0_LDO_CORE	TRUE	
69	PPHV_INT1_AONSW	TOP	TPU6V2 TP-P4
72	PP1V5_UPC1_LDO_CORE	TRUE	
130	PPHV_INT5_AONSW	TOP	TPU6V3 TP-P4
32	PP1V5_UPC5_LDO_CORE	TRUE	

SSD

VREF TP ON SSD PAGE

	GND	TOP	TPU6B0 TP-P4
89	TP_NAND0_S5E0_DROOP_L	TOP	TPU6B1 TP-P4
90	TP_NAND0_S5E1_DROOP_L	TOP	TPU6B2 TP-P4

DISPLAY

128	PP3V8_AWAKESW_TCON	TRUE
95 94	EDP_PANEL_1V8_EN	TRUE
137 94 16 10	LPDP_INT_HPD	TRUE
94	SPI_TCON_CLK_CONN	TRUE
135 94 8	SPI_TCON_CS_L	TRUE
94	SPI_TCON_MISO_CONN	TRUE
94	SPI_TCON_MOSI_CONN	TRUE
94	UART_TCON_D2R_1V8	TRUE
94 54	I2C_DISP_TEMP_1V8_SCL	TRUE
94 54	I2C_DISP_TEMP_1V8_SDA	TRUE
	GND	TOP TPU6E0 TP-P4

BCON

129 97	PP3V29_AWAKESW_BCON_ISNS	TRUE	
128 97 96	PPVOUT_LUXE	TOP	TPU6D0 TP-P4
		TOP	TPU6D1 TP-P4
		TOP	TPU6D2 TP-P4
		TOP	TPU6D3 TP-P4
		TOP	TPU6D4 TP-P4
		TOP	TPU6D5 TP-P4
97	BKLT_BOOST_THROTTLE_CONN_L	TRUE	
97 46	BL_PMIC_PWR_EN	TRUE	
137 130 10	DISP_BKLT_FSYNC	TRUE	
137 97 10	DISP_BKLT_LSYNC	TRUE	
97 53	I2C_BKLT_1V8_SCL	TRUE	
97 53	I2C_BKLT_1V8_SDA	TRUE	
97	SPI_DISP_BKLT_CLK_CONN	TRUE	
137 97 10	SPI_DISP_BKLT_CS_L	TRUE	
97	SPI_DISP_BKLT_MISO_CONN	TRUE	
97	SPI_DISP_BKLT_MOSI_CONN	TRUE	
	GND	TOP	TPU6D6 TP-P4
		TOP	TPU6D7 TP-P4
		TOP	TPU6D8 TP-P4
		TOP	TPU6D9 TP-P4
129	PP3V29_AWAKESW_BCON_ISNS	TRUE	
130 97	DISP_BKLT_FSYNC	TRUE	

MISC

55	I2C_SMC_SNS0_SCL_3V3	TRUE
55	I2C_SMC_SNS0_SDA_3V3	TRUE

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TOUCHID

112 111	IN	PP1V8_TOUCHID_FILT_CONN	TRUE
112 111	IN	PP3V0_TOUCHID_FILT_CONN	TRUE
	TOP 1 TP	TPU7F0 TP-P4	
	TOP 1 TP	TPU7F1 TP-P4	
	TOP 1 TP	TPU7F2 TP-P4	
112 111	IN	PP16V0_TOUCHID_FILT_CONN	TRUE
111	IN	SPI_TOUCHID_CLK_1V8_CONN	TRUE
111	IN	SPI_TOUCHID_MISO_1V8_CONN	TRUE
111	IN	SPI_TOUCHID_MOSI_1V8_CONN	TRUE
111	IN	TOUCHID_BOOST_EN_CONN	TRUE
112 111	IN	TOUCHID_INT_1V8_CONN	TRUE
	GND TOP 1 TP	TPU7F3 TP-P4	
134 112 16 7	IN	TOUCHID_PWR_EN	TRUE

DMIC

105	IN	PP1V8_DMIC	TRUE
105	IN	PDM_DMIC_CLK5_1V8	TRUE
105	IN	PDM_DMIC_CLK6_1V8	TRUE
105	IN	PDM_DMIC_DATA0_1V8	TRUE
105	IN	PDM_DMIC_DATA1_1V8	TRUE

SPEAKER AMP

104 102	IN	SPKRAMP_A_OUTP TOP 1 TP	TPU7G0 TP-P4
		TOP 1 TP	TPU7G1 TP-P4
		TOP 1 TP	TPU7G2 TP-P4
104 102	IN	SPKRAMP_A_OUTN TOP 1 TP	TPU7G3 TP-P4
		TOP 1 TP	TPU7G4 TP-P4
		TOP 1 TP	TPU7G5 TP-P4
104 102	IN	SPKRAMP_B_OUTP TOP 1 TP	TPU7G6 TP-P4
		TOP 1 TP	TPU7G7 TP-P4
		TOP 1 TP	TPU7G8 TP-P4
104 102	IN	SPKRAMP_B_OUTN TOP 1 TP	TPU7G9 TP-P4
		TOP 1 TP	TPU7H0 TP-P4
		TOP 1 TP	TPU7H1 TP-P4
104 102	IN	SPKRAMP_C_OUTP TOP 1 TP	TPU7H2 TP-P4
		TOP 1 TP	TPU7H3 TP-P4
		TOP 1 TP	TPU7H4 TP-P4
104 102	IN	SPKRAMP_C_OUTN TOP 1 TP	TPU7H5 TP-P4
		TOP 1 TP	TPU7H6 TP-P4
		TOP 1 TP	TPU7H7 TP-P4
134 104 7	IN	SPKR_ID0	TRUE
	GND TOP 1 TP	TPU7H8 TP-P4	
	GND TOP 1 TP	TPU7H9 TP-P4	
	GND TOP 1 TP	TPU7J0 TP-P4	
	GND TOP 1 TP	TPU7J1 TP-P4	
104 103	IN	SPKRAMP_D_OUTP TOP 1 TP	TPU7J2 TP-P4
		TOP 1 TP	TPU7J3 TP-P4
		TOP 1 TP	TPU7J4 TP-P4
104 103	IN	SPKRAMP_D_OUTN TOP 1 TP	TPU7J5 TP-P4
		TOP 1 TP	TPU7J6 TP-P4
		TOP 1 TP	TPU7J7 TP-P4
104 103	IN	SPKRAMP_E_OUTP TOP 1 TP	TPU7J8 TP-P4
		TOP 1 TP	TPU7J9 TP-P4
		TOP 1 TP	TPU7K0 TP-P4
104 103	IN	SPKRAMP_E_OUTN TOP 1 TP	TPU7K1 TP-P4
		TOP 1 TP	TPU7K2 TP-P4
		TOP 1 TP	TPU7K3 TP-P4
104 103	IN	SPKRAMP_F_OUTP TOP 1 TP	TPU7K4 TP-P4
		TOP 1 TP	TPU7K5 TP-P4
		TOP 1 TP	TPU7K6 TP-P4
104 103	IN	SPKRAMP_F_OUTN TOP 1 TP	TPU7K7 TP-P4
		TOP 1 TP	TPU7K8 TP-P4
		TOP 1 TP	TPU7K9 TP-P4
134 104 7	IN	SPKR_ID1	TRUE
	GND TOP 1 TP	TPU7L0 TP-P4	
	GND TOP 1 TP	TPU7L1 TP-P4	
	GND TOP 1 TP	TPU7L2 TP-P4	

TRACKPAD

110	IN	PP5V_S2_HOLD_IPD_CONN	
		TOP 1 TP	TPU7M0 TP-P4
		TOP 1 TP	TPU7M1 TP-P4
147 110 107	IN	I2C_KBD_SCL	TRUE
147 110 107	IN	I2C_KBD_SDA	TRUE
110 55	IN	I2C_SMC_IPD_SCL_CONN	TRUE
110 55	IN	I2C_SMC_IPD_SDA_CONN	TRUE
114 110 99 46	IN	IPD_LID_OPEN_1V8	TRUE
134 109 7	IN	IPD_MCU_INT_L	TRUE
110 109	IN	IPD_MCU_RESET_CONN_L	TRUE
110 109	IN	IPD_SYS_AWAKE_CONN	TRUE
110 109	IN	IPD_TOUCH_CLK_CONN	TRUE
134 109 7	IN	IPD_TOUCH_INT_L	TRUE
110 109	IN	IPD_TOUCH_RESET_CONN_L	TRUE
110 107	IN	KBD_INT_L	TRUE
110 109	IN	SPI_IPD_CLK_CONN	TRUE
123 110 109	IN	SPI_IPD_MISO_CONN	TRUE
110 109	IN	SPI_IPD_MOSI_CONN	TRUE
109 46	IN	IPD_WAKE_L	TRUE
	GND TOP 1 TP	TPU7M2 TP-P4	
	TOP 1 TP	TPU7M3 TP-P4	
110 109	IN	IPD_MCU_INT_CONN_L	TRUE
110 109	IN	SPI_IPD_TOUCH_CS_CONN_L	TRUE
110 109	IN	SPI_IPD_MCU_CS_CONN_L	TRUE
110 109	IN	IPD_MTP_FUNC_1_CONN	TRUE
114 110 99 46	IN	IPD_LID_OPEN_1V8	TRUE
110 109	IN	SWD_IPD_DATA_CONN	TRUE
110 109	IN	SWD_IPD_CLK_CONN	TRUE
110	IN	ACT_GND	TRUE
110 109	IN	IPD_WAKE_CONN_L	TRUE

WIFI/BT

129	IN	PP3V8_AON_WLBT_ISNS	TRUE
129	IN	PP1V8_S2_WLBT_ISNS	TRUE

KBD

128	IN	PP3V3_S2_HOLD_IPD	TRUE
108 107	IN	KBD_CAP_CATHODE	TRUE
108 107	IN	KBD_CONTROL_KEY	TRUE
108 107	IN	KBD_DRIVE_Y0	TRUE
108 107	IN	KBD_DRIVE_Y1	TRUE
108 107	IN	KBD_DRIVE_Y10	TRUE
108 107	IN	KBD_DRIVE_Y11	TRUE
108 107	IN	KBD_DRIVE_Y2	TRUE
108 107	IN	KBD_DRIVE_Y3	TRUE
108 107	IN	KBD_DRIVE_Y4	TRUE
108 107	IN	KBD_DRIVE_Y5	TRUE
108 107	IN	KBD_DRIVE_Y6	TRUE
108 107	IN	KBD_DRIVE_Y7	TRUE
108 107	IN	KBD_DRIVE_Y8	TRUE
108 107	IN	KBD_DRIVE_Y9	TRUE
108 107	IN	KBD_ID1	TRUE
108 107	IN	KBD_ID2	TRUE
108 107	IN	KBD_LEFT_OPTION_KEY	TRUE
108 107	IN	KBD_RIGHT_SHIFT_KEY	TRUE
108 107	IN	KBD_SENSE_X0	TRUE
108 107	IN	KBD_SENSE_X1	TRUE
108 107	IN	KBD_SENSE_X10	TRUE
108 107	IN	KBD_SENSE_X11	TRUE
108 107	IN	KBD_SENSE_X12	TRUE
108 107	IN	KBD_SENSE_X2	TRUE
108 107	IN	KBD_SENSE_X3	TRUE
108 107	IN	KBD_SENSE_X4	TRUE
108 107	IN	KBD_SENSE_X5	TRUE
108 107	IN	KBD_SENSE_X6	TRUE
108 107	IN	KBD_SENSE_X7	TRUE
108 107	IN	KBD_SENSE_X8	TRUE
108 107	IN	KBD_SENSE_X9	TRUE
108 107	IN	PP3V3_AON_KBD_CONN	TRUE
128	IN	PPVOUT_KBDLED_CONN	
		TOP 1 TP	TPU7R0 TP-P4
		TOP 1 TP	TPU7R1 TP-P4
108 106	IN	KBDLED_CATHODE1	TRUE
108 106	IN	KBDLED_CATHODE2	TRUE
	GND TOP 1 TP	TPU7R2 TP-P4	
	TOP 1 TP	TPU7R3 TP-P4	
135 106 8	IN	KBD_BKLT_PWM	TRUE

CAMERA

129	IN	PP5V_S2_HOLD_ALSCAM_ISNS	TRUE
133 92 7	IN	ALS_INT_L	TRUE
93 92	IN	FTCAM_ENABLE_1V8_OUT	TRUE
92 56	IN	I2C_ALS_1V8_SCL	TRUE
92 56	IN	I2C_ALS_1V8_SDA	TRUE
92 56	IN	I2C_CAM_1V8_SCL	TRUE
92 56	IN	I2C_CAM_1V8_SDA	TRUE
92	IN	LPDP_FTCAM_AUX	TRUE

HDMI

78	IN	PP5V0_HDMI_DDC_CONN	TRUE
78	IN	HDMI_CEC_CONN	TRUE
78	IN	HDMI_DDC_5V_CONN_SCL	TRUE
78	IN	HDMI_DDC_5V_CONN_SDA	TRUE
78	IN	HDMI_HPD_IN_CONN	TRUE
78	IN	HDMI_RSVD	TRUE
	GND TOP 1 TP	TPU7N0 TP-P4	

LAS

130 98	IN	AMR1_OR_ND_1V8	TRUE
99 98	IN	MGL_1V8	TRUE
98	IN	SPI_AOP_LAS_MISO_1V8_R	TRUE
100 98	IN	SPI_AOP_LAS_MOSI_1V8	TRUE
100 98	IN	SPI_AOP_LAS_SCLK_1V8	TRUE
100 98	IN	SPI_LAS_CS_1V8_L	TRUE
	GND TOP 1 TP	TPU7N1 TP-P4	
130 98	IN	AMR1_OR_ND_1V8	TRUE
133 99 7	IN	DMIC_DISABLE_L	TRUE
133 99 7	IN	DMIC_DISABLE_WARN_L	TRUE

AUDIO JACK

105	IN	AUD_CONN_HP_LEFT	TRUE
105	IN	AUD_CONN_HP_RIGHT	TRUE
105	IN	AUD_CONN_HP_SENSE_L	TRUE
105	IN	AUD_CONN_HP_SENSE_R	TRUE
105	IN	AUD_CONN_RING_SENSE	TRUE
105	IN	AUD_CONN_RING2	TRUE
105	IN	AUD_CONN_RING2_XW	TRUE
105	IN	AUD_CONN_SLEEVE	TRUE
105	IN	AUD_CONN_SLEEVE_XW	TRUE
105	IN	AUD_CONN_TIP_SENSE	TRUE
101	IN	CODEC_AGND	TRUE
	GND TOP 1 TP	TPU7E0 TP-P4	

SD

84 83	IN	PP1V8_GL_SDCONN	TRUE
84 83	IN	PP3V3_GL_SDCONN	TRUE
84	IN	SDCONN_CLK_CONN_FL	TRUE
84	IN	SDCONN_CMD_R_FL	TRUE
84	IN	SDCONN_D0_R_FL	TRUE
84	IN	SDCONN_D1_R_FL	TRUE
84	IN	SDCONN_D2_R_FL	TRUE
84	IN	SDCONN_D3_R_FL	TRUE
85 84	IN	SDCONN_DETECT	TRUE
84	IN	SDCONN_DETECT_R	TRUE
84 83	IN	SDCONN_SD0_UHS2_N	TRUE
84 83	IN	SDCONN_SD0_UHS2_P	TRUE
84 83	IN	SDCONN_SD1_UHS2_N	TRUE
84 83	IN	SDCONN_SD1_UHS2_P	TRUE
84	IN	SDCONN_WP_R	TRUE
	GND TOP 1 TP	TPU7P0 TP-P4	

THROTTLE/PMU

47 46 45	IN	PMU_CRASH_L	TRUE
114 45 39	IN	SPMU_SCRASH_L	TRUE
135 48 8	IN	BUCK0_THERMAL_THROTTLE_L	TRUE
135 48 8	IN	BUCK1_THERMAL_THROTTLE_L	TRUE
135 48	IN	SPMU_VDDMAIN_UVWARN_L	TRUE
135 48	IN	MPMU_VDDHI_UVWARN_L	TRUE
135 48 36 8	IN	MPMU_VDDMAIN_UVWARN_L	TRUE
137 16	IN	BKLT_BOOST_THROTTLE_L	TRUE
114 45 39	IN	SPMU_SCRASH_L	TRUE
44 6	IN	PMU_CLK32K_SOC	TRUE
130 88 87	IN	PMU_CLK32K_WLBT	TRUE
47 46	IN	UPC_PMU_RESET_1V2	TRUE
130 116	IN	UPC_PMU_RESET_1V2_ACE2	TRUE
48 6	IN	SOC_WDOG	TRUE
135 48 8	IN	DBL_CLICK_DET	TRUE

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LUXE

96	IN	LUXE_VPROG_TEST	TOP 1	TP	TPU801 TP-P4
			BOTTOM 1	TP	TPU802 TP-P4
96 53	IN	I2C_LUXE_DEBUG_SCL	TOP 1	TP	TPU803 TP-P4
			BOTTOM 1	TP	TPU804 TP-P4
96 53	IN	I2C_LUXE_DEBUG_SDA	TOP 1	TP	TPU805 TP-P4
			BOTTOM 1	TP	TPU806 TP-P4
126 96	IN	PP1V25_AWAKE_IO	PLACE_NEAR=UP800:30MM 1	TP	TPU807 TP-P4
128 96	IN	PP5V_S2_HOLD	PLACE_NEAR=UP800:30MM 1	TP	TPU808 TP-P4

DISPLAY

94	IN	LPDP_INT_AUX_N	1	TP	TPU8C0 TP-P4
94	IN	LPDP_INT_AUX_P	1	TP	TPU8C1 TP-P4
94	IN	LPDP_INT_AUX_L_N	1	TP	TPU8C2 TP-P4
94	IN	LPDP_INT_AUX_L_P	1	TP	TPU8C3 TP-P4

SD

85 83	IN	I2C_SD_DEBUG_3V3_SCL	TOP 1	TP	TPU8E0 TP-P4
85 83	IN	I2C_SD_DEBUG_3V3_SDA	TOP 1	TP	TPU8E1 TP-P4
53	IN	I2C_SD_DEBUG_SCL	TOP 1	TP	TPU8E2 TP-P4
53	IN	I2C_SD_DEBUG_SDA	TOP 1	TP	TPU8E3 TP-P4

<RDAR://70680903>

6	B1	TP_TST_CLKOUT	BOTTOM 1	TP	TPU810 TP-P4
			TOP 1	TP	TPU811 TP-P4

SPKRAMP

134 103 102 7	IN	SPKRAMP_RESET_L	BOTTOM 1	TP	TPU820 TP-P4
134 103 102 7	IN	SPKRAMP_INT_L	BOTTOM 1	TP	TPU821 TP-P4
131 102	IN	TDM_SPKRAMP_L_BCLK	PLACE_NEAR=UR600.E1:20MM BOTTOM 1	TP	TPU822 TP-P4
131 102	IN	TDM_SPKRAMP_L_FSYNC	PLACE_NEAR=UR600.D2:20MM BOTTOM 1	TP	TPU823 TP-P4
131 102	IN	TDM_SPKRAMP_L_R2D	PLACE_NEAR=UR600.E2:20MM BOTTOM 1	TP	TPU824 TP-P4
131 102	IN	TDM_SPKRAMP_L_D2R	PLACE_NEAR=U0600.V6:20MM BOTTOM 1	TP	TPU825 TP-P4
102	IN	SPKRAMP_ABC_ICC	BOTTOM 1	TP	TPU826 TP-P4
102	IN	TP_SPKRAMP_A_LV_EN	BOTTOM 1	TP	TPU829 TP-P4
102	IN	TP_SPKRAMP_B_LV_EN	BOTTOM 1	TP	TPU830 TP-P4
102	IN	TP_SPKRAMP_C_LV_EN	BOTTOM 1	TP	TPU831 TP-P4
131 103	IN	TDM_SPKRAMP_R_BCLK	PLACE_NEAR=UR700.E1:20MM BOTTOM 1	TP	TPU832 TP-P4
131 103	IN	TDM_SPKRAMP_R_FSYNC	PLACE_NEAR=UR700.E1:20MM BOTTOM 1	TP	TPU833 TP-P4
131 103	IN	TDM_SPKRAMP_R_R2D	PLACE_NEAR=UR700.E1:20MM BOTTOM 1	TP	TPU834 TP-P4
131 103	IN	TDM_SPKRAMP_R_D2R	PLACE_NEAR=U0600.V4:26MM BOTTOM 1	TP	TPU835 TP-P4
103	IN	TP_SPKRAMP_D_LV_EN	BOTTOM 1	TP	TPU838 TP-P4
103	IN	TP_SPKRAMP_E_LV_EN	BOTTOM 1	TP	TPU839 TP-P4
103	IN	TP_SPKRAMP_F_LV_EN	BOTTOM 1	TP	TPU840 TP-P4
103	IN	SPKRAMP_DEF_ICC_R	BOTTOM 1	TP	TPU841 TP-P4

CODEC

101	IN	PP3V8_CODEC_VP	PLACE_NEAR=UR500.C7:20MM BOTTOM 1	TP	TPU850 TP-P4
101	IN	PP1V8_CODEC_VCP	PLACE_NEAR=UR500.D6:20MM BOTTOM 1	TP	TPU851 TP-P4
133 101 7	IN	CODEC_RESET_L	PLACE_NEAR=UR500.D4:20MM BOTTOM 1	TP	TPU852 TP-P4
134 101 7	IN	CODEC_INT_L	PLACE_NEAR=UR500.B7:20MM BOTTOM 1	TP	TPU853 TP-P4
101 14	IN	TDM_CODEC_FSYNC	PLACE_NEAR=UR500.B2:20MM BOTTOM 1	TP	TPU854 TP-P4
101 14	IN	TDM_CODEC_R2D	PLACE_NEAR=UR500.B3:20MM BOTTOM 1	TP	TPU855 TP-P4
135 101 8	IN	TDM_CODEC_D2R	PLACE_NEAR=U0600.BF20:20MM BOTTOM 1	TP	TPU856 TP-P4
101 14	IN	TDM_CODEC_BCLK	PLACE_NEAR=UR500.A3:20MM BOTTOM 1	TP	TPU857 TP-P4

I2C

115 103 53	IN	I2C_HDMI_SPKRAMP_R_SCL	PLACE_NEAR=UR730.F2:20MM BOTTOM 1	TP	TPU836 TP-P4
115 103 53	IN	I2C_HDMI_SPKRAMP_R_SDA	PLACE_NEAR=UR730.F1:20MM BOTTOM 1	TP	TPU837 TP-P4
115 103 53	IN	I2C_HDMI_SPKRAMP_R_SCL	PLACE_NEAR=UH700.L8:30MM BOTTOM 1	TP	TPU83A TP-P4
115 103 53	IN	I2C_HDMI_SPKRAMP_R_SDA	PLACE_NEAR=UH700.L8:30MM BOTTOM 1	TP	TPU83B TP-P4
115 101 52	IN	I2C_SPKRAMP_L_CODEC_SDA	PLACE_NEAR=UR500.B6:20MM BOTTOM 1	TP	TPU858 TP-P4
115 101 52	IN	I2C_SPKRAMP_L_CODEC_SCL	PLACE_NEAR=UR500.A5:20MM BOTTOM 1	TP	TPU859 TP-P4
115 101 52	IN	I2C_SPKRAMP_L_CODEC_SDA	PLACE_NEAR=UR630.F1:20MM TOP 1	TP	TPU85C TP-P4
115 101 52	IN	I2C_SPKRAMP_L_CODEC_SCL	PLACE_NEAR=UR630.F2:20MM TOP 1	TP	TPU85D TP-P4

SYNC_MOTHERPATRICK_SCHEC_REV SYNC_DATE=05/24/2022

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TP SUPPORT

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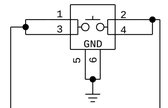
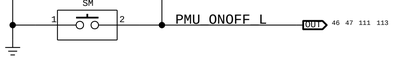
POWER BUTTON

DEBUG_BUTTON
PLACE_SIDE=BOTTOM
1.4 MM TALL
SV000
SKSGPCE010
SM

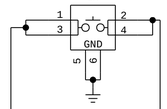


DEBUG_BUTTON
PLACE_SIDE=TOP
0.60 MM TALL
SV001
SKSWCEE010
SM

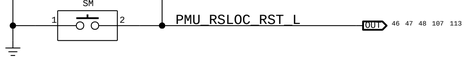


RSLOC

DEBUG_BUTTON
PLACE_SIDE=BOTTOM
1.4 MM TALL
SV002
SKSGPCE010
SM

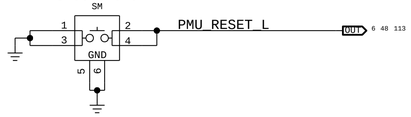


DEBUG_BUTTON
PLACE_SIDE=TOP
0.60 MM TALL
SV003
SKSWCEE010
SM



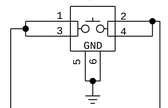
RESET (RESET SOC ONLY)

NOSTUFF
PLACE_SIDE=BOTTOM
1.4 MM TALL
SV008
SKSGPCE010
SM

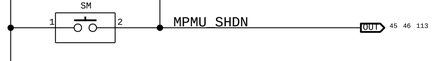


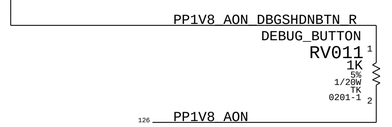
PMU SHUTDOWN

DEBUG_BUTTON
PLACE_SIDE=BOTTOM
1.4 MM TALL
SV010
SKSGPCE010
SM



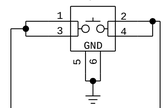
DEBUG_BUTTON
PLACE_SIDE=TOP
0.60 MM TALL
SV011
SKSWCEE010
SM



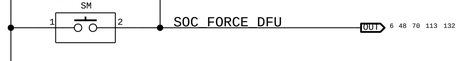


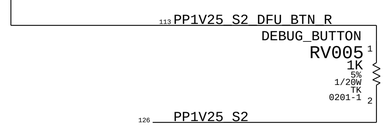
FORCE DFU

DEBUG_BUTTON
PLACE_SIDE=BOTTOM
1.4 MM TALL
SV004
SKSGPCE010
SM



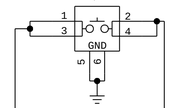
DEBUG_BUTTON
PLACE_SIDE=TOP
0.60 MM TALL
SV005
SKSWCEE010
SM



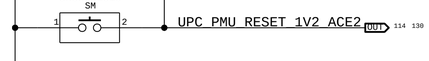


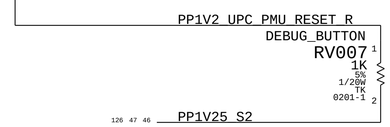
UPC RESET (RESET PMU)

DEBUG_BUTTON
PLACE_SIDE=BOTTOM
1.4 MM TALL
SV006
SKSGPCE010
SM



DEBUG_BUTTON
PLACE_SIDE=TOP
0.60 MM TALL
SV007
SKSWCEE010
SM





BOM_COST_GROUP=DEBUG

PAGE TITLE
DEBUG: BUTTONS

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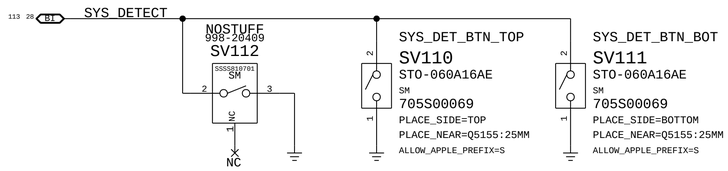
BUTTONS TO DISCONNECT BATTERY WITHOUT UNPLUGGING FLEX

SV112 CAN BE MANUALLY ADDED FOR CHARACTERIZATION IF DESIRED



MADI DEBUG INTERFACE

PLACE ON BOTTOM SIDE EASILY ACCESSIBLE
<RDAR://70197137>

HPD TMU CLKOUT TEST POINTS

<RDAR://70197956>

MPMU FORCE SYNC TP

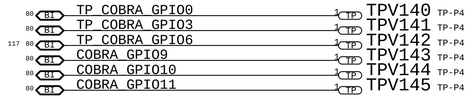
IN STOWE, FORCE_SYNC (FORCE BUCKS TO PWM) IS OVERLOADED ON GPIO 9
<RDAR://71572096>

DOCK ATTENTION TP

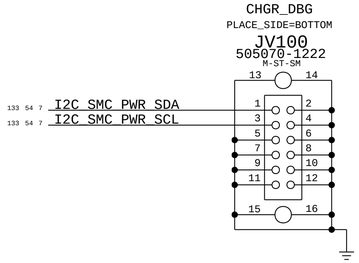
<RDAR://71293051>

LUXE TEST POINTS

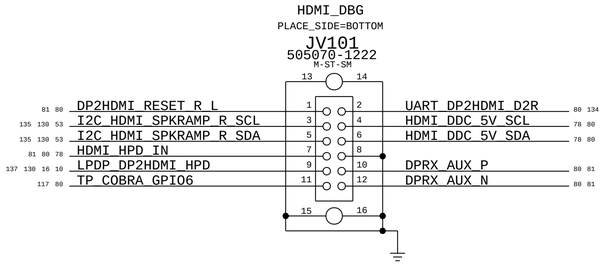
HDMI TEST POINTS



CHARGER ARKANOID CONN

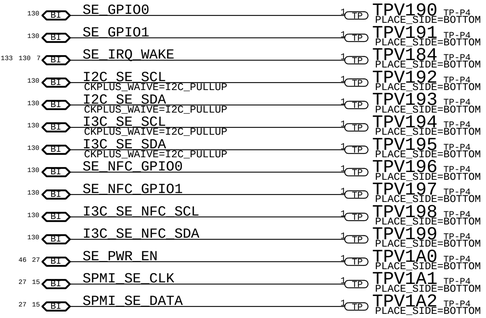


COBRA0 ARKANOID CONN

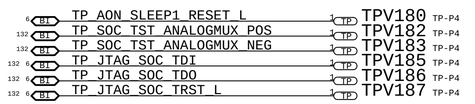


SE SW TEAM DEBUG TEST POINTS

<RDAR://88267382>



EXTRA SOC TEST POINTS



BOM_COST_GROUP=DEBUG

PAGE TITLE
DEBUG: MISC

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DFM DUMMY COMPONENTS TO PROTECT UL101

116S00022
RV350
0
1 2
0% 1/16W TK 0402
PLACE_NEAR=UL101:2MM
CKPLUS_WAIVE=TERMSHORTED

DFM DUMMY COMPONENTS FOR UF260 RDAR://102994677

RV351
0
1 2
0% 1/20W TK 0201
117S00073
PLACE_NEAR=UF260:20MM
CKPLUS_WAIVE=TERMSHORTED

RV352
0
1 2
0% 1/20W TK 0201
117S00073
PLACE_NEAR=UF260:20MM
CKPLUS_WAIVE=TERMSHORTED

RV353
0
1 2
0% 1/20W TK 0201
117S00073
PLACE_NEAR=UF260:20MM
CKPLUS_WAIVE=TERMSHORTED

RV354
0
1 2
0% 1/20W TK 0201
117S00073
PLACE_NEAR=UF260:20MM
CKPLUS_WAIVE=TERMSHORTED

RV355
0
1 2
0% 1/20W TK 0201
117S00073
PLACE_NEAR=UF260:20MM
CKPLUS_WAIVE=TERMSHORTED

BOM_COST_GROUP=DFM

PAGE TITLE: DFM DUMMY PARTS

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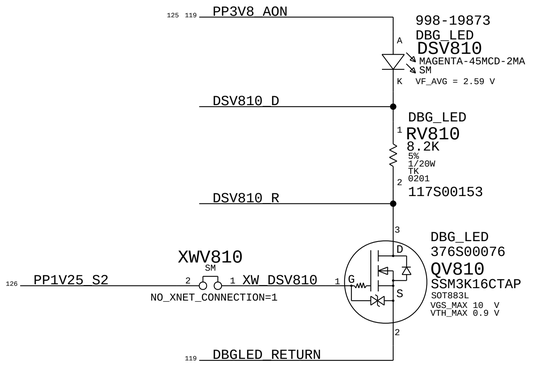
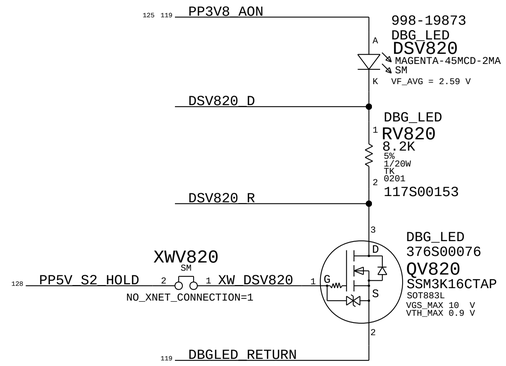
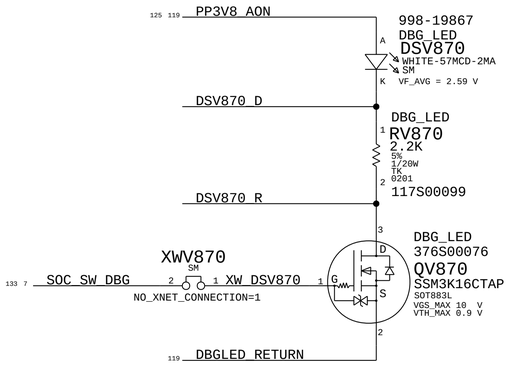
S2 LEDS (MAGENTA)

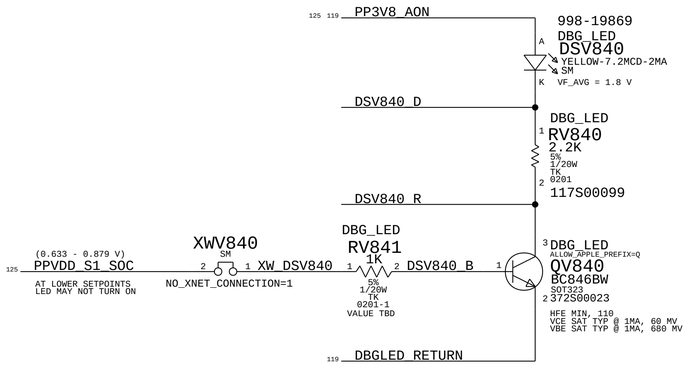




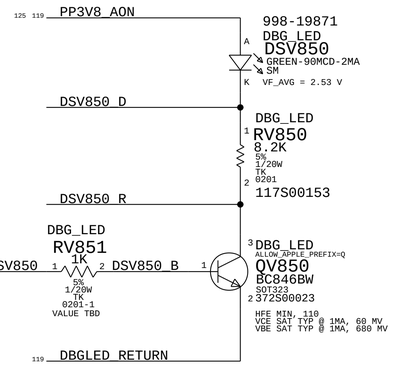
SOC SW_DBG (WHITE)

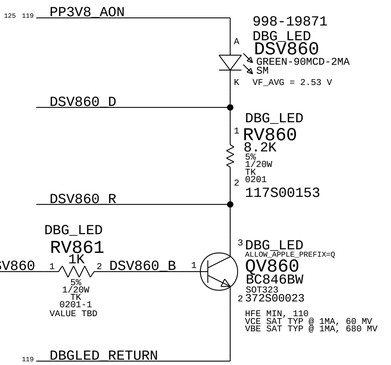


S1 LED (YELLOW)

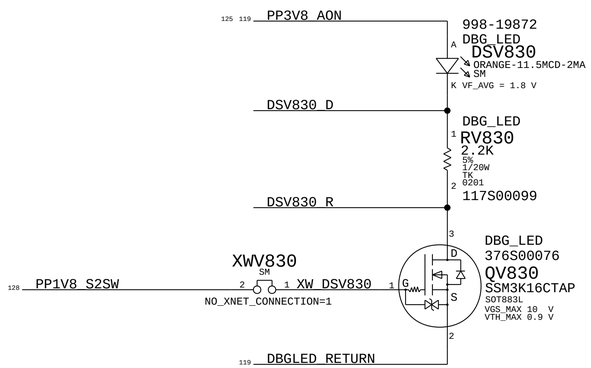


AWAKE LEDS (GREEN)

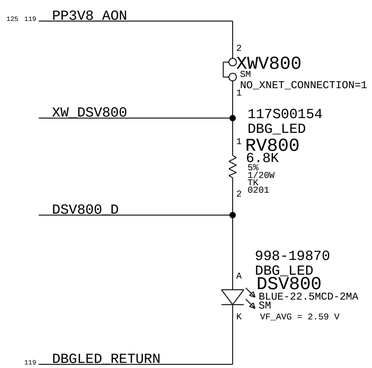




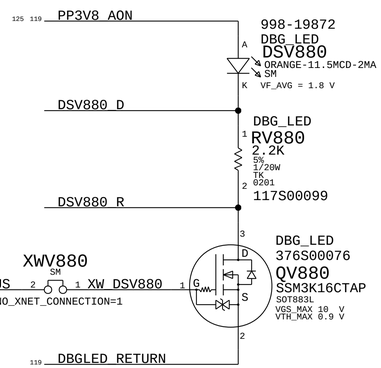
S2SW LED (ORANGE)



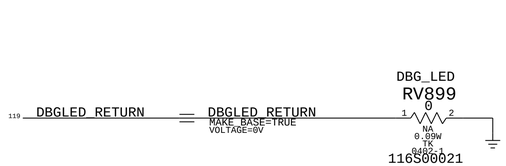
AON LED (BLUE)



DFU STATUS LED (ORANGE)



DEBUG LED ENABLE JUMPER



BOM_COST_GROUP=DEBUG

PAGE TITLE: DEBUG: LEDS

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SOC DESENSE

PPVDD_AWAKE_ECPU
CY000 131S0445 NP0-C0G 0201 25V 5%
CY001 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY002 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY003 131S0445 NP0-C0G 0201 25V 5% 12PF
CY004 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY005 131S0198 C0G 201 25V+/-0.1PF 1.8PF

PPVDD_S1_SOC
CY010 131S0445 NP0-C0G 0201 25V 5% 12PF
CY011 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY012 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY013 131S0445 NP0-C0G 0201 25V 5% 12PF
CY014 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY015 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY016 131S0445 NP0-C0G 0201 25V 5% 12PF

PPVDD_AWAKE_GPU
CY020 131S0445 NP0-C0G 0201 25V 5% 12PF
CY021 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY022 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY023 131S0445 NP0-C0G 0201 25V 5% 12PF
CY024 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY025 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY026 131S0445 NP0-C0G 0201 25V 5% 12PF PLACE_SIDE=BOTTOM
CY027 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF PLACE_SIDE=BOTTOM
CY028 131S0445 NP0-C0G 0201 25V 5% 12PF

PPVDD_AWAKE_CPU_SRAM
CY030 131S0445 NP0-C0G 0201 25V 5% 12PF
CY031 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY032 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY033 131S0445 NP0-C0G 0201 25V 5% 12PF

PP1V12_S2SW_AMPH
CY040 131S0445 NP0-C0G 0201 25V 5% 12PF
CY041 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY042 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY043 131S0445 NP0-C0G 0201 25V 5% 12PF
CY044 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY045 131S0198 C0G 201 25V+/-0.1PF 1.8PF

PP0V72_S2_VDD_LOW
CY050 131S0445 NP0-C0G 0201 25V 5% 12PF
CY051 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY052 131S0198 C0G 201 25V+/-0.1PF 1.8PF

PPVDD_S2SW_VDD2H
CY060 131S0445 NP0-C0G 0201 25V 5% 12PF
CY061 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY062 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY063 131S0445 NP0-C0G 0201 25V 5% 12PF
CY064 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY065 131S0198 C0G 201 25V+/-0.1PF 1.8PF

PPVDD_S2SW_VDD2H
CY070 131S0445 NP0-C0G 0201 25V 5% 12PF NOSTUFF
CY071 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY072 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY073 131S0445 NP0-C0G 0201 25V 5% 12PF
CY074 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY075 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY076 131S0445 NP0-C0G 0201 25V 5% 12PF
CY077 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF

PPVDD_AWAKE_PCPU
CY080 131S0445 NP0-C0G 0201 25V 5% 12PF
CY081 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY082 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY083 131S0445 NP0-C0G 0201 25V 5% 12PF
CY084 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY085 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY086 131S0445 NP0-C0G 0201 25V 5% 12PF PLACE_SIDE=BOTTOM
CY087 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF PLACE_SIDE=BOTTOM

PP0V779_S1_SRAM
CY090 131S0445 NP0-C0G 0201 25V 5% 12PF
CY091 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY092 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY093 131S0445 NP0-C0G 0201 25V 5% 12PF
CY094 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF

PPVDD_S1_DCS
CY0A0 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0A1 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0A2 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY0A3 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0A4 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0A5 131S0198 C0G 201 25V+/-0.1PF 1.8PF

PPVDD_S1_DISP
CY0B0 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0B1 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0B2 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY0B3 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0B4 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0B5 131S0198 C0G 201 25V+/-0.1PF 1.8PF

PP0V8_S1_VDD_FIXED
CY0C0 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0C1 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0C2 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY0C3 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0C4 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0C5 131S0198 C0G 201 25V+/-0.1PF 1.8PF

PP1V8_S2SW
CY0D0 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0D1 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0D2 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY0D3 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0D4 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0D5 131S0198 C0G 201 25V+/-0.1PF 1.8PF

PP1V25_S2
CY0E0 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0E1 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF

PP1V2_AWAKE_PLL
CY0F0 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0F1 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0F2 131S0198 C0G 201 25V+/-0.1PF 1.8PF

PP1V25_AWAKE_IO
CY0G0 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0G1 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0G2 131S0198 C0G 201 25V+/-0.1PF 1.8PF

PPVDD_S1_VDDQL
CY0H0 BOTTOM 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0H1 BOTTOM 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0H2 BOTTOM 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY0H3 131S0445 NP0-C0G 0201 25V 5% 12PF NOSTUFF
CY0H4 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0H5 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY0H6 131S0445 NP0-C0G 0201 25V 5% 12PF NOSTUFF
CY0H7 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0H8 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY0H9 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0HA 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0HB 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY0HC 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0HD 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0HE 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY0HF 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0HG 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0HH 131S0198 C0G 201 25V+/-0.1PF 1.8PF
CY0HI 131S0445 NP0-C0G 0201 25V 5% 12PF
CY0HJ 131S0439 NP0-C0G 0201 25V+/-0.1PF 3.0PF
CY0HK 131S0198 C0G 201 25V+/-0.1PF 1.8PF

PPVDDIO12_GRP1_XW
CY0I0 131S0445 NP0-C0G 0201 25V 5% 12PF

PPVDDIO12_GRP6_XW
CY0J0 131S0445 NP0-C0G 0201 25V 5% 12PF

PPVDDIO12_GRP3_XW
CY0K0 131S0445 NP0-C0G 0201 25V 5% 12PF

PP1V2_S2_CIO
CY0L0 131S0445 NP0-C0G 0201 25V 5% 12PF

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	Apple Inc.
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PMU DESENSE

PP3V8_AON_SPMU_ISNS_VIN (129)
- CY100 12PF
- CY101 3.0PF
- CY102 1.8PF
- CY103 12PF
- CY104 3.0PF
- CY105 1.8PF
- CY106 12PF
- CY107 3.0PF
- CY108 1.8PF
- CY109 12PF
- CY10A 3.0PF
- CY10B 1.8PF
- CY10C 12PF
- CY10D 3.0PF
- CY10E 1.8PF
- CY10F 12PF
- CY10G 3.0PF
- CY10H 1.8PF
- CY10I 12PF
- CY10J 3.0PF
- CY10K 1.8PF
- CY10L 12PF
- CY10M 3.0PF
- CY10N 1.8PF

PPVDD_AWAKE_PCPU (125)
- CY110 12PF
- CY111 3.0PF
- CY112 1.8PF
- CY113 12PF
- CY114 3.0PF
- CY115 1.8PF

PPVDD_S1_SOC (125)
- CY120 12PF
- CY121 3.0PF
- CY122 1.8PF
- CY123 12PF
- CY124 3.0PF
- CY125 1.8PF

PPVDD_AWAKE_GPU (125)
- CY130 12PF
- CY131 3.0PF
- CY132 1.8PF
- CY133 12PF
- CY134 3.0PF
- CY135 1.8PF

PP3V8_AON_MPMU_ISNS_VIN (129)
- CY140 12PF
- CY141 3.0PF
- CY142 1.8PF
- CY143 12PF
- CY144 3.0PF
- CY145 1.8PF
- CY146 12PF
- CY147 3.0PF
- CY148 1.8PF
- CY149 12PF
- CY14A 3.0PF
- CY14B 1.8PF
- CY14C 12PF
- CY14D 3.0PF
- CY14E 1.8PF
- CY14F 12PF
- CY14G 3.0PF
- CY14H 1.8PF
- CY14I 12PF
- CY14J 3.0PF
- CY14K 1.8PF
- CY14L 12PF
- CY14M 3.0PF
- CY14N 1.8PF
- CY14P 12PF
- CY14Q 3.0PF
- CY14R 1.8PF
- CY14S 12PF
- CY14T 3.0PF
- CY14U 1.8PF
- CY14V 12PF
- CY14W 3.0PF
- CY14X 1.8PF

PP1V25_S2 (126)
- CY160 12PF
- CY161 3.0PF
- CY162 1.8PF

PP5V_SPMU_BSTLQ (127)
- CY170 12PF
- CY171 3.0PF
- CY172 1.8PF

PPVDD_S2SW_VDD2H (125)
- CY190 12PF
- CY191 3.0PF
- CY192 1.8PF

PPVDD_AWAKE_CPU_SRAM (125)
- CY1A0 12PF
- CY1A1 3.0PF
- CY1A2 1.8PF

PPVDD_S1_VDDQL (125)
- CY1B0 12PF
- CY1B1 3.0PF
- CY1B2 1.8PF

PP0V779_S1_SRAM (125)
- CY1C0 12PF
- CY1C1 3.0PF
- CY1C2 1.8PF

PPVDD_S1_DISP (125)
- CY1D0 12PF
- CY1D1 3.0PF
- CY1D2 1.8PF

PPVDD_AWAKE_ECPU (125)
- CY1E0 12PF
- CY1E1 3.0PF
- CY1E2 1.8PF

PP1V8_S2 (125)
- CY1F0 12PF
- CY1F1 3.0PF
- CY1F2 1.8PF

PP2V58_AWAKE_NAND_VCC (125)
- CY1G0 12PF
- CY1G1 3.0PF
- CY1G2 1.8PF

PPVDD_S1_DCS (125)
- CY1H0 12PF
- CY1H1 3.0PF
- CY1H2 1.8PF

PP0V88_S1 (125)
- CY1I0 12PF
- CY1I1 3.0PF
- CY1I2 1.8PF

PP5V_MPMU_BSTLQ (127)
- CY1J0 12PF
- CY1J1 3.0PF
- CY1J2 1.8PF

PP1V2_AON_SPMU (127)
- CY1K0 12PF
- CY1K1 3.0PF
- CY1K2 1.8PF

PP0V88_AWAKE_NAND_VDD (126)
- CY1L0 12PF
- CY1L1 3.0PF
- CY1L2 1.8PF

PP1V12_S2SW_AMPH (126)
- CY1M0 12PF
- CY1M1 3.0PF
- CY1M2 1.8PF

PP1V2_AON_MPMU (127)
- CY1N0 12PF
- CY1N1 3.0PF
- CY1N2 1.8PF

PP1V25_AWAKE_NAND_VCCQ (126)
- CY1P0 12PF
- CY1P1 3.0PF
- CY1P2 1.8PF

Each capacitor: 131S0445 NP0-C0G 0201 25V 5% / 131S0439 NP0-C0G 0201 25V+/-0.1PF / 131S0198 C0G 201 25V+/-0.1PF

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	Apple Inc.
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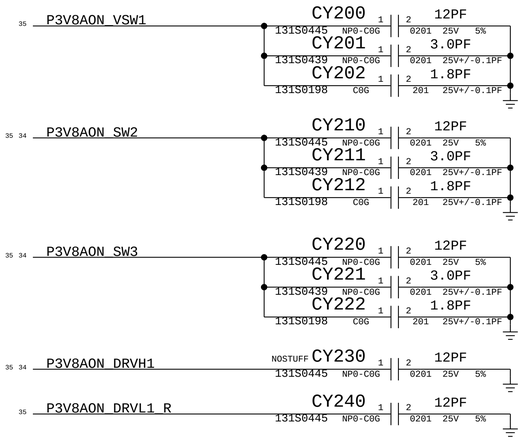
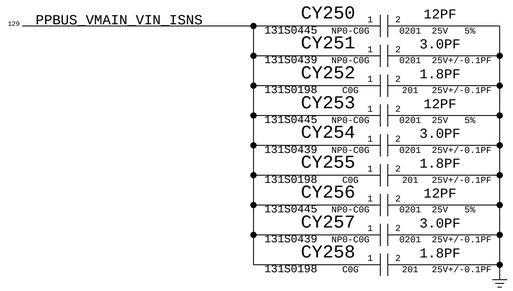
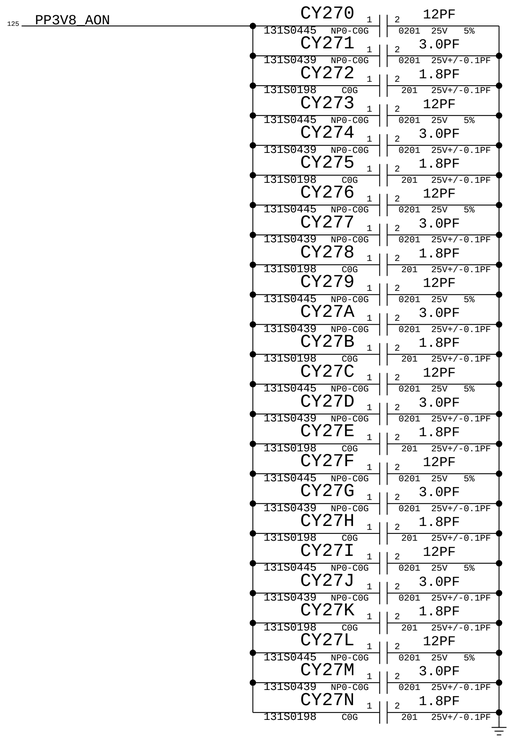
ICEMAN DESENSE







BOM_COST_GROUP=DESENSE

PAGE TITLE: DESENSE CAPS (3/4)

Apple Inc.

DRAWING NUMBER: 051-07754 SIZE: D

REVISION: 6.0.0

BRANCH: dvt-1

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BACKLIGHT DESENSE

129 PPBUS_AON_BKLT_ISNS
- CY300 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY301 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY302 1.8PF 131S0198 C0G 201 25V+/-0.1PF

96 PPLUXE_LX1
- NOSTUFF CY310 12PF 131S0445 NP0-C0G 0201 25V 5%
- NOSTUFF CY311 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- NOSTUFF CY312 1.8PF 131S0198 C0G 201 25V+/-0.1PF

96 PPLUXE_LX2
- NOSTUFF CY320 12PF 131S0445 NP0-C0G 0201 25V 5%
- NOSTUFF CY321 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- NOSTUFF CY322 1.8PF 131S0198 C0G 201 25V+/-0.1PF

96 PPVOUT_LUXE_XW
- CY330 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY331 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY332 1.8PF 131S0198 C0G 201 25V+/-0.1PF

96 PPLUXE_INPUT_R_V
- CY340 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY341 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY342 1.8PF 131S0198 C0G 201 25V+/-0.1PF

USB CIO VR DESENSE

128 70 67 PP1V2_USBC_VDDIO
- CY3Q0 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY3Q1 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY3Q2 1.8PF 131S0198 C0G 201 25V+/-0.1PF

128 67 PP0V855_USBC_CIO
- CY3R0 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY3R1 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY3R2 1.8PF 131S0198 C0G 201 25V+/-0.1PF

128 67 PP0V805_USBC_FIXED
- CY3S0 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY3S1 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY3S2 1.8PF 131S0198 C0G 201 25V+/-0.1PF

IPD SPI DESENSE

109 SPI_IPD_MOSI_CONN_R
- CY3T0 12PF 131S0445 NP0-C0G 0201 25V 5%

114 110 109 SPI_IPD_MISO_CONN
- CY3T1 12PF 131S0445 NP0-C0G 0201 25V 5%

109 SPI_IPD_CLK_CONN_R
- CY3T2 12PF 131S0445 NP0-C0G 0201 25V 5%

109 14 SPI_IPD_CLK
- CY3T3 12PF 131S0445 NP0-C0G 0201 25V 5%

109 14 SPI_IPD_MOSI
- CY3T4 12PF 131S0445 NP0-C0G 0201 25V 5%

109 SPI_IPD_MISO_R
- CY3T5 12PF 131S0445 NP0-C0G 0201 25V 5%

DCIN DESENSE

113 29 PPDCIN_AON_CHGR_R
- CY350 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY351 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY352 1.8PF 131S0198 C0G 201 25V+/-0.1PF
- CY353 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY354 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY355 1.8PF 131S0198 C0G 201 25V+/-0.1PF
- CY356 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY357 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY358 1.8PF 131S0198 C0G 201 25V+/-0.1PF
- CY359 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY35A 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY35B 1.8PF 131S0198 C0G 201 25V+/-0.1PF

125 PPDCIN_USBC_AON
- CY360 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY361 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY362 1.8PF 131S0198 C0G 201 25V+/-0.1PF

VBAT DESENSE

125 113 29 PPVBAT_AON_CHGR_REG
- CY370 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY371 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY372 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF

USB 5V DESENSE

129 PPBUS_AON_PORT5V_VIN_ISNS
- CY380 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY381 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY382 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF

128 113 PP5V_S2_UPC
- CY390 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY391 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY392 1.8PF 131S0198 C0G 201 25V+/-0.1PF

WIFI DESENSE

129 87 PP3V8_AON_WLBT_ISNS
- CY3F0 1.8PF 131S0198 C0G 201 25V+/-0.1PF PLACE_NEAR=U800.11:10MM
- CY3F1 1.8PF 131S0198 C0G 201 25V+/-0.1PF PLACE_NEAR=U800.70:10MM
- CY3F2 1.8PF 131S0198 C0G 201 25V+/-0.1PF PLACE_NEAR=U800.48:10MM
- CY3F3 1.8PF 131S0198 C0G 201 25V+/-0.1PF PLACE_NEAR=U800.38:10MM

129 87 PP1V8_S2_WLBT_ISNS
- CY3G0 1.8PF 131S0198 C0G 201 25V+/-0.1PF PLACE_NEAR=U800.4:10MM
- CY3G1 1.8PF 131S0198 C0G 201 25V+/-0.1PF PLACE_NEAR=U800.22:10MM

KBD DESENSE

129 106 PP5V_S2_HOLD_KBDLED_ISNS
- CY3A0 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY3A1 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY3A2 1.8PF 131S0198 C0G 201 25V+/-0.1PF

106 KBDBKLT_SW2
- NOSTUFF CY3B0 3PF 131S00140 C0G 0201 100V+/-0.1PF

5V S2 DESENSE

128 PP5V_S2_HOLD
- CY3C0 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY3C1 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY3C2 1.8PF 131S0198 C0G 201 25V+/-0.1PF
- CY3C3 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY3C4 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY3C5 1.8PF 131S0198 C0G 201 25V+/-0.1PF

129 PPBUS_AON_5VS2_VIN_ISNS
- CY3D0 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY3D1 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY3D2 1.8PF 131S0198 C0G 201 25V+/-0.1PF
- CY3D3 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY3D4 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY3D5 1.8PF 131S0198 C0G 201 25V+/-0.1PF

126 PP1V25_S2
- CY3E0 12PF 131S0445 NP0-C0G 0201 25V 5%
- CY3E1 3.0PF 131S0439 NP0-C0G 0201 25V+/-0.1PF
- CY3E2 1.8PF 131S0198 C0G 201 25V+/-0.1PF

BOM_COST_GROUP=DESENSE

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	Apple Inc.
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DESENSE POGO PINS

870-12170
ALLOW_APPLE_PREFIX=BP
BPZ000
POGO-2.30D-4.33H-SM
SM
1

870-12170
ALLOW_APPLE_PREFIX=BP
BPZ001
POGO-2.30D-4.33H-SM
SM
1

870-12170
ALLOW_APPLE_PREFIX=BP
BPZ002
POGO-2.30D-4.33H-SM
SM
1

870-12170
ALLOW_APPLE_PREFIX=BP
BPZ003
POGO-2.30D-4.33H-SM
SM
1

870-12170
ALLOW_APPLE_PREFIX=BP
BPZ004
POGO-2.30D-4.33H-SM
SM
1

870-12170
ALLOW_APPLE_PREFIX=BP
BPZ005
POGO-2.30D-4.33H-SM
SM
1

870-12170
ALLOW_APPLE_PREFIX=BP
BPZ006
POGO-2.30D-4.33H-SM
SM
1

870-12170
ALLOW_APPLE_PREFIX=BP
BPZ007
POGO-2.30D-4.33H-SM
SM
1

870-12170
ALLOW_APPLE_PREFIX=BP
BPZ008
POGO-2.30D-4.33H-SM
SM
1

870-12170
ALLOW_APPLE_PREFIX=BP
BPZ009
POGO-2.30D-4.33H-SM
SM
1

870-12170
ALLOW_APPLE_PREFIX=BP
BPZ010
POGO-2.30D-4.33H-SM
SM
1

870-12170
ALLOW_APPLE_PREFIX=BP
BPZ011
POGO-2.30D-4.33H-SM
SM
1

SHIELD CAN ALIGNMENT SLOTS

998-04440
ALLOW_APPLE_PREFIX=BS
BSZ050
TH-NSP
1
SL-1.2X0.4-1.5X0.7

998-04440
ALLOW_APPLE_PREFIX=BS
BSZ051
TH-NSP
1
SL-1.2X0.4-1.5X0.7

998-04440
ALLOW_APPLE_PREFIX=BS
BSZ052
TH-NSP
1
SL-1.2X0.4-1.5X0.7

998-04440
ALLOW_APPLE_PREFIX=BS
BSZ053
TH-NSP
1
SL-1.2X0.4-1.5X0.7

998-04440
ALLOW_APPLE_PREFIX=BS
BSZ054
TH-NSP
1
SL-1.2X0.4-1.5X0.7

998-04440
ALLOW_APPLE_PREFIX=BS
BSZ055
TH-NSP
1
SL-1.2X0.4-1.5X0.7

998-04440
ALLOW_APPLE_PREFIX=BS
BSZ056
TH-NSP
1
SL-1.2X0.4-1.5X0.7

998-04440
ALLOW_APPLE_PREFIX=BS
BSZ057
TH-NSP
1
SL-1.2X0.4-1.5X0.7

998-04440
ALLOW_APPLE_PREFIX=BS
BSZ058
TH-NSP
1
SL-1.2X0.4-1.5X0.7

998-04440
ALLOW_APPLE_PREFIX=BS
BSZ059
TH-NSP
1
SL-1.2X0.4-1.5X0.7

998-04440
ALLOW_APPLE_PREFIX=BS
BSZ060
TH-NSP
1
SL-1.2X0.4-1.5X0.7

998-04440
ALLOW_APPLE_PREFIX=BS
BSZ061
TH-NSP
1
SL-1.2X0.4-1.5X0.7

DESENSE SHIELD CANS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
806-36862	1	SHIELD,FENCE,LONG,X2659	SHIELD_LONG	SHIELD_LONG:YES
806-36861	1	SHIELD,FENCE,HDMI,X2659	SHIELD_HDMI	SHIELD_HDMI:YES
806-40248	1	SHIELD,FENCE,STOWE,X2659	SHIELD_MPMU	SHIELD_MPMU:YES
806-36866	1	SHIELD,FENCE,RT13,X2659	SHIELD_USBC	SHIELD_USBC:YES
806-36865	1	SHIELD,FENCE,VR,X2659	SHIELD_VR	SHIELD_VR:YES
806-36863	1	SHIELD,FENCE,BCKLT,X2659	SHIELD_BKLT	SHIELD_BKLT:YES

BOM_COST_GROUP=DESENSE

PAGE TITLE
DESENSE MECHANICAL PARTS

Apple Inc.

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VBAT

29 28 PPVBAT_AON
PPVBAT_AON
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1500
MIN_LINE_WIDTH=0.6000
113

USBC DCIN

29 28 PPDCIN_USBC_AON
PPDCIN_USBC_AON
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PPDCIN_USBC_AON 33
PPDCIN_USBC_AON 57 62
PPDCIN_USBC_AON 123
PPDCIN_USBC_AON 69
PPDCIN_USBC_AON 33

PBUS

29 PPBUS_AON
PPBUS_AON
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PPBUS_AON 57
PPBUS_AON 59
PPBUS_AON 59
PPBUS_AON 58
PPBUS_AON 44
PPBUS_AON 57
PPBUS_AON 58
PPBUS_AON 57
PPBUS_AON 110

PPVBAT

125 123 113 29 PPVBAT_AON_CHGR_REG
PPVBAT_AON_CHGR_REG
MAKE_BASE=TRUE
29 113 123 125
PPVBAT_AON_CHGR_REG 57

P3V8 VMAIN

35 PP3V8_AON
PP3V8_AON
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PP3V8_AON 58
PP3V8_AON 75
PP3V8_AON 101
PP3V8_AON 36 125
PP3V8_AON 57
PP3V8_AON 57
PP3V8_AON 58
PP3V8_AON 119
PP3V8_AON 28
PP3V8_AON 110
PP3V8_AON 59
PP3V8_AON 50
PP3V8_AON 95
PP3V8_AON 58
PP3V8_AON 58
PP3V8_AON 49
PP3V8_AON 27
PP3V8_AON 51
PP3V8_AON 59
PP3V8_AON 122
PP3V8_AON 107
PP3V8_AON 36 125

P3V8 LD05

34 PP5V_AON
PP5V_AON
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PP5V_AON 34

MPMU BUCK 0

41 PPVDD_AWAKE_PCPU
PPVDD_AWAKE_PCPU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PPVDD_AWAKE_PCPU 17
PPVDD_AWAKE_PCPU 119
PPVDD_AWAKE_PCPU 121
PPVDD_AWAKE_PCPU 120
PPVDD_AWAKE_PCPU 41

MPMU BUCK 1

41 PPVDD_AWAKE_GPU
PPVDD_AWAKE_GPU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PPVDD_AWAKE_GPU 20
PPVDD_AWAKE_GPU 119
PPVDD_AWAKE_GPU 121
PPVDD_AWAKE_GPU 120
PPVDD_AWAKE_GPU 41

MPMU BUCK 2

41 PPVDD_S1_SOC
PPVDD_S1_SOC
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PPVDD_S1_SOC 10
PPVDD_S1_SOC 121
PPVDD_S1_SOC 120
PPVDD_S1_SOC 119
PPVDD_S1_SOC 41

MPMU BUCK 3

47 42 PP1V8_S2
PP1V8_S2
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PP1V8_S2 50
PP1V8_S2 81 82
PP1V8_S2 51
PP1V8_S2 29
PP1V8_S2 53 54
PP1V8_S2 71
PP1V8_S2 73
PP1V8_S2 72
PP1V8_S2 59
PP1V8_S2 93
PP1V8_S2 56 125
PP1V8_S2 64
PP1V8_S2 100
PP1V8_S2 75
PP1V8_S2 42
PP1V8_S2 42
PP1V8_S2 38
PP1V8_S2 42
PP1V8_S2 37
PP1V8_S2 121
PP1V8_S2 59
PP1V8_S2 94
PP1V8_S2 105
PP1V8_S2 105
PP1V8_S2 42
PP1V8_S2 47
PP1V8_S2 56 125
PP1V8_S2 81

MPMU BUCK 4

42 PPVDD_S2SW_VDD2H
PPVDD_S2SW_VDD2H
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PPVDD_S2SW_VDD2H 21
PPVDD_S2SW_VDD2H 43
PPVDD_S2SW_VDD2H 43
PPVDD_S2SW_VDD2H 121
PPVDD_S2SW_VDD2H 120
PPVDD_S2SW_VDD2H 42

SPMU BUCK 5

37 PP0V779_S1_SRAM
PP0V779_S1_SRAM
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PP0V779_S1_SRAM 19 62
PP0V779_S1_SRAM 121
PP0V779_S1_SRAM 120
PP0V779_S1_SRAM 37

SPMU BUCK 6

40 37 PP2V58_AWAKE_NAND_VCC
PP2V58_AWAKE_NAND_VCC
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PP2V58_AWAKE_NAND_VCC 89 90
PP2V58_AWAKE_NAND_VCC 121
PP2V58_AWAKE_NAND_VCC 37 40

MPMU BUCK 7

42 PPVDD_AWAKE_CPU_SRAM
PPVDD_AWAKE_CPU_SRAM
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PPVDD_AWAKE_CPU_SRAM 19 62
PPVDD_AWAKE_CPU_SRAM 121
PPVDD_AWAKE_CPU_SRAM 120
PPVDD_AWAKE_CPU_SRAM 42

SPMU BUCK 8

37 PPVDD_S1_DISP
PPVDD_S1_DISP
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PPVDD_S1_DISP 20
PPVDD_S1_DISP 120
PPVDD_S1_DISP 121
PPVDD_S1_DISP 37

MPMU BUCK 9

42 PPVDD_S1_DCS
PPVDD_S1_DCS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PPVDD_S1_DCS 19
PPVDD_S1_DCS 120
PPVDD_S1_DCS 121
PPVDD_S1_DCS 42

SPMU BUCK 10

<RDAR://66792653>
37 PPVDD_S1_VDDQL
PPVDD_S1_VDDQL
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PPVDD_S1_VDDQL 5 21
PPVDD_S1_VDDQL 121
PPVDD_S1_VDDQL 120
PPVDD_S1_VDDQL 37

MPMU BUCK 11

42 PPVDD_AWAKE_ECPU
PPVDD_AWAKE_ECPU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PPVDD_AWAKE_ECPU 18
PPVDD_AWAKE_ECPU 120
PPVDD_AWAKE_ECPU 121
PPVDD_AWAKE_ECPU 42

SPMU BUCK 12

37 PP0V88_S1
PP0V88_S1
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
113
PP0V88_S1 38
PP0V88_S1 38
PP0V88_S1 38
PP0V88_S1 121
PP0V88_S1 37

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MPMU BUCK 13

47 42 PP1V25_S2 → PP1V25_S2 (113)
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V25_S2 (120)
PP1V25_S2 (24)
PP1V25_S2 (52 54 55)
PP1V25_S2 (27)
PP1V25_S2 (32)
PP1V25_S2 (30)
PP1V25_S2 (56 126)
PP1V25_S2 (69 71 72)
PP1V25_S2 (81)
PP1V25_S2 (119)
PP1V25_S2 (74)
PP1V25_S2 (74)
PP1V25_S2 (74)
PP1V25_S2 (73)
PP1V25_S2 (126)
PP1V25_S2 (64)
PP1V25_S2 (65)
PP1V25_S2 (87)
PP1V25_S2 (101)
PP1V25_S2 (27)
PP1V25_S2 (126)
PP1V25_S2 (116)
PP1V25_S2 (23)
PP1V25_S2 (126)
PP1V25_S2 (38)
PP1V25_S2 (42)
PP1V25_S2 (38)
PP1V25_S2 (42)
PP1V25_S2 (37)
PP1V25_S2 (73)
PP1V25_S2 (100)
PP1V25_S2 (6)
PP1V25_S2 (46 47 116)
PP1V25_S2 (93 99)
PP1V25_S2 (105)
PP1V25_S2 (106)
PP1V25_S2 (109)
PP1V25_S2 (42)
PP1V25_S2 (126)
PP1V25_S2 (16)
PP1V25_S2 (82)
PP1V25_S2 (73)
PP1V25_S2 (121)
PP1V25_S2 (111)
PP1V25_S2 (16)
PP1V25_S2 (123)
PP1V25_S2 (56 126)

SPMU BUCK 14

37 PP1V12_S2SW_AMPH → PP1V12_S2SW_AMPH (113)
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V12_S2SW_AMPH (21)
PP1V12_S2SW_AMPH (121)
PP1V12_S2SW_AMPH (120)
PP1V12_S2SW_AMPH (37)

MPMU BUCK 3 SW 1

42 PP1V8_AWAKE → PP1V8_AWAKE (113)
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V8_AWAKE (56)
PP1V8_AWAKE (13)
PP1V8_AWAKE (101)
PP1V8_AWAKE (102 103)

MPMU BUCK 3 SW 2

42 NC_PPVOUT_MPMU_SW2_REG → NC_PPVOUT_MPMU_SW2_REG
MAKE_BASE=TRUE NO_TEST=1

MPMU BUCK 13 SW 3

42 PP1V25_AWAKE_IO → PP1V25_AWAKE_IO (113)
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V25_AWAKE_IO (4 23 24 120)
PP1V25_AWAKE_IO (85)
PP1V25_AWAKE_IO (13)
PP1V25_AWAKE_IO (56)
PP1V25_AWAKE_IO (13)
PP1V25_AWAKE_IO (101 102)
PP1V25_AWAKE_IO (101)
PP1V25_AWAKE_IO (52 53)
PP1V25_AWAKE_IO (6 11)
PP1V25_AWAKE_IO (40 46)
PP1V25_AWAKE_IO (85)
PP1V25_AWAKE_IO (97)
PP1V25_AWAKE_IO (96 115)
PP1V25_AWAKE_IO (102 103)
PP1V25_AWAKE_IO (94)

SPMU BUCK 3 SW 4

38 PP1V8_AWAKE_SPMU_GPIO → PP1V8_AWAKE_SPMU_GPIO (113)
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

SPMU BUCK 13 SW 5

38 PP1V25_AWAKE_NAND_VCCQ → PP1V25_AWAKE_NAND_VCCQ (113)
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V25_AWAKE_NAND_VCCQ (89 90)
PP1V25_AWAKE_NAND_VCCQ (121)

SPMU BUCK 12 SW 6/7

38 PP0V88_AWAKE_NAND_VDD → PP0V88_AWAKE_NAND_VDD (113)
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP0V88_AWAKE_NAND_VDD (89)
PP0V88_AWAKE_NAND_VDD (90)
PP0V88_AWAKE_NAND_VDD (121)

SPMU BUCK 12 SW 7

TIED TO SW6

MPMU LDO 1

43 NC_MPMU_VLDO1 → NC_MPMU_VLDO1
MAKE_BASE=TRUE NO_TEST=1

MPMU LDO 2

43 PP1V8_AON → PP1V8_AON (113)
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V8_AON (110)
PP1V8_AON (98)
PP1V8_AON (99)
PP1V8_AON (43)
PP1V8_AON (95)
PP1V8_AON (116)
PP1V8_AON (100)
PP1V8_AON (30)
PP1V8_AON (47)
PP1V8_AON (109)
PP1V8_AON (109)

MPMU LDO 3

43 NC_MPMU_VLDO3 → NC_MPMU_VLDO3
MAKE_BASE=TRUE NO_TEST=1

SPMU LDO 4

38 PP0V72_S2_VDD_LOW → PP0V72_S2_VDD_LOW (113)
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP0V72_S2_VDD_LOW (24 62)
PP0V72_S2_VDD_LOW (38)
PP0V72_S2_VDD_LOW (120)

MPMU LDO 5

43 NC_MPMU_VLDO5 → NC_MPMU_VLDO5
MAKE_BASE=TRUE NO_TEST=1

SPMU LDO 6

38 NC_SPMU_VLDO6 → NC_SPMU_VLDO6
MAKE_BASE=TRUE NO_TEST=1

MPMU LDO 7

43 PP3V3_S2_LDO → PP3V3_S2_LDO (113)
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V3_S2_LDO (69 71 72)
PP3V3_S2_LDO (43)
PP3V3_S2_LDO (85)
PP3V3_S2_LDO (74)
PP3V3_S2_LDO (81)
PP3V3_S2_LDO (74)
PP3V3_S2_LDO (73)
PP3V3_S2_LDO (59)
PP3V3_S2_LDO (106)
PP3V3_S2_LDO (32)
PP3V3_S2_LDO (55)
PP3V3_S2_LDO (73)

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MPMU LDO 8

43 PP1V2_AWAKE_PLL

PP1V2_AWAKE_PLL — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000 — 113

PP1V2_AWAKE_PLL — 23

PP1V2_AWAKE_PLL — 23 120

PP1V2_AWAKE_PLL — 43

MPMU LDO 9

43 PP1V8_AON_MPMU

PP1V8_AON_MPMU — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.0750, MIN_LINE_WIDTH=0.1500 — 113

PP1V8_AON_MPMU — 43 45

PP1V8_AON_MPMU — 44 46 47

MPMU LDO 9B

43 PP1V2_AON_MPMU

PP1V2_AON_MPMU — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.0750, MIN_LINE_WIDTH=0.1500 — 113

PP1V2_AON_MPMU — 43

PP1V2_AON_MPMU — 42

PP1V2_AON_MPMU — 121

SPMU LDO 9

38 PP1V8_AON_SPMU

PP1V8_AON_SPMU — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.0750, MIN_LINE_WIDTH=0.1500 — 113

PP1V8_AON_SPMU — 38

SPMU LDO 9B

38 PP1V2_AON_SPMU

PP1V2_AON_SPMU — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.0750, MIN_LINE_WIDTH=0.1500 — 113

PP1V2_AON_SPMU — 38

PP1V2_AON_SPMU — 37

PP1V2_AON_SPMU — 121

MPMU LDO 10

43 PP3V3_AON

PP3V3_AON — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.0750, MIN_LINE_WIDTH=0.1500 — 113

PP3V3_AON — 98

PP3V3_AON — 43

PP3V3_AON — 107

PP3V3_AON — 28

MPMU LDO 11

43 PP0V855_S2SW_CIO

PP0V855_S2SW_CIO — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000 — 113

PP0V855_S2SW_CIO — 24

PP0V855_S2SW_CIO — 43

SPMU LDO12

38 PP0V8_S1_VDD_FIXED

PP0V8_S1_VDD_FIXED — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000 — 113

PP0V8_S1_VDD_FIXED — 22 127

PP0V8_S1_VDD_FIXED — 22 127

PP0V8_S1_VDD_FIXED — 22

PP0V8_S1_VDD_FIXED — 38

PP0V8_S1_VDD_FIXED — 120

MPMU LDO13

43 PP3V3_S2SW_SNS

PP3V3_S2SW_SNS — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000 — 113

PP3V3_S2SW_SNS — 43

PP3V3_S2SW_SNS — 61

PP3V3_S2SW_SNS — 55 57 58 59 60

MPMU LDO14

43 NC_MPMU_VLDO14 — NC_MPMU_VLDO14 — MAKE_BASE=TRUE, NO_TEST=1

SPMU LDO15

38 NC_SPMU_VLDO15 — NC_SPMU_VLDO15 — MAKE_BASE=TRUE, NO_TEST=1

MPMU LDO16

43 NC_MPMU_VLDO16 — NC_MPMU_VLDO16 — MAKE_BASE=TRUE

SPMU LDO17

38 NC_SPMU_VLDO17 — NC_SPMU_VLDO17 — MAKE_BASE=TRUE, NO_TEST=1

SPMU LDO18

38 NC_SPMU_VLDO18 — NC_SPMU_VLDO18 — MAKE_BASE=TRUE, NO_TEST=1

MPMU LDO19

(NOT USED)

MPMU LDO20

43 PP1V2_S2_CIO

PP1V2_S2_CIO — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000 — 113

PP1V2_S2_CIO — 23

PP1V2_S2_CIO — 120

PP1V2_S2_CIO — 43

MPMU LDOINT

43 PP1V5_LDOINT_MPMU

PP1V5_LDOINT_MPMU — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000 — 113

PP1V5_LDOINT_MPMU — 41

PP1V5_LDOINT_MPMU — 41

PP1V5_LDOINT_MPMU — 43

PP1V5_LDOINT_MPMU — 43

SPMU LDOINT

38 PP1V5_LDOINT_SPMU

PP1V5_LDOINT_SPMU — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000 — 113

PP1V5_LDOINT_SPMU — 37

PP1V5_LDOINT_SPMU — 37

PP1V5_LDOINT_SPMU — 38

MPMU VDD BOOST

44 PP5V_MPMU_BSTLQ

PP5V_MPMU_BSTLQ — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000 — 113

PP5V_MPMU_BSTLQ — 42

PP5V_MPMU_BSTLQ — 121

SPMU VDD BOOST

37 PP5V_SPMU_BSTLQ

PP5V_SPMU_BSTLQ — MAKE_BASE=TRUE, MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000 — 113

PP5V_SPMU_BSTLQ — 37

PP5V_SPMU_BSTLQ — 121

MPMU LDO RTC

SHORTED TO MPMU LDOINT FOR PORTABLES

SOC GUT GND DETECT

25 GND — GND — MAKE_BASE=TRUE

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KEYBOARD BACKLIGHT

106 PPVOUT_KBDLED_CONN
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ 114
→ PPVOUT_KBDLED_CONN 108

DISPLAY BACKLIGHT

128 113 97 96 PPVOUT_LUXE
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ 96 97 113 128

VDD1 1V8 SWITCH

50 PP1V8_S2SW
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ 113
→ PP1V8_S2SW 21
→ PP1V8_S2SW 120
→ PP1V8_S2SW 119

IPD 3V3 S2

110 PP3V3_S2_HOLD_IPD
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ 114
→ PP3V3_S2_HOLD_IPD 60
→ PP3V3_S2_HOLD_IPD 60

KBD 1V825 S2 LDO

107 PP1V825_S2_HOLD_KBDLDO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.825V
→ 113
→ PP1V825_S2_HOLD_KBDLDO 60

5V S2

49 PP5V_S2_HOLD
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ 113
→ PP5V_S2_HOLD 30
→ PP5V_S2_HOLD 36 128
→ PP5V_S2_HOLD 60
→ PP5V_S2_HOLD 60
→ PP5V_S2_HOLD 119
→ PP5V_S2_HOLD 81
→ PP5V_S2_HOLD 59
→ PP5V_S2_HOLD 123
→ PP5V_S2_HOLD 65
→ PP5V_S2_HOLD 96 115
→ PP5V_S2_HOLD 36 128

USB 1V2 VDDIO

76 69 PP1V2_USBC_VDDIO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ 113
→ PP1V2_USBC_VDDIO 67 70 123
→ PP1V2_USBC_VDDIO 68 70
→ PP1V2_USBC_VDDIO 67
→ PP1V2_USBC_VDDIO 68
→ PP1V2_USBC_VDDIO 67
→ PP1V2_USBC_VDDIO 68
→ PP1V2_USBC_VDDIO 67
→ PP1V2_USBC_VDDIO 68
→ PP1V2_USBC_VDDIO 67
→ PP1V2_USBC_VDDIO 68
→ PP1V2_USBC_VDDIO 74
→ PP1V2_USBC_VDDIO 74

USB 0V855 CIO

76 69 PP0V855_USBC_CIO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ 113
→ PP0V855_USBC_CIO 67 123
→ PP0V855_USBC_CIO 68

USB 0V805 FIXED

76 PP0V805_USBC_FIXED
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ 113
→ PP0V805_USBC_FIXED 67 123
→ PP0V805_USBC_FIXED 68
→ PP0V805_USBC_FIXED 67
→ PP0V805_USBC_FIXED 68

3V8 DISPLAY POWER SEQUENCER

95 PP3V8_AWAKESW_TCON
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ 113
→ PP3V8_AWAKESW_TCON 60

3V29 DISPLAY POWER SEQUENCER

95 PP3V29_BCON_AWAKESW
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ 113
→ PP3V29_BCON_AWAKESW 60

5V UPC

75 PP5V_S2_UPC
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ 113 123
→ PP5V_S2_UPC 71 72
→ PP5V_S2_UPC 71 72

BLC 1.29V

51 PP1V29_AWAKESW_BLC
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
→ 113
→ PP1V29_AWAKESW_BLC 97

MIPI SOC POWER

22 GND
MAKE_BASE=TRUE
23 GND
MAKE_BASE=TRUE

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3V8 AON HIGH SIDE SENSE RESISTOR

57 PPBUS_VMAIN_VIN_ISNS

PPBUS_VMAIN_VIN_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPBUS_VMAIN_VIN_ISNS 34 35
PPBUS_VMAIN_VIN_ISNS 122

MAIN PMU HIGH SIDE SENSE RESISTOR

57 PP3V8_AON_MPMU_ISNS_VIN

PP3V8_AON_MPMU_ISNS_VIN
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V8_AON_MPMU_ISNS_VIN 41 43 44 46
PP3V8_AON_MPMU_ISNS_VIN 43
PP3V8_AON_MPMU_ISNS_VIN 121
PP3V8_AON_MPMU_ISNS_VIN 43
PP3V8_AON_MPMU_ISNS_VIN 44 47

SECONDARY PMU HIGH SIDE SENSE RESISTOR

57 PP3V8_AON_SPMU_ISNS_VIN

PP3V8_AON_SPMU_ISNS_VIN
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V8_AON_SPMU_ISNS_VIN 37 40
PP3V8_AON_SPMU_ISNS_VIN 121
PP3V8_AON_SPMU_ISNS_VIN 38
PP3V8_AON_SPMU_ISNS_VIN 38
PP3V8_AON_SPMU_ISNS_VIN 38
PP3V8_AON_SPMU_ISNS_VIN 38

LUXE HIGH SIDE SENSE RESISTOR

58 PPBUS_AON_BKLT_ISNS

PPBUS_AON_BKLT_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPBUS_AON_BKLT_ISNS 96
PPBUS_AON_BKLT_ISNS 96
PPBUS_AON_BKLT_ISNS 123

5V S2 VR HIGH SIDE SENSE RESISTOR

57 PPBUS_AON_5VS2_VIN_ISNS

PPBUS_AON_5VS2_VIN_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPBUS_AON_5VS2_VIN_ISNS 49
PPBUS_AON_5VS2_VIN_ISNS 123

USB PORT 5V HIGH SIDE SENSE RESISTOR

57 PPBUS_AON_PORT5V_VIN_ISNS

PPBUS_AON_PORT5V_VIN_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPBUS_AON_PORT5V_VIN_ISNS 123
PPBUS_AON_PORT5V_VIN_ISNS 75

ATC VR HIGH SIDE SENSE RESISTOR

58 PP3V8_AON_ATC_ISNS

PP3V8_AON_ATC_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V8_AON_ATC_ISNS 76
PP3V8_AON_ATC_ISNS 76
PP3V8_AON_ATC_ISNS 76
PP3V8_AON_ATC_ISNS 76

MESA HIGH SIDE SENSE RESISTOR

58 PP3V8_MESA_ISNS

PP3V8_MESA_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V8_MESA_ISNS 112

SD 3V3 HIGH SIDE SENSE RESISTOR

58 PPBUS_AON_SD_ISNS

PPBUS_AON_SD_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPBUS_AON_SD_ISNS 86

LEFT AMP PBUS SENSE RESISTOR

59 PPBUS_SPKRAMP_LEFT_ISNS

PPBUS_SPKRAMP_LEFT_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPBUS_SPKRAMP_LEFT_ISNS 102 104
PPBUS_SPKRAMP_LEFT_ISNS 102
PPBUS_SPKRAMP_LEFT_ISNS 102

RIGHT AMP PBUS SENSE RESISTOR

59 PPBUS_SPKRAMP_RIGHT_ISNS

PPBUS_SPKRAMP_RIGHT_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPBUS_SPKRAMP_RIGHT_ISNS 103 104
PPBUS_SPKRAMP_RIGHT_ISNS 103
PPBUS_SPKRAMP_RIGHT_ISNS 103

LEFT AMP 3V8 SENSE RESISTOR

58 PP3V8_AON_SPKRAMP_LEFT_ISNS

PP3V8_AON_SPKRAMP_LEFT_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V8_AON_SPKRAMP_LEFT_ISNS 102
PP3V8_AON_SPKRAMP_LEFT_ISNS 102
PP3V8_AON_SPKRAMP_LEFT_ISNS 102

RIGHT AMP 3V8 SENSE RESISTOR

58 PP3V8_AON_SPKRAMP_RIGHT_ISNS

PP3V8_AON_SPKRAMP_RIGHT_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V8_AON_SPKRAMP_RIGHT_ISNS 103
PP3V8_AON_SPKRAMP_RIGHT_ISNS 103
PP3V8_AON_SPKRAMP_RIGHT_ISNS 103

USB2 LEVEL SHIFTER 3.3V SENSE RESISTOR

59 PP3V3_S2SW_USBLS1_ISNS

NRC

PP3V3_S2SW_USBLS1_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V3_S2SW_USBLS1_ISNS 73

USB2 LEVEL SHIFTER 1.8V SENSE RESISTOR

59 PP1V8_S2_USBLS1_ISNS

PP1V8_S2_USBLS1_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V8_S2_USBLS1_ISNS 73

KBD 3.3V LOAD SIDE SENSE RESISTOR

60 PP3V3_S2_HOLD_KBD_ISNS

PP3V3_S2_HOLD_KBD_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V3_S2_HOLD_KBD_ISNS 107
PP3V3_S2_HOLD_KBD_ISNS 107

1V825 KBD LOAD SIDE SENSE RESISTOR

60 PP1V825_S2_HOLD_KBD_ISNS

PP1V825_S2_HOLD_KBD_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.825V

PP1V825_S2_HOLD_KBD_ISNS 107 108

KEYBOARD LED, TOUCHID 5V SENSE RESISTOR

59 PP5V_S2_HOLD_KBDLED_ISNS

PP5V_S2_HOLD_KBDLED_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP5V_S2_HOLD_KBDLED_ISNS 106 123
PP5V_S2_HOLD_KBDLED_ISNS 106

TPAD 5V SENSE RESISTOR

60 PP5V_S2_HOLD_TPAD_ISNS

PP5V_S2_HOLD_TPAD_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP5V_S2_HOLD_TPAD_ISNS 110

TPAD 3.3V SENSE RESISTOR

60 PP3V3_S2_HOLD_TPAD_ISNS

PP3V3_S2_HOLD_TPAD_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V3_S2_HOLD_TPAD_ISNS 110
PP3V3_S2_HOLD_TPAD_ISNS 55
PP3V3_S2_HOLD_TPAD_ISNS 109

3V8 WLANBT LOAD SIDE SENSE RESISTOR

59 PP3V8_AON_WLBT_ISNS

PP3V8_AON_WLBT_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V8_AON_WLBT_ISNS 87 123

WIFI/BT 1.8V SENSE RESISTOR

59 PP1V8_S2_WLBT_ISNS

PP1V8_S2_WLBT_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V8_S2_WLBT_ISNS 87 123

5V ALSCAM LOAD SIDE SENSE RESISTOR

60 PP5V_S2_HOLD_ALSCAM_ISNS

PP5V_S2_HOLD_ALSCAM_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP5V_S2_HOLD_ALSCAM_ISNS 92

3V8 TCON LOAD SIDE SENSE RESISTOR

60 PP3V8_AWAKESW_TCON_ISNS

PP3V8_AWAKESW_TCON_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V8_AWAKESW_TCON_ISNS 94

3V29 BKLT LOAD SIDE SENSE RESISTOR

60 PP3V29_AWAKESW_BCON_ISNS

PP3V29_AWAKESW_BCON_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V29_AWAKESW_BCON_ISNS 97 113

3V8 HDMI HIGH SIDE SENSE RESISTOR

59 PP3V8_AON_HDMI_ISNS

PP3V8_AON_HDMI_ISNS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V8_AON_HDMI_ISNS 82
PP3V8_AON_HDMI_ISNS 82

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ALIASES POWER (5/5)

Apple Inc.

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REVISION 6.0.0
BRANCH dvt-1
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RT13 REF DESIGN

67	SWD_NUB_ATCRTMR_SWCLK	—	SWD_NUB_ATCRTMR_SWCLK		15 130
			MAKE_BASE=TRUE		
68	SWD_NUB_ATCRTMR_SWCLK	—	SWD_NUB_ATCRTMR_SWCLK		15 130
			MAKE_BASE=TRUE		
67	SWD_NUB_ATCRTMR_SWDIO	—	SWD_NUB_ATCRTMR_SWDIO		15 130
			MAKE_BASE=TRUE		
68	SWD_NUB_ATCRTMR_SWDIO	—	SWD_NUB_ATCRTMR_SWDIO		15 130
			MAKE_BASE=TRUE		
73	EUSB_ATC0_P	—	EUSB_ATC0_P		12 16 139
			MAKE_BASE=TRUE		
73	EUSB_ATC0_N	—	EUSB_ATC0_N		12 16 139
			MAKE_BASE=TRUE		
73	EUSB_ATC1_P	—	EUSB_ATC1_P		12 16 139
			MAKE_BASE=TRUE		
73	EUSB_ATC1_N	—	EUSB_ATC1_N		12 16 139
			MAKE_BASE=TRUE		
139 12	CIO_ATC0_LSRX	—	CIO_ATC0_LSRX		67 139
			MAKE_BASE=TRUE		
139 12	CIO_ATC0_LSTX	—	CIO_ATC0_LSTX		67 139
			MAKE_BASE=TRUE		
139 12	CIO_ATC1_LSRX	—	CIO_ATC1_LSRX		68 139
			MAKE_BASE=TRUE		
139 12	CIO_ATC1_LSTX	—	CIO_ATC1_LSTX		68 139
			MAKE_BASE=TRUE		
73	ATCRTMR0_RESET_1V2_L	—	ATCRTMR0_RESET_1V2_L		67 74 113
			MAKE_BASE=TRUE		
73	SOC_DOCK_CONNECT	—	SOC_DOCK_CONNECT		6 113 132
			MAKE_BASE=TRUE		
73	USB2_ATC0_LS_P	—	USB2_ATC0_LS_P		77 113
			MAKE_BASE=TRUE		
73	USB2_ATC0_LS_N	—	USB2_ATC0_LS_N		77 113
			MAKE_BASE=TRUE		
73	USB2_ATC1_LS_P	—	USB2_ATC1_LS_P		77
			MAKE_BASE=TRUE		
73	USB2_ATC1_LS_N	—	USB2_ATC1_LS_N		77
			MAKE_BASE=TRUE		
67	GND	—	GND		
			MAKE_BASE=TRUE		
68	GND	—	GND		
			MAKE_BASE=TRUE		
77 67	TST_ATCRTMR0_JTAG_TDI	—	TST_ATCRTMR0_JTAG_TDI		
			MAKE_BASE=TRUE		
77 67	TST_ATCRTMR0_ANALOGMUX_OUT	—	TST_ATCRTMR0_ANALOGMUX_OUT		
			MAKE_BASE=TRUE		
77 67	TST_ATCRTMR0_JTAG_TRESET	—	TST_ATCRTMR0_JTAG_TRESET		
			MAKE_BASE=TRUE		
67	NC_ATCRTMR0_GPIO0	—	NC_ATCRTMR0_GPIO0		
			MAKE_BASE=TRUE		
67	NC_ATCRTMR0_GPIO2	—	NC_ATCRTMR0_GPIO2		
			MAKE_BASE=TRUE		
67	NC_ATCRTMR0_GPIO3	—	NC_ATCRTMR0_GPIO3		
			MAKE_BASE=TRUE		
67	NC_ATCRTMR0_TST_CLKOUT	—	NC_ATCRTMR0_TST_CLKOUT		
			MAKE_BASE=TRUE		
77 68	NC_ATCRTMR1_JTAG_TDI	—	NC_ATCRTMR1_JTAG_TDI		
			MAKE_BASE=TRUE		
77 68	NC_ATCRTMR1_ANALOGMUX_OUT	—	NC_ATCRTMR1_ANALOGMUX_OUT		
			MAKE_BASE=TRUE		
77 68	NC_ATCRTMR1_JTAG_TRESET	—	NC_ATCRTMR1_JTAG_TRESET		
			MAKE_BASE=TRUE		
68	NC_ATCRTMR1_GPIO0	—	NC_ATCRTMR1_GPIO0		
			MAKE_BASE=TRUE		
68	NC_ATCRTMR1_GPIO2	—	NC_ATCRTMR1_GPIO2		
			MAKE_BASE=TRUE		
68	NC_ATCRTMR1_GPIO3	—	NC_ATCRTMR1_GPIO3		
			MAKE_BASE=TRUE		
68	NC_ATCRTMR1_TST_CLKOUT	—	NC_ATCRTMR1_TST_CLKOUT		
			MAKE_BASE=TRUE		
73	EUSB_ATC1_DBG_P	—	EUSB_ATC1_DBG_P		73
			MAKE_BASE=TRUE		
73	EUSB_ATC1_DBG_N	—	EUSB_ATC1_DBG_N		73
			MAKE_BASE=TRUE		
71	USB_ATC0_DBG_LS_P	—	USB_ATC0_DBG_LS_P		113
			MAKE_BASE=TRUE		
73	USB_ATC0_DBG_LS_P	—			
71	USB_ATC0_DBG_LS_N	—	USB_ATC0_DBG_LS_N		113
			MAKE_BASE=TRUE		
73	USB_ATC0_DBG_LS_N	—			
72 70	USB_ATC1_DBG_LS_P	—	USB_ATC1_DBG_LS_P		130
			MAKE_BASE=TRUE		
72 70	USB_ATC1_DBG_LS_N	—	USB_ATC1_DBG_LS_N		130
			MAKE_BASE=TRUE		
73 70	USB_ATC1_DBG_LS_P	—	USB_ATC1_DBG_LS_P		130
			MAKE_BASE=TRUE		
73 70	USB_ATC1_DBG_LS_N	—	USB_ATC1_DBG_LS_N		130
			MAKE_BASE=TRUE		
72 71	UPC_PMU_RESET_1V2_ACE2	—	UPC_PMU_RESET_1V2_ACE2		114 116 130
			MAKE_BASE=TRUE		
71 70	UPC01_5V_EN	—	UPC01_5V_EN		75 130
			MAKE_BASE=TRUE		
72 70	UPC01_5V_EN	—	UPC01_5V_EN		75 130
			MAKE_BASE=TRUE		
73	TST_MACAW0_DEBUG_SWDCLK	—	TST_MACAW0_DEBUG_SWDCLK		77
			MAKE_BASE=TRUE		
73	TST_MACAW0_DEBUG_SWDDAT	—	TST_MACAW0_DEBUG_SWDDAT		77
			MAKE_BASE=TRUE		
73	TST_MACAW1_DEBUG_SWDCLK	—	TST_MACAW1_DEBUG_SWDCLK		77
			MAKE_BASE=TRUE		
73	TST_MACAW1_DEBUG_SWDDAT	—	TST_MACAW1_DEBUG_SWDDAT		77
			MAKE_BASE=TRUE		

GL9755 REF DESIGN

83	PCIE_SD_R2D_C_P	—	PCIE_SD_R2D_C_P		138
			MAKE_BASE=TRUE		
83	PCIE_SD_R2D_C_N	—	PCIE_SD_R2D_C_N		138
			MAKE_BASE=TRUE		
83	PCIE_SD_D2R_P	—	PCIE_SD_D2R_P		138
			MAKE_BASE=TRUE		
83	PCIE_SD_D2R_N	—	PCIE_SD_D2R_N		138
			MAKE_BASE=TRUE		
85	SD_CLKREQ_L	—	SD_CLKREQ_L		138
			MAKE_BASE=TRUE		
85	SD_RESET_L	—	SD_RESET_L		138
			MAKE_BASE=TRUE		
83	PCIE_CLK100M_SD_P	—	PCIE_CLK100M_SD_P		138
			MAKE_BASE=TRUE		
83	PCIE_CLK100M_SD_N	—	PCIE_CLK100M_SD_N		138
			MAKE_BASE=TRUE		

LUXE REF DESIGN

113 97	DISP_BKLT_FSYNC	—	DISP_BKLT_FSYNC		10 113 137
			MAKE_BASE=TRUE		
96	PP5V_S2_HOLD_LUXE_VDDA	—	PP5V_S2_HOLD_LUXE_VDDA		
			MAKE_BASE=TRUE		

STOWE AND VALE REF DESIGN

39	SWD_NUB_SWCLK_SPMU	—	SWD_NUB_SWCLK_SPMU		15
			MAKE_BASE=TRUE		
39	SWD_NUB_SWDIO_SPMU	—	SWD_NUB_SWDIO_SPMU		15
			MAKE_BASE=TRUE		
45	SWD_NUB_SWCLK_MPMU	—	SWD_NUB_SWCLK_MPMU		15
			MAKE_BASE=TRUE		
45	SWD_NUB_SWDIO_MPMU	—	SWD_NUB_SWDIO_MPMU		15
			MAKE_BASE=TRUE		
47	UPC_PMU_RESET_1V2_ACE2	—	UPC_PMU_RESET_1V2_ACE2		114 116 130
			MAKE_BASE=TRUE		
44	PMU_CLK32K_WLBT	—	PMU_CLK32K_WLBT		87 88 114
			MAKE_BASE=TRUE		

WHAMOLA MP REF DESIGN

30	P5VS2HOLD_PWR_EN	—	P5VS2HOLD_PWR_EN		36 46 131
			MAKE_BASE=TRUE		
29	CHGR_AUX_OK	—	CHGR_AUX_OK		46 113
			MAKE_BASE=TRUE		
30	P5VS2HOLD_PGOOD	—	P5VS2HOLD_PGOOD		131
			MAKE_BASE=TRUE		

SECDIS AND LAS REF DESIGN

99	AMR1_OR_ND_1V8	—	AMR1_OR_ND_1V8		130
			MAKE_BASE=TRUE		
99	AMR1_OR_ND_1V8	—	AMR1_OR_ND_1V8		130
			MAKE_BASE=TRUE		
114 98	AMR1_OR_ND_1V8	—	AMR1_OR_ND_1V8		130
			MAKE_BASE=TRUE		
114 98	AMR1_OR_ND_1V8	—	AMR1_OR_ND_1V8		130
			MAKE_BASE=TRUE		

5V PORT POWER LT8642-1 REF DESIGN

75	PMU_SYS_ALIVE_1V8	—	PMU_SYS_ALIVE_1V8		47 81 95
			MAKE_BASE=TRUE		
75	PP5VUSBC01_DSCHG	—	PP5VUSBC01_DSCHG		
			MAKE_BASE=TRUE		

S5E REF DESIGN

90	TP_NAND0_S5E1_JTAG_TDO	—	TP_NAND0_S5E1_JTAG_TDO		91
			MAKE_BASE=TRUE		
89	NAND0_RESET0_L	—	NAND0_RESET0_L		91 134
			MAKE_BASE=TRUE		
90	NAND0_RESET1_L	—	NAND0_RESET1_L		91 134
			MAKE_BASE=TRUE		

MAGSAFE 20V REF DESIGN

77 32	UPC5_CHGR_AUX_DET_SHORT	—	UPC5_CHGR_AUX_DET_SHORT		
			MAKE_BASE=TRUE		
32	TST_UPC5_SER_DBG	—	TST_UPC5_SER_DBG		
			MAKE_BASE=TRUE		
32	UPC_I2C_INT_L	—	UPC_I2C_INT_L		7 52 134
			MAKE_BASE=TRUE		
33 32	PPHV_INT5_AONSW	—	PPHV_INT5_AONSW		113 130
			MAKE_BASE=TRUE		
32	PPHV_INT5_AONSW	—	PPHV_INT5_AONSW		113 130
			MAKE_BASE=TRUE		
32	PPVBUS_USBC5	—	PPVBUS_USBC5		31 32 113
			MAKE_BASE=TRUE		

EOS REF DESIGN

27	SE_NFC_GPIO0	—	SE_NFC_GPIO0		117
			MAKE_BASE=TRUE		
27	SE_NFC_GPIO1	—	SE_NFC_GPIO1		117
			MAKE_BASE=TRUE		
27	SE_IRQ_WAKE	—	SE_IRQ_WAKE		7 117 133
			MAKE_BASE=TRUE		
27	I2C_SE_SCL	—	I2C_SE_SCL		117
			MAKE_BASE=TRUE		
27	I2C_SE_SDA	—	I2C_SE_SDA		117
			MAKE_BASE=TRUE		
27	I3C_SE_SCL	—	I3C_SE_SCL		117
			MAKE_BASE=TRUE		
27	I3C_SE_SDA	—	I3C_SE_SDA		117
			MAKE_BASE=TRUE		
27	SE_GPIO0	—	SE_GPIO0		117
			MAKE_BASE=TRUE		
27	SE_GPIO1	—	SE_GPIO1		117
			MAKE_BASE=TRUE		
27	I3C_SE_NFC_SCL	—	I3C_SE_NFC_SCL		117
			MAKE_BASE=TRUE		
27	I3C_SE_NFC_SDA	—	I3C_SE_NFC_SDA		117
			MAKE_BASE=TRUE		
27	NC_SE_K1	—	NC_SE_K1		
			MAKE_BASE=TRUE		
27	NC_SE_K8	—	NC_SE_K8		
			MAKE_BASE=TRUE		

COBRA REF DESIGN

80	LPDP_DP2HDMI_HPD	—	LPDP_DP2HDMI_HPD		10 16 117 137
			MAKE_BASE=TRUE		
80	I2C_HDMI_SPKRAMP_R_SCL	—	I2C_HDMI_SPKRAMP_R_SCL		53 117 135
			MAKE_BASE=TRUE		
80	I2C_HDMI_SPKRAMP_R_SDA	—	I2C_HDMI_SPKRAMP_R_SDA		53 117 135
			MAKE_BASE=TRUE		
81	LPDP_DP2HDMI_DATA_C_P<0>	—	LPDP_DP2HDMI_DATA_C_P<0>		10 137
			MAKE_BASE=TRUE		
81	LPDP_DP2HDMI_DATA_C_N<0>	—	LPDP_DP2HDMI_DATA_C_N<0>		10 137
			MAKE_BASE=TRUE		
81	LPDP_DP2HDMI_DATA_C_P<1>	—	LPDP_DP2HDMI_DATA_C_P<1>		10 137
			MAKE_BASE=TRUE		
81	LPDP_DP2HDMI_DATA_C_N<1>	—	LPDP_DP2HDMI_DATA_C_N<1>		10 137
			MAKE_BASE=TRUE		
81	LPDP_DP2HDMI_DATA_C_P<2>	—	LPDP_DP2HDMI_DATA_C_P<2>		10 137
			MAKE_BASE=TRUE		
81	LPDP_DP2HDMI_DATA_C_N<2>	—	LPDP_DP2HDMI_DATA_C_N<2>		10 137
			MAKE_BASE=TRUE		
81	LPDP_DP2HDMI_DATA_C_P<3>	—	LPDP_DP2HDMI_DATA_C_P<3>		10 137
			MAKE_BASE=TRUE		
81	LPDP_DP2HDMI_DATA_C_N<3>	—	LPDP_DP2HDMI_DATA_C_N<3>		10 137
			MAKE_BASE=TRUE		
81	LPDP_DP2HDMI_AUX_C_P	—	LPDP_DP2HDMI_AUX_C_P		10 137
			MAKE_BASE=TRUE		
81	LPDP_DP2HDMI_AUX_C_N	—	LPDP_DP2HDMI_AUX_C_N		10 137
			MAKE_BASE=TRUE		
81	NC_UH805_6	—	NC_UH805_6		
			MAKE_BASE=TRUE		
80	NC_COBRA_VDD09_ON	—	NC_COBRA_VDD09_ON		
			MAKE_BASE=TRUE		
82 81	PP5V_S2_HOLD_HDMI_LDO	—	PP5V_S2_HOLD_HDMI_LDO		
			MAKE_BASE=TRUE		
82 78	PP5V_S2_HOLD_HDMI	—	PP5V_S2_HOLD_HDMI		130
			MAKE_BASE=TRUE		
82	PP5V_S2_HOLD_HDMI	—	PP5V_S2_HOLD_HDMI		130
			MAKE_BASE=TRUE		
130 81	NC_UH805_5	—	NC_UH805_5		81 130
			MAKE_BASE=TRUE		
130 81	NC_UH805_11	—	NC_UH805_11		81 130
			MAKE_BASE=TRUE		
82 81	DP2HDMI_PWR_EN_PMU	—	DP2HDMI_PWR_EN_PMU		46
			MAKE_BASE=TRUE		
80	NC_HDMI_CEC_IRQ	—	NC_HDMI_CEC_IRQ		
			MAKE_BASE=TRUE		

BOM_COST_GROUP=PLATFORM POWER

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SPEAKER AMP REF DESIGN

115 102	TDM_SPKRAMP_L_BCLK	—	TDM_SPKRAMP_L_BCLK	MAKE_BASE=TRUE	14 131
102	TDM_SPKRAMP_L_BCLK	—	TDM_SPKRAMP_L_BCLK	MAKE_BASE=TRUE	14 131
102	TDM_SPKRAMP_L_BCLK	—	TDM_SPKRAMP_L_BCLK	MAKE_BASE=TRUE	14 131
115 102	TDM_SPKRAMP_L_R2D	—	TDM_SPKRAMP_L_R2D	MAKE_BASE=TRUE	14 131
102	TDM_SPKRAMP_L_R2D	—	TDM_SPKRAMP_L_R2D	MAKE_BASE=TRUE	14 131
102	TDM_SPKRAMP_L_R2D	—	TDM_SPKRAMP_L_R2D	MAKE_BASE=TRUE	14 131
115 102	TDM_SPKRAMP_L_FSYNC	—	TDM_SPKRAMP_L_FSYNC	MAKE_BASE=TRUE	14 131
102	TDM_SPKRAMP_L_FSYNC	—	TDM_SPKRAMP_L_FSYNC	MAKE_BASE=TRUE	14 131
102	TDM_SPKRAMP_L_FSYNC	—	TDM_SPKRAMP_L_FSYNC	MAKE_BASE=TRUE	14 131
115 102	TDM_SPKRAMP_L_D2R	—	TDM_SPKRAMP_L_D2R	MAKE_BASE=TRUE	8 131 135
102	TDM_SPKRAMP_L_D2R	—	TDM_SPKRAMP_L_D2R	MAKE_BASE=TRUE	8 131 135
102	TDM_SPKRAMP_L_D2R	—	TDM_SPKRAMP_L_D2R	MAKE_BASE=TRUE	8 131 135
115 103	TDM_SPKRAMP_R_BCLK	—	TDM_SPKRAMP_R_BCLK	MAKE_BASE=TRUE	14 131
103	TDM_SPKRAMP_R_BCLK	—	TDM_SPKRAMP_R_BCLK	MAKE_BASE=TRUE	14 131
103	TDM_SPKRAMP_R_BCLK	—	TDM_SPKRAMP_R_BCLK	MAKE_BASE=TRUE	14 131
115 103	TDM_SPKRAMP_R_R2D	—	TDM_SPKRAMP_R_R2D	MAKE_BASE=TRUE	14 131
103	TDM_SPKRAMP_R_R2D	—	TDM_SPKRAMP_R_R2D	MAKE_BASE=TRUE	14 131
103	TDM_SPKRAMP_R_R2D	—	TDM_SPKRAMP_R_R2D	MAKE_BASE=TRUE	14 131
115 103	TDM_SPKRAMP_R_FSYNC	—	TDM_SPKRAMP_R_FSYNC	MAKE_BASE=TRUE	14 131
103	TDM_SPKRAMP_R_FSYNC	—	TDM_SPKRAMP_R_FSYNC	MAKE_BASE=TRUE	14 131
103	TDM_SPKRAMP_R_FSYNC	—	TDM_SPKRAMP_R_FSYNC	MAKE_BASE=TRUE	14 131
115 103	TDM_SPKRAMP_R_D2R	—	TDM_SPKRAMP_R_D2R	MAKE_BASE=TRUE	8 131 135
103	TDM_SPKRAMP_R_D2R	—	TDM_SPKRAMP_R_D2R	MAKE_BASE=TRUE	8 131 135
103	TDM_SPKRAMP_R_D2R	—	TDM_SPKRAMP_R_D2R	MAKE_BASE=TRUE	8 131 135

MAGSAFE REF DESIGN

32	NC_MAGSAFE_ACE_DEB_CON_10	—	NC_MAGSAFE_ACE_DEB_CON_10	MAKE_BASE=TRUE	
15	SWD_UPC_SWDIO2	—	SWD_UPC_SWDIO2	MAKE_BASE=TRUE	16 32

5V S2 VR REF DESIGN

49	P5VS2HOLD_PWR_EN	—	P5VS2HOLD_PWR_EN	MAKE_BASE=TRUE	36 46 130 131
49	P5VS2HOLD_PGOOD	—	P5VS2HOLD_PGOOD	MAKE_BASE=TRUE	130
49	P5VS2HOLD_DSCHG	—	P5VS2HOLD_DSCHG	MAKE_BASE=TRUE	
113 110 82 49	P5VS2HOLD_PWR_EN	—	P5VS2HOLD_PWR_EN	MAKE_BASE=TRUE	36 46 130 131

ICEMAN REF DESIGN

34	GND	—	GND	MAKE_BASE=TRUE	
34	GND	—	GND	MAKE_BASE=TRUE	

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MTR TD (METROLOGY)

6	NC_SOC_MTR_TD_B	NC_SOC_MTR_TD_B	MAKE_BASE=TRUE
6	NC_SOC_MTR_TD_BS	NC_SOC_MTR_TD_BS	MAKE_BASE=TRUE
6	NC_SOC_MTR_TD_E	NC_SOC_MTR_TD_E	MAKE_BASE=TRUE
6	NC_SOC_MTR_TD_ES	NC_SOC_MTR_TD_ES	MAKE_BASE=TRUE
6	NC_SOC_MTR_TD_ESD	NC_SOC_MTR_TD_ESD	MAKE_BASE=TRUE

EUSB DBG

6	EUSB_DBG_P	EUSB_DBG_P	MAKE_BASE=TRUE	16 73
6	EUSB_DBG_N	EUSB_DBG_N	MAKE_BASE=TRUE	16 73

MISC

132 6 4	SOC_UNTRUSTED_BOOTCONFIG	SOC_UNTRUSTED_BOOTCONFIG	MAKE_BASE=TRUE	4 6 132
132 117 6	SOC_DOCK_ATTENTION	SOC_DOCK_ATTENTION	MAKE_BASE=TRUE	6 117 132
132 130 113 6	SOC_DOCK_CONNECT	SOC_DOCK_CONNECT	MAKE_BASE=TRUE	6 113 130 132
132 116 113 70 48 6	SOC_FORCE_DFU	SOC_FORCE_DFU	MAKE_BASE=TRUE	6 48 70 113 116 132
132 119 113 70 6	SOC_DFU_STATUS	SOC_DFU_STATUS	MAKE_BASE=TRUE	6 70 113 119 132
132 113 6	SOC_KIS_DFU_SELECT	SOC_KIS_DFU_SELECT	MAKE_BASE=TRUE	6 113 132

SWD

6	SWD_NAND0_SWCLK_R	SWD_NAND0_SWCLK_R	MAKE_BASE=TRUE	15
132 15 6	SWD_NAND0_SWDIO_R	SWD_NAND0_SWDIO_R	MAKE_BASE=TRUE	6 15 132
6	NC_SOC_SWD_TMS5	NC_SOC_SWD_TMS5	MAKE_BASE=TRUE	
6	NC_SOC_SWD_TMS6	NC_SOC_SWD_TMS6	MAKE_BASE=TRUE	

JTAG

6	TP_SOC_TST_ANALOGMUX_POS	TP_SOC_TST_ANALOGMUX_POS	MAKE_BASE=TRUE	117
6	TP_SOC_TST_ANALOGMUX_NEG	TP_SOC_TST_ANALOGMUX_NEG	MAKE_BASE=TRUE	117
132 14 6	SWD_SOC_SWCLK_R	SWD_SOC_SWCLK_R	MAKE_BASE=TRUE	6 14 132
132 117 6	TP_JTAG_SOC_TDI	TP_JTAG_SOC_TDI	MAKE_BASE=TRUE	6 117 132
132 117 6	TP_JTAG_SOC_TDO	TP_JTAG_SOC_TDO	MAKE_BASE=TRUE	6 117 132
132 14 6	SWD_SOC_SWDIO_R	SWD_SOC_SWDIO_R	MAKE_BASE=TRUE	6 14 132
132 117 6	TP_JTAG_SOC_TRST_L	TP_JTAG_SOC_TRST_L	MAKE_BASE=TRUE	6 117 132
132 6	SOC_JTAG_SEL	SOC_JTAG_SEL	MAKE_BASE=TRUE	6 132

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AOP GPIO

	7	NC_PDM_DMIC_DATA2	NC_PDM_DMIC_DATA2	
	7	NC_UWB_CS_L	NC_UWB_CS_L	
	7	NC_UWB_DUMP_TRIG	NC_UWB_DUMP_TRIG	
	7	NC_UWB_HOST_WAKE	NC_UWB_HOST_WAKE	
	7	AOP_LEAP_MADI_IN	AOP_LEAP_MADI_IN	117
	7	AOP_LEAP_MADI_OUT	AOP_LEAP_MADI_OUT	117
133 64	7	SPI_GYRO_CS_L	SPI_GYRO_CS_L	7 64 133
133 64	7	GYRO_INT	GYRO_INT	7 64 133
133 64	7	GYRO_MOTION_INT	GYRO_MOTION_INT	7 64 133
133 81	7	HDMI_CEC_AOP_TX	HDMI_CEC_AOP_TX	7 81 133
133 81	7	HDMI_CEC_AOP_RX	HDMI_CEC_AOP_RX	7 81 133
133 114 92	7	ALS_INT_L	ALS_INT_L	7 92 114 133
133 81	7	SPI_DP2HDMI_HOLD_L	SPI_DP2HDMI_HOLD_L	7 81 133
133 100	7	SPI_LAS_CS_L	SPI_LAS_CS_L	7 100 133
133 81	7	HDMI_HPD_AOP	HDMI_HPD_AOP	7 81 133
133 130 117	7	SE_IRQ_WAKE	SE_IRQ_WAKE	7 117 130 133

AOP I2C

133 56	7	I2C_AOP_ALS_SCL	I2C_AOP_ALS_SCL	7 56 133
133 56	7	I2C_AOP_ALS_SDA	I2C_AOP_ALS_SDA	7 56 133
	7	NC_SOC_AOP_I2CM1_SCL	NC_SOC_AOP_I2CM1_SCL	
	7	NC_SOC_AOP_I2CM1_SDA	NC_SOC_AOP_I2CM1_SDA	
	7	NC_SOC_AOP_I2CM2_SCL	NC_SOC_AOP_I2CM2_SCL	
	7	NC_SOC_AOP_I2CM2_SDA	NC_SOC_AOP_I2CM2_SDA	

AOP I2S

	7	NC_AOP_I2S0_BCLK	NC_AOP_I2S0_BCLK	
	7	NC_AOP_I2S0_DIN	NC_AOP_I2S0_DIN	
	7	NC_AOP_I2S0_DOUT	NC_AOP_I2S0_DOUT	
	7	NC_AOP_I2S0_LRCK	NC_AOP_I2S0_LRCK	
	7	NC_AOP_I2S0_MCK	NC_AOP_I2S0_MCK	
133 14	7	PDM_DMIC_CLK5_R	PDM_DMIC_CLK5_R	7 14 133
133 14	7	PDM_DMIC_DATA1	PDM_DMIC_DATA1	7 14 133
133 14	7	PDM_DMIC_CLK6_R	PDM_DMIC_CLK6_R	7 14 133
	7	NC_PDM_DMIC_CLK7_R	NC_PDM_DMIC_CLK7_R	
133 14	7	PDM_DMIC_DATA0	PDM_DMIC_DATA0	7 14 133

AOP SPI

133 64	7	SPI_AOP_GYRO_MISO	SPI_AOP_GYRO_MISO	7 64 133
133 14	7	SPI_AOP_GYRO_MOSI_R	SPI_AOP_GYRO_MOSI_R	7 14 133
133 14	7	SPI_AOP_GYRO_CLK_R	SPI_AOP_GYRO_CLK_R	7 14 133
133 100	7	SPI_AOP_SENSORS_MISO	SPI_AOP_SENSORS_MISO	7 100 133
133 14	7	SPI_AOP_SENSORS_MOSI_R	SPI_AOP_SENSORS_MOSI_R	7 14 133
133 14	7	SPI_AOP_SENSORS_CLK_R	SPI_AOP_SENSORS_CLK_R	7 14 133

AOP SPMI

133 15	7	SPMI_AOP_WLBT_CLK_R	SPMI_AOP_WLBT_CLK_R	7 15 133
133 15	7	SPMI_AOP_WLBT_DATA_R	SPMI_AOP_WLBT_DATA_R	7 15 133
133 15	7	SPMI_AOP_SE_CLK_R	SPMI_AOP_SE_CLK_R	7 15 133
133 15	7	SPMI_AOP_SE_DATA_R	SPMI_AOP_SE_DATA_R	7 15 133

AOP UART

	7	NC_SOC_AOP_UART0_RXD	NC_SOC_AOP_UART0_RXD	
	7	NC_SOC_AOP_UART0_TXD	NC_SOC_AOP_UART0_TXD	
	7	NC_SOC_AOP_UART1_RXD	NC_SOC_AOP_UART1_RXD	
	7	NC_SOC_AOP_UART1_TXD	NC_SOC_AOP_UART1_TXD	
	7	NC_SOC_AOP_UART2_RXD	NC_SOC_AOP_UART2_RXD	
	7	NC_SOC_AOP_UART2_TXD	NC_SOC_AOP_UART2_TXD	

MIC

133 114 99	7	DMIC_DISABLE_L	DMIC_DISABLE_L	7 99 114 133
133 114 99	7	DMIC_DISABLE_WARN_L	DMIC_DISABLE_WARN_L	7 99 114 133

NUB CLK

	7	NC_SOC_NUB_CLK_OUT_0	NC_SOC_NUB_CLK_OUT_0	
133 16	7	TP_SOC_NUB_CLK_OUT_1	TP_SOC_NUB_CLK_OUT_1	7 16 133

NUB GPIO

	7	NC_BKLT_PWR_ON	NC_BKLT_PWR_ON	
133 115 101	7	CODEC_RESET_L	CODEC_RESET_L	7 101 115 133
	7	NC_SOC_NUB_GPIO_2	NC_SOC_NUB_GPIO_2	
	7	NC_SOC_NUB_GPIO_3	NC_SOC_NUB_GPIO_3	
	7	NC_SOC_NUB_GPIO_4	NC_SOC_NUB_GPIO_4	
	7	NC_SOC_NUB_GPIO_5	NC_SOC_NUB_GPIO_5	
133 113 30	7	CHGR_INT_L	CHGR_INT_L	7 30 113 133
133 113	7	SMC_FIXTURE_MODE_L	SMC_FIXTURE_MODE_L	7 113 133
133 119	7	SOC_SW_DBG	SOC_SW_DBG	7 119 133
	7	NC_ENET_LOW_PWR	NC_ENET_LOW_PWR	
	7	NC_SOC_NUB_GPIO_10	NC_SOC_NUB_GPIO_10	
133 109	7	IPD_SYS_AWAKE	IPD_SYS_AWAKE	7 109 133
	7	NC_SOC_NUB_GPIO_12	NC_SOC_NUB_GPIO_12	
	7	NC_SOC_NUB_GPIO_13	NC_SOC_NUB_GPIO_13	
	7	NC_SOC_NUB_GPIO_14	NC_SOC_NUB_GPIO_14	
	7	NC_SOC_NUB_GPIO_15	NC_SOC_NUB_GPIO_15	

NUB SPMI

133 14	7	SPMI_NUB_MPMU_CLK_R	SPMI_NUB_MPMU_CLK_R	7 14 133
133 14	7	SPMI_NUB_MPMU_DATA_R	SPMI_NUB_MPMU_DATA_R	7 14 133
133 14	7	SPMI_NUB_SPMU_CLK_R	SPMI_NUB_SPMU_CLK_R	7 14 133
133 14	7	SPMI_NUB_SPMU_DATA_R	SPMI_NUB_SPMU_DATA_R	7 14 133
	7	NC_SOC_NUB_SPMI2_SCLK	NC_SOC_NUB_SPMI2_SCLK	
	7	NC_SOC_NUB_SPMI2_SDATA	NC_SOC_NUB_SPMI2_SDATA	

NUB SWD

133 15	7	SWD_NUB_PMU_SWCLK_R	SWD_NUB_PMU_SWCLK_R	7 15 133
133 15	7	SWD_IPD_SWCLK_R	SWD_IPD_SWCLK_R	7 15 133
133 15	7	SWD_NUB_ATCRTMR_SWCLK_R	SWD_NUB_ATCRTMR_SWCLK_R	7 15 133
133 15	7	SWD_NUB_PMU_SWDIO_R	SWD_NUB_PMU_SWDIO_R	7 15 133
		SWD_IPD_SWDIO_R	SWD_IPD_SWDIO_R	7 15
133 15	7	SWD_NUB_ATCRTMR_SWDIO_R	SWD_NUB_ATCRTMR_SWDIO_R	7 15 133
	7	NC_SOC_NUB_SWD_TMS3	NC_SOC_NUB_SWD_TMS3	

SMC I2C

133 113 54	7	I2C_SMC_UPC_SCL	I2C_SMC_UPC_SCL	7 54 113 133
133 113 54	7	I2C_SMC_UPC_SDA	I2C_SMC_UPC_SDA	7 54 113 133
133 117 54	7	I2C_SMC_PWR_SCL	I2C_SMC_PWR_SCL	7 54 117 133
133 117 54	7	I2C_SMC_PWR_SDA	I2C_SMC_PWR_SDA	7 54 117 133
133 54	7	I2C_SMC_SNS1_SCL	I2C_SMC_SNS1_SCL	7 54 133
133 54	7	I2C_SMC_SNS1_SDA	I2C_SMC_SNS1_SDA	7 54 133
133 55	7	I2C_SMC_IPD_SCL	I2C_SMC_IPD_SCL	7 55 133
133 55	7	I2C_SMC_IPD_SDA	I2C_SMC_IPD_SDA	7 55 133
133 55	7	I2C_SMC_SNS0_SCL	I2C_SMC_SNS0_SCL	7 55 133
133 55	7	I2C_SMC_SNS0_SDA	I2C_SMC_SNS0_SDA	7 55 133

SMC UART

	7	NC_SOC_UART_SMC_DEBUGPRT_D2R	NC_SOC_UART_SMC_DEBUGPRT_D2R	
	7	NC_SOC_UART_SMC_DEBUGPRT_R2D	NC_SOC_UART_SMC_DEBUGPRT_R2D	

SMC GPIO

133 54	7	UPC_SMC_I2C_INT_L	UPC_SMC_I2C_INT_L	7 54 133
	7	NC_SOC_SMC_GPIO_1	NC_SOC_SMC_GPIO_1	

SMC PWM

133 65	7	SMC_FAN_0_PWM	SMC_FAN_0_PWM	7 65 133
133 65	7	SMC_FAN_0_TACH	SMC_FAN_0_TACH	7 65 133
	7	NC_SMC_FAN_1_PWM	NC_SMC_FAN_1_PWM	
	7	NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	

MAKE_BASE=TRUE

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AP GPIO

134 130 52 7	UPC_I2C_INT_L	=	UPC_I2C_INT_L	7 52 130 134
7	NC_SOC_AP_GPIO_1	=	NC_SOC_AP_GPIO_1	
134 114 104 7	SPKR_ID0	=	SPKR_ID0	7 104 114 134
134 114 104 7	SPKR_ID1	=	SPKR_ID1	7 104 114 134
134 115 103 102 7	SPKRAMP_RESET_L	=	SPKRAMP_RESET_L	7 102 103 115 134
134 115 103 102 7	SPKRAMP_INT_L	=	SPKRAMP_INT_L	7 102 103 115 134
134 115 101 7	CODEC_INT_L	=	CODEC_INT_L	7 101 115 134
134 15 7	SWD_UPC_SWCLK_R	=	SWD_UPC_SWCLK_R	7 15 134
134 15 7	SWD_UPC_SWDIO0_R	=	SWD_UPC_SWDIO0_R	7 15 134
134 15 7	SWD_UPC_SWDIO1_R	=	SWD_UPC_SWDIO1_R	7 15 134
7	NC_CCG_I2C_INT	=	NC_CCG_I2C_INT	
134 7 4	BOARD_REV0	=	BOARD_REV0	4 7 134
134 7 4	BOARD_REV1	=	BOARD_REV1	4 7 134
134 7 4	BOARD_REV2	=	BOARD_REV2	4 7 134
134 7 4	BOARD_REV3	=	BOARD_REV3	4 7 134
7	NC_SD_PRSNT_L	=	NC_SD_PRSNT_L	
7	NC_SOC_AP_GPIO_16	=	NC_SOC_AP_GPIO_16	
7	NC_SOC_AP_GPIO_17	=	NC_SOC_AP_GPIO_17	
7	NC_SWD_UPC_SWDIO2_R	=	NC_SWD_UPC_SWDIO2_R	
7	NC_SOC_AP_GPIO_19	=	NC_SOC_AP_GPIO_19	
7	NC_SOC_AP_GPIO_20	=	NC_SOC_AP_GPIO_20	
134 112 7	TOUCHID_INT	=	TOUCHID_INT	7 112 134
134 114 112 16 7	TOUCHID_PWR_EN	=	TOUCHID_PWR_EN	7 16 112 114 134
7	NC_SOC_AP_GPIO_23	=	NC_SOC_AP_GPIO_23	
7	NC_SOC_AP_GPIO_24	=	NC_SOC_AP_GPIO_24	
7	NC_SOC_AP_GPIO_25	=	NC_SOC_AP_GPIO_25	
7	NC_SOC_AP_GPIO_26	=	NC_SOC_AP_GPIO_26	

BOARD ID

134 7 4	BOARD_ID0	=	BOARD_ID0	4 7 134
134 7 4	BOARD_ID1	=	BOARD_ID1	4 7 134
134 7 4	BOARD_ID2	=	BOARD_ID2	4 7 134
134 7 4	BOARD_ID3	=	BOARD_ID3	4 7 134
134 7 4	BOARD_ID4	=	BOARD_ID4	4 7 134

MTP FUNC

134 114 109 7	IPD_TOUCH_INT_L	=	IPD_TOUCH_INT_L	7 109 114 134
7	IPD_MTP_FUNC_1	=	IPD_MTP_FUNC_1	109
7	NC_SOC_MTP_FUNC_2	=	NC_SOC_MTP_FUNC_2	
134 109 7	SPI_IPD_MCU_CS_L	=	SPI_IPD_MCU_CS_L	7 109 134
134 109 7	SPI_IPD_TOUCH_CS_L	=	SPI_IPD_TOUCH_CS_L	7 109 134
134 114 109 7	IPD_MCU_INT_L	=	IPD_MCU_INT_L	7 109 114 134
7	NC_SOC_MTP_FUNC_6	=	NC_SOC_MTP_FUNC_6	
7	NC_SOC_MTP_FUNC_7	=	NC_SOC_MTP_FUNC_7	

AP UART

134 113 70 7	UART_DEBUGPRT_D2R	=	UART_DEBUGPRT_D2R	7 70 113 134
134 113 70 7	UART_DEBUGPRT_R2D	=	UART_DEBUGPRT_R2D	7 70 113 134
7	NC_SOC_AP_UART1_CTS_L	=	NC_SOC_AP_UART1_CTS_L	
7	NC_SOC_AP_UART1_RTS_L	=	NC_SOC_AP_UART1_RTS_L	
7	NC_SOC_AP_UART1_RXD	=	NC_SOC_AP_UART1_RXD	
7	NC_SOC_AP_UART1_TXD	=	NC_SOC_AP_UART1_TXD	
7	NC_UART_WLAN_D2R_CTS_L	=	NC_UART_WLAN_D2R_CTS_L	
7	NC_UART_WLAN_R2D_RTS_L	=	NC_UART_WLAN_R2D_RTS_L	
7	NC_UART_WLAN_D2R	=	NC_UART_WLAN_D2R	
7	NC_UART_WLAN_R2D	=	NC_UART_WLAN_R2D	
7	NC_SOC_AP_UART3_CTS_L	=	NC_SOC_AP_UART3_CTS_L	
7	NC_SOC_AP_UART3_RTS_L	=	NC_SOC_AP_UART3_RTS_L	
7	NC_SOC_AP_UART3_RXD	=	NC_SOC_AP_UART3_RXD	
7	NC_SOC_AP_UART3_TXD	=	NC_SOC_AP_UART3_TXD	
7	NC_SOC_AP_UART4_RXD	=	NC_SOC_AP_UART4_RXD	
7	NC_SOC_AP_UART4_TXD	=	NC_SOC_AP_UART4_TXD	
134 94 7	UART_TCON_D2R	=	UART_TCON_D2R	7 94 134
7	NC_SOC_AP_UART6_TXD	=	NC_SOC_AP_UART6_TXD	
7	UART_DP2HDMI_D2R	=	UART_DP2HDMI_D2R	80 117
7	UART_DP2HDMI_R2D	=	UART_DP2HDMI_R2D	80

NAND

134 91 7	NAND0_CLK24M0_R	=	NAND0_CLK24M0_R	7 91 134
134 91 7	NAND0_CLK24M1_R	=	NAND0_CLK24M1_R	7 91 134
134 91 90 89 7	NAND_BFH	=	NAND_BFH	7 89 90 91 134
7	NAND0_RESET0_L	=	NAND0_RESET0_L	91 130
7	NAND0_RESET1_L	=	NAND0_RESET1_L	91 130

MTP I2C

7	NC_SOC_MTP_I2C0_SCL	=	NC_SOC_MTP_I2C0_SCL	
7	NC_SOC_MTP_I2C0_SDA	=	NC_SOC_MTP_I2C0_SDA	

MTP SPI

134 109 7	SPI_IPD_MISO	=	SPI_IPD_MISO	7 109 134
134 14 7	SPI_IPD_MOSI_R	=	SPI_IPD_MOSI_R	7 14 134
134 14 7	SPI_IPD_CLK_R	=	SPI_IPD_CLK_R	7 14 134

MAKE_BASE=TRUE

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ALIASES SOC CSA 8

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AP I2S

135 14 8	TDM_SPKRAMP_L_BCLK_R	=	TDM_SPKRAMP_L_BCLK_R	8 14 135
135 131 8	TDM_SPKRAMP_L_D2R	=	TDM_SPKRAMP_L_D2R	8 131 135
135 14 8	TDM_SPKRAMP_L_R2D_R	=	TDM_SPKRAMP_L_R2D_R	8 14 135
135 14 8	TDM_SPKRAMP_L_FSYNC_R	=	TDM_SPKRAMP_L_FSYNC_R	8 14 135
8	NC_SOC_AP_I2S0_MCK	=	NC_SOC_AP_I2S0_MCK	
135 14 8	TDM_SPKRAMP_R_BCLK_R	=	TDM_SPKRAMP_R_BCLK_R	8 14 135
135 131 8	TDM_SPKRAMP_R_D2R	=	TDM_SPKRAMP_R_D2R	8 131 135
135 14 8	TDM_SPKRAMP_R_R2D_R	=	TDM_SPKRAMP_R_R2D_R	8 14 135
135 14 8	TDM_SPKRAMP_R_FSYNC_R	=	TDM_SPKRAMP_R_FSYNC_R	8 14 135
8	NC_SOC_AP_I2S1_MCK	=	NC_SOC_AP_I2S1_MCK	
135 14 8	TDM_CODEC_BCLK_R	=	TDM_CODEC_BCLK_R	8 14 135
135 115 101 8	TDM_CODEC_D2R	=	TDM_CODEC_D2R	8 101 115 135
135 14 8	TDM_CODEC_R2D_R	=	TDM_CODEC_R2D_R	8 14 135
135 14 8	TDM_CODEC_FSYNC_R	=	TDM_CODEC_FSYNC_R	8 14 135
8	NC_SOC_AP_I2S2_MCK	=	NC_SOC_AP_I2S2_MCK	
8	NC_TDM_SPKRAMP_TOP_BCLK_R	=	NC_TDM_SPKRAMP_TOP_BCLK_R	
8	NC_TDM_SPKRAMP_TOP_D2R	=	NC_TDM_SPKRAMP_TOP_D2R	
8	NC_TDM_SPKRAMP_TOP_R2D_R	=	NC_TDM_SPKRAMP_TOP_R2D_R	
8	NC_TDM_SPKRAMP_TOP_FSYNC_R	=	NC_TDM_SPKRAMP_TOP_FSYNC_R	
135 88 87 8	BT_TIME_SYNC	=	BT_TIME_SYNC	8 87 88 135

MAKE_BASE=TRUE

AP I2C

135 113 52 8	I2C_UPC_SCL	=	I2C_UPC_SCL	8 52 113 135
135 113 52 8	I2C_UPC_SDA	=	I2C_UPC_SDA	8 52 113 135
8	I2C_SPKRAMP_L_CODEC_SCL	=	I2C_SPKRAMP_L_CODEC_SCL	52
8	I2C_SPKRAMP_L_CODEC_SDA	=	I2C_SPKRAMP_L_CODEC_SDA	52
135 52 8	I2C_ATCRTMR_SCL	=	I2C_ATCRTMR_SCL	8 52 135
135 52 8	I2C_ATCRTMR_SDA	=	I2C_ATCRTMR_SDA	8 52 135
8	I2C_HDMI_SPKRAMP_R_SCL	=	I2C_HDMI_SPKRAMP_R_SCL	53 117 130
8	I2C_HDMI_SPKRAMP_R_SDA	=	I2C_HDMI_SPKRAMP_R_SDA	53 117 130
135 53 8	I2C_SD_DISP_BKLT_SCL	=	I2C_SD_DISP_BKLT_SCL	8 53 135
135 53 8	I2C_SD_DISP_BKLT_SDA	=	I2C_SD_DISP_BKLT_SDA	8 53 135

MAKE_BASE=TRUE

AP PWM

135 88 87 8	WLAN_TIME_SYNC	=	WLAN_TIME_SYNC	8 87 88 135
135 114 106 8	KBD_BKLT_PWM	=	KBD_BKLT_PWM	8 106 114 135
8	P3V8AON_ILIMIT_DIV_PULL_PWM	=	P3V8AON_ILIMIT_DIV_PULL_PWM	36

MAKE_BASE=TRUE

SPGIO

135 114 48 8	DBL_CLICK_DET	=	DBL_CLICK_DET	8 48 114 135
8	NC_SOC_SGPIO1	=	NC_SOC_SGPIO1	

MAKE_BASE=TRUE

AP SPI

135 8 4	BOOT_CONFIG2	=	BOOT_CONFIG2	4 8 135
135 8 4	BOOT_CONFIG1	=	BOOT_CONFIG1	4 8 135
135 8 4	BOOT_CONFIG0	=	BOOT_CONFIG0	4 8 135
13 8	SPI_SOCROM_IO1	=	SPI_SOCROM_IO1	
13 8	SPI_SOCROM_IO0	=	SPI_SOCROM_IO0	
135 14 8	SPI_SOCROM_CLK_R	=	SPI_SOCROM_CLK_R	8 14 135
135 13 8	SPI_SOCROM_CS_L	=	SPI_SOCROM_CS_L	8 13 135
135 111 8	SPI_TOUCHID_MISO	=	SPI_TOUCHID_MISO	8 111 135
135 14 8	SPI_TOUCHID_MOSI_R	=	SPI_TOUCHID_MOSI_R	8 14 135
135 14 8	SPI_TOUCHID_CLK_R	=	SPI_TOUCHID_CLK_R	8 14 135
8	NC_SOC_AP_SPI2_CS_L	=	NC_SOC_AP_SPI2_CS_L	
8	NC_SOC_AP_SPI3_MISO	=	NC_SOC_AP_SPI3_MISO	
8	NC_SOC_AP_SPI3_MOSI	=	NC_SOC_AP_SPI3_MOSI	
8	NC_SOC_AP_SPI3_SCLK	=	NC_SOC_AP_SPI3_SCLK	
8	NC_SOC_AP_SPI3_CS_L	=	NC_SOC_AP_SPI3_CS_L	
135 94 8	SPI_TCON_MISO	=	SPI_TCON_MISO	8 94 135
135 14 8	SPI_TCON_MOSI_R	=	SPI_TCON_MOSI_R	8 14 135
135 14 8	SPI_TCON_CLK_R	=	SPI_TCON_CLK_R	8 14 135
135 113 94 8	SPI_TCON_CS_L	=	SPI_TCON_CS_L	8 94 113 135
8	NC_SOC_AP_SPI5_MISO	=	NC_SOC_AP_SPI5_MISO	
8	NC_SOC_AP_SPI5_MOSI	=	NC_SOC_AP_SPI5_MOSI	
8	NC_SOC_AP_SPI5_SCLK	=	NC_SOC_AP_SPI5_SCLK	
8	NC_SOC_AP_SPI5_CS_L	=	NC_SOC_AP_SPI5_CS_L	

MAKE_BASE=TRUE

SEP I2C

135 13 8	I2C_SEEPROM_SCL	=	I2C_SEEPROM_SCL	8 13 135
135 13 8	I2C_SEEPROM_SDA	=	I2C_SEEPROM_SDA	8 13 135

MAKE_BASE=TRUE

SEP SPI

8	NC_SOC_SSPI0_MISO	=	NC_SOC_SSPI0_MISO	
8	NC_SOC_SSPI0_MOSI	=	NC_SOC_SSPI0_MOSI	
8	NC_SOC_SSPI0_SCLK	=	NC_SOC_SSPI0_SCLK	

MAKE_BASE=TRUE

THROTTLE

135 114 48 8	BUCK0_THERMAL_THROTTLE_L	=	BUCK0_THERMAL_THROTTLE_L	8 48 114 135
135 114 48 8	BUCK1_THERMAL_THROTTLE_L	=	BUCK1_THERMAL_THROTTLE_L	8 48 114 135
8	SPMU_VDDMAIN_UVWARN_L	=	SPMU_VDDMAIN_UVWARN_L	48 114
8	MPMU_VDDHI_UVWARN_L	=	MPMU_VDDHI_UVWARN_L	48 114
135 114 48 36 8	MPMU_VDDMAIN_UVWARN_L	=	MPMU_VDDMAIN_UVWARN_L	8 36 48 114 135

MAKE_BASE=TRUE

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ISP I2C

136 56 9	I2C_CAM_SCL	=	I2C_CAM_SCL	9 56 136	MAKE_BASE=TRUE
136 56 9	I2C_CAM_SDA	=	I2C_CAM_SDA	9 56 136	MAKE_BASE=TRUE
13 9	SPI_SOCROM_IO2	=	SPI_SOCROM_IO2		MAKE_BASE=TRUE
13 9	SPI_SOCROM_IO3	=	SPI_SOCROM_IO3		MAKE_BASE=TRUE

ISP GPIO

136 93 9	FTCAM_RESET_L	=	FTCAM_RESET_L	9 93 136	MAKE_BASE=TRUE
9	NC_SOC_ISP_GPIO_1	=	NC_SOC_ISP_GPIO_1		MAKE_BASE=TRUE
9	NC_SOC_ISP_GPIO_2	=	NC_SOC_ISP_GPIO_2		MAKE_BASE=TRUE
9	NC_SOC_ISP_GPIO_3	=	NC_SOC_ISP_GPIO_3		MAKE_BASE=TRUE

ISP SPMI

9	NC_SOC_ISP_SPMI0_SCLK	=	NC_SOC_ISP_SPMI0_SCLK	MAKE_BASE=TRUE
9	NC_SOC_ISP_SPMI0_SDATA	=	NC_SOC_ISP_SPMI0_SDATA	MAKE_BASE=TRUE
9	NC_SOC_ISP_SPMI1_SCLK	=	NC_SOC_ISP_SPMI1_SCLK	MAKE_BASE=TRUE
9	NC_SOC_ISP_SPMI1_SDATA	=	NC_SOC_ISP_SPMI1_SDATA	MAKE_BASE=TRUE

ISP CLK

9	NC_SOC_SENSOR0_CLK	=	NC_SOC_SENSOR0_CLK	MAKE_BASE=TRUE
9	NC_SOC_SENSOR1_CLK	=	NC_SOC_SENSOR1_CLK	MAKE_BASE=TRUE

MIPI

9	NC_SOC_MIPI0C_DPCLK	=	NC_SOC_MIPI0C_DPCLK	MAKE_BASE=TRUE
9	NC_SOC_MIPI0C_DNCLK	=	NC_SOC_MIPI0C_DNCLK	MAKE_BASE=TRUE
9	NC_SOC_MIPI0C_DPDATA<0>	=	NC_SOC_MIPI0C_DPDATA<0>	MAKE_BASE=TRUE
9	NC_SOC_MIPI0C_DNDATA<0>	=	NC_SOC_MIPI0C_DNDATA<0>	MAKE_BASE=TRUE
9	NC_SOC_MIPI0C_DPDATA<1>	=	NC_SOC_MIPI0C_DPDATA<1>	MAKE_BASE=TRUE
9	NC_SOC_MIPI0C_DNDATA<1>	=	NC_SOC_MIPI0C_DNDATA<1>	MAKE_BASE=TRUE
9	NC_MIPIC0_REXT	=	NC_MIPIC0_REXT	MAKE_BASE=TRUE

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LPDP RX AUX

10	NC_LPDP_FTCAM_AUX_C	NC_LPDP_FTCAM_AUX_C	
10	NC_SOC_LPDP_RX_AUX_D1	NC_SOC_LPDP_RX_AUX_D1	
10	NC_SOC_LPDP_RX_AUX_D2	NC_SOC_LPDP_RX_AUX_D2	
10	NC_SOC_LPDP_RX_AUX_D3	NC_SOC_LPDP_RX_AUX_D3	
10	NC_SOC_LPDP_RX_AUX_D4	NC_SOC_LPDP_RX_AUX_D4	
10	NC_SOC_LPDP_RX_AUX_D5	NC_SOC_LPDP_RX_AUX_D5	
10	NC_SOC_LPDP_RX_AUX_D6	NC_SOC_LPDP_RX_AUX_D6	
10	NC_SOC_LPDP_RX_AUX_D7	NC_SOC_LPDP_RX_AUX_D7	

MAKE_BASE=TRUE

LPDP RX DATA

137 92 10	LPDP_FTCAM_DATA_P<0>	LPDP_FTCAM_DATA_P<0>	10 92 137
137 92 10	LPDP_FTCAM_DATA_N<0>	LPDP_FTCAM_DATA_N<0>	10 92 137
10	NC_SOC_LPDP_RX_D1_P	NC_SOC_LPDP_RX_D1_P	
10	NC_SOC_LPDP_RX_D1_N	NC_SOC_LPDP_RX_D1_N	
10	NC_SOC_LPDP_RX_D2P	NC_SOC_LPDP_RX_D2P	
10	NC_SOC_LPDP_RX_D2N	NC_SOC_LPDP_RX_D2N	
10	NC_SOC_LPDP_RX_D3P	NC_SOC_LPDP_RX_D3P	
10	NC_SOC_LPDP_RX_D3N	NC_SOC_LPDP_RX_D3N	
10	NC_SOC_LPDP_RX_D4P	NC_SOC_LPDP_RX_D4P	
10	NC_SOC_LPDP_RX_D4N	NC_SOC_LPDP_RX_D4N	
10	NC_SOC_LPDP_RX_D5P	NC_SOC_LPDP_RX_D5P	
10	NC_SOC_LPDP_RX_D5N	NC_SOC_LPDP_RX_D5N	
10	NC_SOC_LPDP_RX_D6P	NC_SOC_LPDP_RX_D6P	
10	NC_SOC_LPDP_RX_D6N	NC_SOC_LPDP_RX_D6N	
10	NC_SOC_LPDP_RX_D7P	NC_SOC_LPDP_RX_D7P	
10	NC_SOC_LPDP_RX_D7N	NC_SOC_LPDP_RX_D7N	

MAKE_BASE=TRUE

LPDP RX RCAL

10	SOC_LPDP_RX0_RCAL_POS	SOC_LPDP_RX0_RCAL_POS	
10	SOC_LPDP_RX0_RCAL_NEG	SOC_LPDP_RX0_RCAL_NEG	
10	NC_SOC_LPDP_RX1_RCAL_POS	NC_SOC_LPDP_RX1_RCAL_POS	
10	NC_SOC_LPDP_RX1_RCAL_NEG	NC_SOC_LPDP_RX1_RCAL_NEG	
10	NC_SOC_LPDP_RX1_RCAL_NEG	NC_SOC_LPDP_RX1_RCAL_NEG	

MAKE_BASE=TRUE

LPDP TX

137 94 10	LPDP_INT_DATA_C_P<0>	LPDP_INT_DATA_C_P<0>	10 94 137
137 94 10	LPDP_INT_DATA_C_N<0>	LPDP_INT_DATA_C_N<0>	10 94 137
137 94 10	LPDP_INT_DATA_C_P<1>	LPDP_INT_DATA_C_P<1>	10 94 137
137 94 10	LPDP_INT_DATA_C_N<1>	LPDP_INT_DATA_C_N<1>	10 94 137
137 94 10	LPDP_INT_DATA_C_P<2>	LPDP_INT_DATA_C_P<2>	10 94 137
137 94 10	LPDP_INT_DATA_C_N<2>	LPDP_INT_DATA_C_N<2>	10 94 137
137 94 10	LPDP_INT_DATA_C_P<3>	LPDP_INT_DATA_C_P<3>	10 94 137
137 94 10	LPDP_INT_DATA_C_N<3>	LPDP_INT_DATA_C_N<3>	10 94 137
137 94 10	LPDP_INT_AUX_C_P	LPDP_INT_AUX_C_P	10 94 137
137 94 10	LPDP_INT_AUX_C_N	LPDP_INT_AUX_C_N	10 94 137
137 10	SOC_LPDP_INT_RCAL_NEG	SOC_LPDP_INT_RCAL_NEG	10 137
137 10	SOC_LPDP_INT_RCAL_NEG	SOC_LPDP_INT_RCAL_NEG	10 137

MAKE_BASE=TRUE

LPDP TX EXT

137 130 10	LPDP_DP2HDMI_DATA_C_P<0>	LPDP_DP2HDMI_DATA_C_P<0>	10 130 137
137 130 10	LPDP_DP2HDMI_DATA_C_N<0>	LPDP_DP2HDMI_DATA_C_N<0>	10 130 137
137 130 10	LPDP_DP2HDMI_DATA_C_P<1>	LPDP_DP2HDMI_DATA_C_P<1>	10 130 137
137 130 10	LPDP_DP2HDMI_DATA_C_N<1>	LPDP_DP2HDMI_DATA_C_N<1>	10 130 137
137 130 10	LPDP_DP2HDMI_DATA_C_P<2>	LPDP_DP2HDMI_DATA_C_P<2>	10 130 137
137 130 10	LPDP_DP2HDMI_DATA_C_N<2>	LPDP_DP2HDMI_DATA_C_N<2>	10 130 137
137 130 10	LPDP_DP2HDMI_DATA_C_P<3>	LPDP_DP2HDMI_DATA_C_P<3>	10 130 137
137 130 10	LPDP_DP2HDMI_DATA_C_N<3>	LPDP_DP2HDMI_DATA_C_N<3>	10 130 137
137 130 10	LPDP_DP2HDMI_AUX_C_P	LPDP_DP2HDMI_AUX_C_P	10 130 137
137 130 10	LPDP_DP2HDMI_AUX_C_N	LPDP_DP2HDMI_AUX_C_N	10 130 137
137 10	SOC_LPDP_DP2HDMI_RCAL_NEG	SOC_LPDP_DP2HDMI_RCAL_NEG	10 137
137 10	SOC_LPDP_DP2HDMI_RCAL_NEG	SOC_LPDP_DP2HDMI_RCAL_NEG	10 137

MAKE_BASE=TRUE

DISPLAY HPD

137 113 94 16 10	LPDP_INT_HPD	LPDP_INT_HPD	10 16 94 113 137
137 130 117 16 10	LPDP_DP2HDMI_HPD	LPDP_DP2HDMI_HPD	10 16 117 130 137

MAKE_BASE=TRUE

DISPLAY SPI

137 97 10	SPI_DISP_BKLT_MISO	SPI_DISP_BKLT_MISO	10 97 137
137 14 10	SPI_DISP_BKLT_MOSI_R	SPI_DISP_BKLT_MOSI_R	10 14 137
137 14 10	SPI_DISP_BKLT_CLK_R	SPI_DISP_BKLT_CLK_R	10 14 137
137 113 97 10	SPI_DISP_BKLT_CS_L	SPI_DISP_BKLT_CS_L	10 97 113 137

MAKE_BASE=TRUE

DISPLAY SPMI

137 14 10	SPMI_DISP_BKLT_CLK_R	SPMI_DISP_BKLT_CLK_R	10 14 137
137 14 10	SPMI_DISP_BKLT_DATA_R	SPMI_DISP_BKLT_DATA_R	10 14 137

MAKE_BASE=TRUE

DISPLAY

10	NC_SOC_DISP_POL	NC_SOC_DISP_POL	
	DISP_BKLT_FSYNC	DISP_BKLT_FSYNC	10 113 130
137 113 97 10	DISP_BKLT_LSYNC	DISP_BKLT_LSYNC	10 97 113 137
10	NC_SOC_DISP_TOUCH_BSYNC0	NC_SOC_DISP_TOUCH_BSYNC0	
10	NC_SOC_DISP_TOUCH_BSYNC1	NC_SOC_DISP_TOUCH_BSYNC1	
10	NC_SOC_DISP_TOUCH_EB	NC_SOC_DISP_TOUCH_EB	
10	BKLT_BOOST_THROTTLE_L	BKLT_BOOST_THROTTLE_L	16 114

MAKE_BASE=TRUE

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PCIE STORAGE

138 89 11	PCIE_NAND0_D2R_P<0>	=	PCIE_NAND0_D2R_P<0>	11 89 138	MAKE_BASE=TRUE
138 89 11	PCIE_NAND0_D2R_N<0>	=	PCIE_NAND0_D2R_N<0>	11 89 138	MAKE_BASE=TRUE
138 89 11	PCIE_NAND0_R2D_C_P<0>	=	PCIE_NAND0_R2D_C_P<0>	11 89 138	MAKE_BASE=TRUE
138 89 11	PCIE_NAND0_R2D_C_N<0>	=	PCIE_NAND0_R2D_C_N<0>	11 89 138	MAKE_BASE=TRUE
138 91 89 11	PCIE_CLK100M_NAND0_0_P	=	PCIE_CLK100M_NAND0_0_P	11 89 91 138	MAKE_BASE=TRUE
138 91 89 11	PCIE_CLK100M_NAND0_0_N	=	PCIE_CLK100M_NAND0_0_N	11 89 91 138	MAKE_BASE=TRUE
138 91 11	NAND0_CLKREQ0_L	=	NAND0_CLKREQ0_L	11 91 138	MAKE_BASE=TRUE
138 91 90 89 11	NAND0_PCIE_RESET_L	=	NAND0_PCIE_RESET_L	11 89 90 91 138	MAKE_BASE=TRUE
138 90 11	PCIE_NAND0_D2R_P<1>	=	PCIE_NAND0_D2R_P<1>	11 90 138	MAKE_BASE=TRUE
138 90 11	PCIE_NAND0_D2R_N<1>	=	PCIE_NAND0_D2R_N<1>	11 90 138	MAKE_BASE=TRUE
138 90 11	PCIE_NAND0_R2D_C_P<1>	=	PCIE_NAND0_R2D_C_P<1>	11 90 138	MAKE_BASE=TRUE
138 90 11	PCIE_NAND0_R2D_C_N<1>	=	PCIE_NAND0_R2D_C_N<1>	11 90 138	MAKE_BASE=TRUE
138 91 90 11	PCIE_CLK100M_NAND0_1_P	=	PCIE_CLK100M_NAND0_1_P	11 90 91 138	MAKE_BASE=TRUE
138 91 90 11	PCIE_CLK100M_NAND0_1_N	=	PCIE_CLK100M_NAND0_1_N	11 90 91 138	MAKE_BASE=TRUE
138 91 11	NAND0_CLKREQ1_L	=	NAND0_CLKREQ1_L	11 91 138	MAKE_BASE=TRUE

PCIE 0

138 87 11	PCIE_WLBT_D2R_P	=	PCIE_WLBT_D2R_P	11 87 138	MAKE_BASE=TRUE
138 87 11	PCIE_WLBT_D2R_N	=	PCIE_WLBT_D2R_N	11 87 138	MAKE_BASE=TRUE
138 87 11	PCIE_WLBT_R2D_C_P	=	PCIE_WLBT_R2D_C_P	11 87 138	MAKE_BASE=TRUE
138 87 11	PCIE_WLBT_R2D_C_N	=	PCIE_WLBT_R2D_C_N	11 87 138	MAKE_BASE=TRUE
138 87 11	PCIE_CLK100M_WLBT_P	=	PCIE_CLK100M_WLBT_P	11 87 138	MAKE_BASE=TRUE
138 87 11	PCIE_CLK100M_WLBT_N	=	PCIE_CLK100M_WLBT_N	11 87 138	MAKE_BASE=TRUE
138 88 87 11	WLBT_CLKREQ_L	=	WLBT_CLKREQ_L	11 87 88 138	MAKE_BASE=TRUE
138 88 87 11	WLBT_RESET_L	=	WLBT_RESET_L	11 87 88 138	MAKE_BASE=TRUE

PCIE 1

11	PCIE_SD_D2R_P	=	PCIE_SD_D2R_P	130	MAKE_BASE=TRUE
11	PCIE_SD_D2R_N	=	PCIE_SD_D2R_N	130	MAKE_BASE=TRUE
11	PCIE_SD_R2D_C_P	=	PCIE_SD_R2D_C_P	130	MAKE_BASE=TRUE
11	PCIE_SD_R2D_C_N	=	PCIE_SD_R2D_C_N	130	MAKE_BASE=TRUE
11	PCIE_CLK100M_SD_P	=	PCIE_CLK100M_SD_P	130	MAKE_BASE=TRUE
11	PCIE_CLK100M_SD_N	=	PCIE_CLK100M_SD_N	130	MAKE_BASE=TRUE
11	SD_CLKREQ_L	=	SD_CLKREQ_L	130	MAKE_BASE=TRUE
11	SD_RESET_L	=	SD_RESET_L	130	MAKE_BASE=TRUE

PCIE 2

11	NC_PCIE_USBHC_D2R_P	=	NC_PCIE_USBHC_D2R_P		MAKE_BASE=TRUE
11	NC_PCIE_USBHC_D2R_N	=	NC_PCIE_USBHC_D2R_N		MAKE_BASE=TRUE
11	NC_PCIE_USBHC_R2D_C_P	=	NC_PCIE_USBHC_R2D_C_P		MAKE_BASE=TRUE
11	NC_PCIE_USBHC_R2D_C_N	=	NC_PCIE_USBHC_R2D_C_N		MAKE_BASE=TRUE
11	NC_PCIE_CLK100M_USBHC_P	=	NC_PCIE_CLK100M_USBHC_P		MAKE_BASE=TRUE
11	NC_PCIE_CLK100M_USBHC_N	=	NC_PCIE_CLK100M_USBHC_N		MAKE_BASE=TRUE
11	NC_USBHC_CLKREQ_L	=	NC_USBHC_CLKREQ_L		MAKE_BASE=TRUE
11	NC_USBHC_RESET_L	=	NC_USBHC_RESET_L		MAKE_BASE=TRUE

PCIE 3

11	NC_SOC_GP_PCIE_RX3_P	=	NC_SOC_GP_PCIE_RX3_P		MAKE_BASE=TRUE
11	NC_SOC_GP_PCIE_RX3_N	=	NC_SOC_GP_PCIE_RX3_N		MAKE_BASE=TRUE
11	NC_SOC_GP_PCIE_TX3_P	=	NC_SOC_GP_PCIE_TX3_P		MAKE_BASE=TRUE
11	NC_SOC_GP_PCIE_TX3_N	=	NC_SOC_GP_PCIE_TX3_N		MAKE_BASE=TRUE
11	NC_SOC_GP_PCIE_CLK3_100M_P	=	NC_SOC_GP_PCIE_CLK3_100M_P		MAKE_BASE=TRUE
11	NC_SOC_GP_PCIE_CLK3_100M_N	=	NC_SOC_GP_PCIE_CLK3_100M_N		MAKE_BASE=TRUE
11	NC_SOC_GP_PCIE_CLKREQ_3_L	=	NC_SOC_GP_PCIE_CLKREQ_3_L		MAKE_BASE=TRUE
11	NC_SOC_GP_PCIE_PERST_3_L	=	NC_SOC_GP_PCIE_PERST_3_L		MAKE_BASE=TRUE

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ALIASES SOC CSA 12

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ATC0

139 67 12	USBC_ATC0_D2R_P<1>	=	USBC_ATC0_D2R_P<1>	MAKE_BASE=TRUE	12 67 139
139 67 12	USBC_ATC0_D2R_N<1>	=	USBC_ATC0_D2R_N<1>	MAKE_BASE=TRUE	12 67 139
139 67 12	USBC_ATC0_R2D_C_P<1>	=	USBC_ATC0_R2D_C_P<1>	MAKE_BASE=TRUE	12 67 139
139 67 12	USBC_ATC0_R2D_C_N<1>	=	USBC_ATC0_R2D_C_N<1>	MAKE_BASE=TRUE	12 67 139
139 67 12	USBC_ATC0_D2R_P<2>	=	USBC_ATC0_D2R_P<2>	MAKE_BASE=TRUE	12 67 139
139 67 12	USBC_ATC0_D2R_N<2>	=	USBC_ATC0_D2R_N<2>	MAKE_BASE=TRUE	12 67 139
139 67 12	USBC_ATC0_R2D_C_P<2>	=	USBC_ATC0_R2D_C_P<2>	MAKE_BASE=TRUE	12 67 139
139 67 12	USBC_ATC0_R2D_C_N<2>	=	USBC_ATC0_R2D_C_N<2>	MAKE_BASE=TRUE	12 67 139
139 69 12	USBC_ATC0_AUX_P	=	USBC_ATC0_AUX_P	MAKE_BASE=TRUE	12 69 139
139 69 12	USBC_ATC0_AUX_N	=	USBC_ATC0_AUX_N	MAKE_BASE=TRUE	12 69 139
130 12	CIO_ATC0_LSRX	=	CIO_ATC0_LSRX	MAKE_BASE=TRUE	67 130
130 12	CIO_ATC0_LSTX	=	CIO_ATC0_LSTX	MAKE_BASE=TRUE	67 130
139 130 16 12	EUSB_ATC0_P	=	EUSB_ATC0_P	MAKE_BASE=TRUE	12 16 130 139
139 130 16 12	EUSB_ATC0_N	=	EUSB_ATC0_N	MAKE_BASE=TRUE	12 16 130 139
139 117 12	DP_ATC0_HPD	=	DP_ATC0_HPD	MAKE_BASE=TRUE	12 117 139

ATC1

139 68 12	USBC_ATC1_D2R_P<1>	=	USBC_ATC1_D2R_P<1>	MAKE_BASE=TRUE	12 68 139
139 68 12	USBC_ATC1_D2R_N<1>	=	USBC_ATC1_D2R_N<1>	MAKE_BASE=TRUE	12 68 139
139 68 12	USBC_ATC1_R2D_C_P<1>	=	USBC_ATC1_R2D_C_P<1>	MAKE_BASE=TRUE	12 68 139
139 68 12	USBC_ATC1_R2D_C_N<1>	=	USBC_ATC1_R2D_C_N<1>	MAKE_BASE=TRUE	12 68 139
139 68 12	USBC_ATC1_D2R_P<2>	=	USBC_ATC1_D2R_P<2>	MAKE_BASE=TRUE	12 68 139
139 68 12	USBC_ATC1_D2R_N<2>	=	USBC_ATC1_D2R_N<2>	MAKE_BASE=TRUE	12 68 139
139 68 12	USBC_ATC1_R2D_C_P<2>	=	USBC_ATC1_R2D_C_P<2>	MAKE_BASE=TRUE	12 68 139
139 68 12	USBC_ATC1_R2D_C_N<2>	=	USBC_ATC1_R2D_C_N<2>	MAKE_BASE=TRUE	12 68 139
139 69 12	USBC_ATC1_AUX_P	=	USBC_ATC1_AUX_P	MAKE_BASE=TRUE	12 69 139
139 69 12	USBC_ATC1_AUX_N	=	USBC_ATC1_AUX_N	MAKE_BASE=TRUE	12 69 139
130 12	CIO_ATC1_LSRX	=	CIO_ATC1_LSRX	MAKE_BASE=TRUE	68 130
130 12	CIO_ATC1_LSTX	=	CIO_ATC1_LSTX	MAKE_BASE=TRUE	68 130
139 130 16 12	EUSB_ATC1_P	=	EUSB_ATC1_P	MAKE_BASE=TRUE	12 16 130 139
139 130 16 12	EUSB_ATC1_N	=	EUSB_ATC1_N	MAKE_BASE=TRUE	12 16 130 139
139 117 12	DP_ATC1_HPD	=	DP_ATC1_HPD	MAKE_BASE=TRUE	12 117 139

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DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculates dielectric distance from stackup. Shortest distance is used unless "X" is defined	EXAMPLE: 1,3-5,7C,9C-10C 2-12
A_DIELECTRIC_(N)XD_XV,XVL,X Calculates dielectric distance from hybrid table and stackup. Shortest distance is used unless "X" defined	EXAMPLE: 2-5V,7V,9VL,10VL,12 PLEASE USE HYBRID TABLE
A_DIELECTRIC_(N)XIN_(N)XOUT Calculates dielectric distance from stackup. Shortest distance is used unless "X" is defined	EXAMPLE: 2,4,6,8,10

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17.2 RULES

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CONFIG BOMS

BOM NUMBER	BOM NAME	BOM OPTIONS
639-16830	PCBA,MLB1,8GB,KX-512GB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:8G,X2482_NAND:512GB_KX
639-16865	PCBA,MLB1,16GB,KX-512GB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:16G,X2482_NAND:512GB_KX
639-16831	PCBA,MLB1,24GB,KX-512GB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:24G,X2482_NAND:512GB_KX
639-16832	PCBA,MLB1,8GB,WD-512GB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:8G,X2482_NAND:512GB_WD
639-16833	PCBA,MLB1,16GB,WD-512GB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:16G,X2482_NAND:512GB_WD
639-16834	PCBA,MLB1,24GB,WD-512GB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:24G,X2482_NAND:512GB_WD
639-16835	PCBA,MLB1,8GB,HY-512GB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:8G,X2482_NAND:512GB_HY
639-16836	PCBA,MLB1,16GB,HY-512GB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:16G,X2482_NAND:512GB_HY
639-16837	PCBA,MLB1,24GB,HY-512GB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:24G,X2482_NAND:512GB_HY
639-16838	PCBA,MLB1,8GB,KX-1TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:8G,X2482_NAND:1TB_KX
639-16839	PCBA,MLB1,16GB,KX-1TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:16G,X2482_NAND:1TB_KX
639-16840	PCBA,MLB1,24GB,KX-1TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:24G,X2482_NAND:1TB_KX
639-16841	PCBA,MLB1,8GB,WD-1TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:8G,X2482_NAND:1TB_WD
639-16842	PCBA,MLB1,16GB,WD-1TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:16G,X2482_NAND:1TB_WD
639-16843	PCBA,MLB1,24GB,WD-1TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:24G,X2482_NAND:1TB_WD
639-16844	PCBA,MLB1,8GB,HY-1TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:8G,X2482_NAND:1TB_HY
639-16845	PCBA,MLB1,16GB,HY-1TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:16G,X2482_NAND:1TB_HY
639-16846	PCBA,MLB1,24GB,HY-1TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:24G,X2482_NAND:1TB_HY
639-16847	PCBA,MLB1,8GB,KX-2TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:8G,X2482_NAND:2TB_KX
639-16848	PCBA,MLB1,16GB,KX-2TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:16G,X2482_NAND:2TB_KX
639-16849	PCBA,MLB1,24GB,KX-2TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:24G,X2482_NAND:2TB_KX
639-16850	PCBA,MLB1,8GB,WD-2TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:8G,X2482_NAND:2TB_WD
639-16851	PCBA,MLB1,16GB,WD-2TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:16G,X2482_NAND:2TB_WD
639-16852	PCBA,MLB1,24GB,WD-2TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:24G,X2482_NAND:2TB_WD
639-16853	PCBA,MLB1,8GB,HY-2TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:8G,X2482_NAND:2TB_HY
639-16854	PCBA,MLB1,16GB,HY-2TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:16G,X2482_NAND:2TB_HY
639-16855	PCBA,MLB1,24GB,HY-2TB,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:24G,X2482_NAND:2TB_HY

DEV BOMS

BOM NUMBER	BOM NAME	BOM OPTIONS
939-13976	PCBA,DEV,NO-CPU,N-SSD,X2482	ALT_CMN,ALTERNATE:PART,X2482_CMN_BOM,CPU:OFF,X2482_NAND:OFF

NOTE: SOME OF THESE ARE PLACEHOLDER 639'S
NAND TEAM HAS NOT COMMITTED TO ALL VENDORS FOR P1

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BOM VARIANT TABLES

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SOC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-30907	1	SOC,IBZ C0+8G,1Y,4C,BIN1,CX,H,M2565	U0600	CRITICAL	CPU:8G
998-30908	1	SOC,IBZ C0+16G,1Y,4C,BIN1,CX,H,M2565	U0600	CRITICAL	CPU:16G
998-30909	1	SOC,IBZ C0+24G,1Z,4C,BIN1,CX,H,M2565	U0600	CRITICAL	CPU:24G

SETTING HYNIX BIN 1 AS THE PRIMARY, ALL OTHERS WILL BE ALTS

EUSB LS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00902	2	IC,RTMR,CYUSB2402,A2,CSP24	UF600,UF650	CRITICAL	EUSB_LS:A2_OTP_CORV2
338S00908	2	IC,RTMR,CYUSB2402,A3,CSP24	UF600,UF650	CRITICAL	EUSB_LS:A3_OTP_CORV2

LFKA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-27476	2	IC,RTMR,B1,USB-C RETIMER,DEV,FCCSP154	UF000,UF100	CRITICAL	ATCRTMR:B1_DEV
338S00888	2	IC,RTMR,B1,USB-C RETIMER,ATK,FCCSP154	UF000,UF100	CRITICAL	ATCRTMR:B1_POR_ATK
338S00889	2	IC,RTMR,B1,USB-C RETIMER,SCK,FCCSP154	UF000,UF100	CRITICAL	ATCRTMR:B1_POR_SCK
338S00890	2	IC,RTMR,B1,USB-C RETIMER,ASE,FCCSP154	UF000,UF100	CRITICAL	ATCRTMR:B1_POR_ASE
998-30147	2	IC,LIFUKA,B2,USBC RETIMER,DEV,AXX,CSP154	UF000,UF100	CRITICAL	ATCRTMR:B2_DEV

UPC 0, UPC 1, UPC MAGSAFE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S02993	3	IC,ACE2,B3,USB PWR SW W/HV,ROM3,BGA123	U5500,UF400,UF500	CRITICAL	USBCPC:B3_ROM3

SPI ACE UPC0 PROGRAMMABLE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	UF260	CRITICAL	UPC01_ROM:BLANK_WINBOND
335S00537	1	IC,SPI SERIAL FLASH,8MBIT,2-3.6V,USON8	UF260	CRITICAL	UPC01_ROM:BLANK_MACRONIX
341S01914	1	ROM,ACE-P01 (VXXX) PROTO-1,X2211	UF260	CRITICAL	UPC01_ROM:FW_P1
341S02198	1	ROM,ACE-P01 (V3.016.0.1) PI-BU,X2482	UF260	CRITICAL	UPC01_ROM:FW_P1BU

MAGSAFE ACE PROGRAMMABLE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	U5560	CRITICAL	UPC5_ROM:BLANK_WINBOND
335S00537	1	IC,SPI SERIAL FLASH,8MBIT,2-3.6V,USON8	U5560	CRITICAL	UPC5_ROM:BLANK_MACRONIX
341S01892	1	ROM,ACE-P5 (V2.92.0.1) P-0,X2211	U5560	CRITICAL	UPC5_ROM:FW_V2P92P0P1
341S01924	1	ROM,ACE-P5 (V2.102.0.2) PROTO-1,X2211	U5560	CRITICAL	UPC5_ROM:FW_V2P102P0P2
341S02199	1	ROM,ACE-P5 (V3.016.0.1) P1-BU,X2482	U5560	CRITICAL	UPC5_ROM:FW_V3P016P0P1

SD CONNECTOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514-00196	1	CONN,RCPT,BLK,SD,X1982	JK600	CRITICAL	

HDMI CONNECTOR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
514S00510	1	CONN,RCPT,HDMI,BTN2,X2757	JH500	CRITICAL	

SPEAKERAMP DESENSE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S0852	2	CAP,CER,C0G,12PF,5%,25V,0201	CR610,CR611	CRITICAL	SPKRAMP_A_DESENSE
131S0852	2	CAP,CER,C0G,12PF,5%,25V,0201	CR640,CR641	CRITICAL	SPKRAMP_B_DESENSE
131S0852	2	CAP,CER,C0G,12PF,5%,25V,0201	CR670,CR671	CRITICAL	SPKRAMP_C_DESENSE
131S0852	2	CAP,CER,C0G,12PF,5%,25V,0201	CR710,CR711	CRITICAL	SPKRAMP_D_DESENSE
131S0852	2	CAP,CER,C0G,12PF,5%,25V,0201	CR740,CR741	CRITICAL	SPKRAMP_E_DESENSE
131S0852	2	CAP,CER,C0G,12PF,5%,25V,0201	CR770,CR771	CRITICAL	SPKRAMP_F_DESENSE

IPD SPI LS SERIES R

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S00113	2	RES,TK,20 OHM,5%,1/20W,0201	RT36B,RT352	CRITICAL	IPD_SPI_CS_R:20_OHM

IPD SPI SOC PULLUPS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S00129	5	RES,TK,47K OHM,5%,1/20W,0201	RT350,RT363,RT341,RT371	CRITICAL	TPAD_SOC_PULLUP:47K

IPD SPI SOC PULLUPS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00557	2	NFET,30V,440MA,1.2 OHM,DFN1006	Q5155,Q5270	CRITICAL	

SE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-23222	1	IC,SN300V,A0,SE,DEV,SW=TBD,WLCSP79	U5000	CRITICAL	SE:A0_DEV
338S00877	1	IC,SE,SN300V,B1,DEV,Y50,WLCSP79	U5000	CRITICAL	SE:B1_DEV
338S00878	1	IC,SE,SN300V,B1,PROD,RP0,WLCSP79	U5000	CRITICAL	SE:B1_PROD

SOC ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00574	1	IC,FLASH,64MBIT,1.2V,QE=1,W,4X4MM,SON8	U1900	CRITICAL	SOC_ROM:WINBOND
335S00575	1	IC,FLASH,64MBIT,1.2V,QE=1,W,4X4MM,SON8	U1900	CRITICAL	SOC_ROM:MACRONIX

RT13 ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00574	2	IC,FLASH,64MBIT,1.2V,QE=1,W,4X4MM,SON8	UF090,UF190	CRITICAL	RT13_ROM:WINBOND
335S00575	2	IC,FLASH,64MBIT,1.2V,QE=1,W,4X4MM,SON8	UF090,UF190	CRITICAL	RT13_ROM:MACRONIX

SPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-23585	1	IC,PMU,SPMU,CSP196	U7700	CRITICAL	SPMU:DEV
998-27998	1	IC,PMU,SPMU,A1,OTP-JPK,WLCSP196	U7700	CRITICAL	SPMU:A1_JPK
998-28583	1	IC,PMU,SPMU,A1,OTP-QPF,WLCSP196	U7700	CRITICAL	SPMU:A1_QPF
998-29292	1	IC,PMU,SPMU,A1,OTP-QPG,WLCSP196	U7700	CRITICAL	SPMU:A1_QPG
998-30156	1	IC,PMU,SPMU,A1,OTP-QPH,WLCSP196	U7700	CRITICAL	SPMU:A1_QPH
998-30827	1	IC,PMU,SPMU,A1,OTP-QPI,WLCSP196	U7700	CRITICAL	SPMU:A1_QPI

MPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-23524	1	IC,PMU,MPMU,CSP420	U8100	CRITICAL	MPMU:DEV
998-27997	1	IC,PMU,MPMU,A1,OTP-JPK,WLCSP420	U8100	CRITICAL	MPMU:A1_JPK
998-28446	1	IC,PMU,MPMU,A1,OTP-QPE,WLCSP420	U8100	CRITICAL	MPMU:A1_QPE
998-29291	1	IC,PMU,MPMU,A1,OTP-QPF,WLCSP420	U8100	CRITICAL	MPMU:A1_QPF
998-30382	1	IC,PMU,MPMU,A1,OTP-QPG,WLCSP420	U8100	CRITICAL	MPMU:A1_QPG
998-30826	1	IC,PMU,MPMU,A1,OTP-QPH,WLCSP420	U8100	CRITICAL	MPMU:A1_QPH
998-31309	1	IC,PMU,MPMU,A1,OTP-QPI,WLCSP420	U8100	CRITICAL	MPMU:A1_QPI

NAND0

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00552	1	NAND,BC5T,256GB,S5E,11.0,512G,K,ULGA315	UN000	CRITICAL	NAND0:256GB_KX
335S00553	1	NAND,BC5T,512GB,S5E,XX.X,512G,K,ULGA315	UN000	CRITICAL	NAND0:512GB_KX
335S00561	1	NAND,BC5T,1TB,S5E,XX.X,512G,K,MLGA315	UN000	CRITICAL	NAND0:1TB_KX
335S00620	1	NAND,BC5T,256GB,S5E,11.0,512G,W,ULGA315	UN000	CRITICAL	NAND0:256GB_WD
335S00550	1	NAND,BC5T,512GB,S5E,11.0.1,512G,W,LGA315	UN000	CRITICAL	NAND0:512GB_WD
335S00567	1	NAND,BC5ST,1024GB,S5E,11.0,512G,W,LGA315	UN000	CRITICAL	NAND0:1TB_WD
335S00581	1	NAND,3DV7T,256GB,S5E,XX.X,512G,H,ULGA315	UN000	CRITICAL	NAND0:256GB_HY
335S00583	1	NAND,3DV7T,512GB,S5E,XX.X,512G,H,ULGA315	UN000	CRITICAL	NAND0:512GB_HY
335S00610	1	NAND,3DV7T,1TB,S5E,XX.X,512G,H,MLGA315	UN000	CRITICAL	NAND0:1TB_HY

NAND1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00552	1	NAND,BC5T,256GB,S5E,11.0,512G,K,ULGA315	UN100	CRITICAL	NAND1:256GB_KX
335S00553	1	NAND,BC5T,512GB,S5E,XX.X,512G,K,ULGA315	UN100	CRITICAL	NAND1:512GB_KX
335S00561	1	NAND,BC5T,1TB,S5E,XX.X,512G,K,MLGA315	UN100	CRITICAL	NAND1:1TB_KX
335S00620	1	NAND,BC5T,256GB,S5E,11.0,512G,W,ULGA315	UN100	CRITICAL	NAND1:256GB_WD
335S00550	1	NAND,BC5T,512GB,S5E,11.0.1,512G,W,LGA315	UN100	CRITICAL	NAND1:512GB_WD
335S00567	1	NAND,BC5ST,1024GB,S5E,11.0,512G,W,LGA315	UN100	CRITICAL	NAND1:1TB_WD
335S00581	1	NAND,3DV7T,256GB,S5E,XX.X,512G,H,ULGA315	UN100	CRITICAL	NAND1:256GB_HY
335S00583	1	NAND,3DV7T,512GB,S5E,XX.X,512G,H,ULGA315	UN100	CRITICAL	NAND1:512GB_HY
335S00610	1	NAND,3DV7T,1TB,S5E,XX.X,512G,H,MLGA315	UN100	CRITICAL	NAND1:1TB_HY

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COMMON BOM GROUPS

BOM GROUP	BOM OPTIONS
X2482_COMMON_PARTS	SCH,PCB,ALT_CMN,COMMON,ALTERNATE:PART,X2482_DES,X2482_341,X2482_USB,X2482_PMU,X2482_BLC,X2482_PWR,X2482_HDMI,X2482_MISC,X2482_SOC,X2482_STRAPS
X2482_DES	SHIELD_LONG:YES,SHIELD_HDMI:YES,SHIELD_MPMU:YES,SHIELD_USBC:YES,SHIELD_VR:YES,SHIELD_BKLT:YES
X2482_341	HDMI_ROM:512,UPC01_ROM:FW_P1BU,UPC5_ROM:FW_V3P016P0P1
X2482_USB	ATCRTMR:B2_DEV,EUSB_LS:A3_OTP_CORV2,USBCPC:B3_ROM3,RT13_ROM:MACRONIX,USBC_DUAL_KIS:NO,LFKA_TEST_MODE:NO,ACE_WILL_BE_OTPED:YES
X2482_PMU	SPMU:A1_QPI,MPMU:A1_QPI,PMU_FB:FF,PMU_32K_CLK:XOSC,PMU_OTP_SEL:PD,PMU_OUT32K:WLBT,PMU_PBUS:BATT3S,PMU:PORTABLES
X2482_BLC	BLC_5V_SERIES:10_OHM,BLC_5V_CAP:4P7_UF
X2482_PWR	WHAMOLA:0A5-13V7,P3V8AON_IC:A2_R170,P3V8AON_LPM,BLC_BEN_IC:V4,5VS2TPS_VOUT:5V232,5V_DLY:YES,P5VUSB_DSCHG
X2482_HDMI	DATA_FILT,HDMI_CL_FILT:YES,LDO_HDMI:5V,COBRAPART:0,COBRA-A1_CGF2
X2482_MISC	CPU_SLEDS:YES,RF_CONN,SE:B1_DEV,REFIMU_IC:BMI286,SSD_2L,IPD_SPI_CS_R:20_OHM,REFSECDIS_SOC_PU:47K,REFIMU_RE400:47K,TPAD_SOC_PULLUP:47K
X2482_SOC	SOC_ROM:MACRONIX,DEV_DFU:TADFU
X2482_STRAPS	BOARD_ID_1,BOOT_CFG_2,BOOT_CFG_1,BOARD_REV_3,BOARD_REV_1,BOARD_REV_0

DEV BOM GROUPS

BOM GROUP	BOM OPTIONS
X2482_DEV_PARTS	ALT_CMN,X2482_DEV_GROUP1
X2482_DEBUG_PARTS	ALT_CMN,X2482_DEV_GROUP2
X2482_DEV_GROUP1	ALT_CMN,ALTERNATE:PART,USBC_DBG,BATT_DBG,CHGR_DBG,HDMI_DBG
X2482_DEV_GROUP2	GND_LOOP_TOP,GND_LOOP_BOT,SYS_DET_BTN_TOP,SYS_DET_BTN_BOT,DBG_LED,DEBUG_BUTTON

NAND BOM GROUPS

BOM GROUP	BOM OPTIONS
X2482_NAND:512GB_KX	NAND0:256GB_KX,NAND1:256GB_KX
X2482_NAND:512GB_WD	NAND0:256GB_WD,NAND1:256GB_WD
X2482_NAND:512GB_HY	NAND0:OFF,NAND1:OFF
X2482_NAND:1TB_KX	NAND0:512GB_KX,NAND1:512GB_KX
X2482_NAND:1TB_WD	NAND0:512GB_WD,NAND1:512GB_WD
X2482_NAND:1TB_HY	NAND0:OFF,NAND1:OFF
X2482_NAND:2TB_KX	NAND0:1TB_KX,NAND1:1TB_KX
X2482_NAND:2TB_WD	NAND0:1TB_WD,NAND1:1TB_WD
X2482_NAND:2TB_HY	NAND0:OFF,NAND1:OFF

SYSTEM PARTS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-07754	1	SCHEM,MLB	SCH	CRITICAL	SCH
820-02757	1	PCBF,MLB	PCB	CRITICAL	PCB
685-00444	1	COMMON PARTS,MLB	COMMON_PARTS	CRITICAL	X2482_CMN_BOM
985-01645	1	DEV PARTS,MLB	DEV_PARTS	CRITICAL	X2482_DEV_BOM
985-02058	1	DEBUG PARTS,MLB	DEBUG_PARTS	CRITICAL	X2482_DEBUG_BOM

COMMON PARTS BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00444	COMMON PARTS,MLB	X2482_COMMON_PARTS

DEV PARTS BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
985-01645	DEV PARTS,MLB	X2482_DEV_PARTS
985-02058	DEBUG PARTS,MLB	X2482_DEBUG_PARTS

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BOM GROUPS

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S00318	197S00323	ALT_CMN	ALL	<RDAR://73672537>
197S00335	197S00323	ALT_CMN	ALL	<RDAR://73672537>
197S00335	197S00323	ALT_CMN	ALL	<RDAR://98692335>
107S0276	107S00020	ALT_CMN	ALL	<RDAR://72344523>
197S0590	197S0591	ALT_CMN	ALL	<RDAR://74453590>
197S0588	197S0591	ALT_CMN	ALL	<RDAR://74453590>
376S00633	376S00294	ALT_CMN	ALL	<RDAR://99711250>
376S00292	376S00294	ALT_CMN	ALL	<RDAR://60290541>
740S00081	740S00053	ALT_CMN	ALL	<RDAR://74151268>
107S00365	107S00373	ALT_CMN	ALL	<RDAR://74150055>
311S00279	311S00285	ALT_CMN	ALL	<RDAR://60663112>
377S00210	377S00172	ALT_CMN	ALL	<RDAR://74149325>
311S00267	311S00244	ALT_CMN	ALL	<RDAR://74206523>
311S00269	311S00234	ALT_CMN	ALL	<RDAR://74206479>
138S00047	138S00073	ALT_CMN	ALL	<RDAR://74205854>
311S00268	311S00246	ALT_CMN	ALL	<RDAR://74206431>
377S00186	377S00060	ALT_CMN	ALL	<RDAR://74205815>
138S00049	138S0831	ALT_CMN	ALL	<RDAR://98076991>
138S00450	138S0831	ALT_CMN	ALL	<RDAR://98076991>
155S00097	155S0664	ALT_CMN	ALL	<RDAR://74205681>
155S0660	155S0513	ALT_CMN	ALL	<RDAR://74205441>
138S00229	138S00078	ALT_CMN	ALL	<RDAR://96318079>
138S00107	138S00078	ALT_CMN	ALL	<RDAR://96318079>
138S00104	138S0978	ALT_CMN	ALL	<RDAR://74203696>
107S0150	107S00460	ALT_CMN	ALL	<RDAR://74203571>
107S00298	107S00460	ALT_CMN	ALL	<RDAR://74203571>
353S02402	353S1429	ALT_CMN	ALL	<RDAR://74203527>
353S02897	353S1429	ALT_CMN	ALL	<RDAR://76782934>
377S00166	377S00160	ALT_CMN	ALL	<RDAR://74203284>
376S00632	376S0820	ALT_CMN	ALL	<RDAR://99663002>
132S00229	132S00010	ALT_CMN	ALL	<RDAR://74371419>
138S0852	138S0818	ALT_CMN	ALL	<RDAR://74371364>
138S00097	138S0750	ALT_CMN	ALL	<RDAR://74371277>
311S00392	311S00129	ALT_CMN	ALL	<RDAR://91058082>
376S00224	376S00557	ALT_CMN	ALL	<RDAR://104655122>
353S00878	353S00599	ALT_CMN	ALL	<RDAR://74371021>
138S00332	138S00328	ALT_CMN	ALL	<RDAR://74370983>
138S00416	138S00328	ALT_CMN	ALL	<RDAR://75630410>
371S00325	371S00085	ALT_CMN	ALL	<RDAR://84307925>
107S00101	107S00005	ALT_CMN	ALL	<RDAR://74370853>
377S0155	377S0184	ALT_CMN	ALL	<RDAR://74370211>
128S00058	128S00098	ALT_CMN	ALL	<RDAR://74043733>
128S00105	128S00098	ALT_CMN	ALL	<RDAR://74043733>
138S00385	138S00377	ALT_CMN	ALL	<RDAR://74041033>
107S00021	107S0284	ALT_CMN	ALL	<RDAR://79745917>
377S00123	377S00031	ALT_CMN	ALL	<RDAR://79886515>
377S00223	377S00040	ALT_CMN	ALL	<RDAR://76766041>
353S02434	353S3332	ALT_CMN	ALL	<RDAR://89779783>
155S0694	155S0387	ALT_CMN	ALL	<RDAR://74205389>
152S00785	152S00477	ALT_CMN	ALL	<RDAR://90732212>
138S0734	138S0838	ALT_CMN	ALL	<RDAR://90732045>
155S00737	155S0921	ALT_CMN	ALL	<RDAR://90731647>
371S00322	371S00047	ALT_CMN	ALL	<RDAR://90858680>
371S00370	371S00062	ALT_CMN	ALL	<RDAR://90858827>
353S02787	353S01211	ALT_CMN	ALL	<RDAR://90858464>
311S00271	311S00286	ALT_CMN	ALL	<RDAR://90857233>
311S00310	311S00306	ALT_CMN	ALL	<RDAR://98348196>
107S00076	107S00044	ALT_CMN	ALL	<RDAR://90655976>
107S00233	107S00232	ALT_CMN	ALL	<RDAR://90657059>
155S00754	155S00098	ALT_CMN	ALL	<RDAR://90802448>

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00330	138S00081	ALT_CMN	ALL	<RDAR://74370168>
311S00254	311S00245	ALT_CMN	ALL	<RDAR://74370093>
107S00094	107S00109	ALT_CMN	ALL	<RDAR://74151209>
371S00220	371S00307	ALT_CMN	ALL	<RDAR://74443357>
132S00176	132S0640	ALT_CMN	ALL	<RDAR://74443234>
740S0118	740S00028	ALT_CMN	ALL	<RDAR://74443626>
740S0144	740S00028	ALT_CMN	ALL	<RDAR://74443626>
138S00148	138S00149	ALT_CMN	ALL	<RDAR://74041065>
138S00151	138S00149	ALT_CMN	ALL	<RDAR://74041065>
138S00150	138S00149	ALT_CMN	ALL	<RDAR://74041065>
311S00335	311S00155	ALT_CMN	ALL	<RDAR://75317754>
311S00360	311S00362	ALT_CMN	ALL	<RDAR://81722614>
107S00479	107S00478	ALT_CMN	ALL	<RDAR://83504734>
138S00181	138S0835	ALT_CMN	ALL	<RDAR://87353192>
138S00291	138S0835	ALT_CMN	ALL	<RDAR://87353192>
155S00648	155S00647	ALT_CMN	ALL	<RDAR://87353138>
353S00636	353S03251	ALT_CMN	ALL	<RDAR://90774958>
353S4037	353S03251	ALT_CMN	ALL	<RDAR://90774958>
353S03294	353S03251	ALT_CMN	ALL	<RDAR://90774958>
128S00119	128S00016	ALT_CMN	ALL	<RDAR://90815715>
152S01787	152S00285	ALT_CMN	ALL	<RDAR://97746187>
107S00041	107S00039	ALT_CMN	ALL	<RDAR://90655855>
353S03084	353S02407	ALT_CMN	ALL	<RDAR://91010156>
116S00014	116S00044	ALT_CMN	ALL	<RDAR://90657244>
311S00322	311S00321	ALT_CMN	ALL	<RDAR://90858060>
138S1103	138S0719	ALT_CMN	ALL	<RDAR://90729967>
138S00167	138S00237	ALT_CMN	ALL	<RDAR://90729810>
131S00213	131S0556	ALT_CMN	ALL	<RDAR://90729348>
138S0772	138S00013	ALT_CMN	ALL	<RDAR://90729647>
138S00022	138S00020	ALT_CMN	ALL	<RDAR://90729709>
353S02175	353S00882	ALT_CMN	ALL	<RDAR://90858310>
155S0830	155S0316	ALT_CMN	ALL	<RDAR://90802613>
152S00343	152S01325	ALT_CMN	ALL	<RDAR://91758662>
353S01655	353S03149	ALT_CMN	ALL	<RDAR://94767306>
311S00385	311S00323	ALT_CMN	ALL	<RDAR://94764663>
138S00124	138S00123	ALT_CMN	ALL	<RDAR://94762897>
197S00374	197S00375	ALT_CMN	ALL	<RDAR://95641294>
197S00371	197S00375	ALT_CMN	ALL	<RDAR://95641294>
311S0341	311S0536	ALT_CMN	ALL	<RDAR://64195790>
335S00603	335S0915	ALT_CMN	ALL	<RDAR://99408427>
155S00309	155S0831	ALT_CMN	ALL	<RDAR://90856828>
311S00405	311S0665	ALT_CMN	ALL	<RDAR://91780028>
353S03028	353S01211	ALT_CMN	ALL	<RDAR://101148863>
376S00631	376S0636	ALT_CMN	ALL	<RDAR://98790874>

DCDC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00979	152S00874	ALT_CMN	ALL	<RDAR://71851492>
138S00164	138S00138	ALT_CMN	ALL	<RDAR://74151613>
138S00280	138S00138	ALT_CMN	ALL	<RDAR://74151613>
138S00139	138S00138	ALT_CMN	ALL	<RDAR://74151613>
107S00055	107S00090	ALT_CMN	ALL	<RDAR://74151396>
376S00303	376S00012	ALT_CMN	ALL	<RDAR://74423676>
128S00069	128S00094	ALT_CMN	ALL	<RDAR://89473596>
128S00131	128S00094	ALT_CMN	ALL	<RDAR://92423680>
128S00026	128S00011	ALT_CMN	ALL	<RDAR://74428451>
128S00031	128S00011	ALT_CMN	ALL	<RDAR://74428451>
128S00132	128S00011	ALT_CMN	ALL	<RDAR://100460472>
128S00039	128S00038	ALT_CMN	ALL	<RDAR://74424316>
152S00398	152S00204	ALT_CMN	ALL	<RDAR://74426184>
376S1147	376S00281	ALT_CMN	ALL	<RDAR://74425029>
152S01788	152S00182	ALT_CMN	ALL	<RDAR://97746618>
152S01836	152S01268	ALT_CMN	ALL	<RDAR://102913705>
152S01494	152S01263	ALT_CMN	ALL	<RDAR://74426334>
152S01378	152S01283	ALT_CMN	ALL	<RDAR://74754401>
152S01461	152S01283	ALT_CMN	ALL	RDAR://92424119
152S00367	152S01248	ALT_CMN	ALL	<RDAR://74751850>
152S01452	152S01248	ALT_CMN	ALL	<RDAR://74751850>
152S01789	152S00265	ALT_CMN	ALL	<RDAR://97746866>
138S00284	138S00136	ALT_CMN	ALL	<RDAR://79783536>
138S00413	138S00410	ALT_CMN	ALL	<RDAR://79784459>
138S00343	138S00329	ALT_CMN	ALL	<RDAR://79783647>
138S1065	138S1058	ALT_CMN	ALL	<RDAR://81275265>
152S00991	152S00984	ALT_CMN	ALL	<RDAR://84171872>
152S00199	152S01218	ALT_CMN	ALL	<RDAR://90732304>
376S00600	376S0761	ALT_CMN	ALL	<RDAR://90859030>
376S00614	376S0761	ALT_CMN	ALL	<RDAR://90859030>
376S00521	376S00519	ALT_CMN	ALL	<RDAR://91254625>
131S00691	131S00365	ALT_CMN	ALL	<RDAR://90728912>
376S00516	376S00544	ALT_CMN	ALL	<RDAR://85838031>
376S00618	376S00544	ALT_CMN	ALL	<RDAR://99302290>

BACKLIGHT

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S00093	128S00009	ALT_CMN	ALL	<RDAR://72858503>
128S00103	128S00009	ALT_CMN	ALL	<RDAR://72858503>
138S00087	138S1086	ALT_CMN	ALL	<RDAR://72858503>
138S00482	138S1086	ALT_CMN	ALL	<RDAR://100740141>
152S00812	152S1701	ALT_CMN	ALL	<RDAR://72858503>
371S00217	371S00079	ALT_CMN	ALL	<RDAR://72858503>
376S00021	376S00263	ALT_CMN	ALL	<RDAR://89109299>
376S00328	376S00263	ALT_CMN	ALL	<RDAR://89109299>

RT13 AND SOC ROM ALTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00574	335S00575	ALT_CMN	ALL	<RDAR://83987581>

RT13 VR/COBRA DISCHARGER FET ALTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00588	376S00078	ALT_CMN	ALL	<RDAR://87561915>
376S00647	376S00078	ALT_CMN	ALL	<RDAR://100511122>
376S00634	376S00078	ALT_CMN	ALL	<RDAR://100511122>

RT13 VR/COBRA DISCHARGER REQUIRES LOWER DCR

NON RT13 VR DISCHARGER FET ALTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S00078	376S00074	ALT_CMN	ALL	<RDAR://87561676>
376S00588	376S00074	ALT_CMN	ALL	<RDAR://87561676>
376S00332	376S00074	ALT_CMN	ALL	<RDAR://87561676>
376S00634	376S00074	ALT_CMN	ALL	<RDAR://99353418>
376S00647	376S00074	ALT_CMN	ALL	<RDAR://99353418>

NON RT13 VR DISCHARGER CAN TOLERATE HIGHER DCR SO MORE ALTS

SOC ALTS - 8GB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-30910	998-30907	ALT_CMN	ALL	<RDAR://90316327>

SOC ALTS - 16GB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-30911	998-30908	ALT_CMN	ALL	<RDAR://90316327>

SOC ALTS - 24GB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
998-30912	998-30909	ALT_CMN	ALL	<RDAR://90316327>

BOM_COST_GROUP=NO CATEGORY

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REF_SOC_H15G

PACK_OPTIONS TO INCLUDE IN NETLIST
PCIE_GP0
PCIE_GP1
LPDP_INT_RCAL
LPDP_EXT
LPDPRX0_RCAL

REF_CHARGER_WHAMOLA_MP_NEWFET

PACK_OPTIONS TO INCLUDE IN NETLIST
5V_DELAY:YES
CHGR_MLCC-STD
CHGR_PBUS16V_33UF
3V8_PWR_EN_LS_THICKSTNCL
5V_DELAY_YES_U5350:THICK_STNCL

REF_MAGSAFE_ACE2_20V

PACK_OPTIONS TO INCLUDE IN NETLIST
MAGSAFE_ACE_UPC_DBG:SMALL

REF_VR_ICEMAN

PACK_OPTIONS TO INCLUDE IN NETLIST
3V8_AON_PBUS-B12
3V8_INDUCTOR:2P4MM
3V8_AON_MLCC-LN
3V8_AON_LG_R:YES
3V8_AON_CTRL_PKG:QFN_THICKSTENCIL

REF_PMU_STOWE_VALE

PACK_OPTIONS TO INCLUDE IN NETLIST
PMU_32K_XOSC
PMU_SYSALIVE_LS
PMU_PORTABLES
PMU_LDO2
PMU_CHGR_RESET
BUCK5_LOCAL_CAPS
BUCK8_LOCAL_CAPS
BUCK14_LOCAL_CAPS
PMU_32K_WLBT
BUCK6_RMT
PMU_LDO10
PBUS_SNS:OPA333
PMU_WLBT_IPD_32K

REF_VR_5V_TPS62130

PACK_OPTIONS TO INCLUDE IN NETLIST
5VS2TPS_PBUS-B12
5VS2TPS_THINSTNCL

REF_IMU_SOVEREIGN

PACK_OPTIONS TO INCLUDE IN NETLIST
REFIMU_VDD:LCFILT
REFIMU_TP:P5MM
REFIMU_TEST:NO

REF_BLC_LUXE

PACK_OPTIONS TO INCLUDE IN NETLIST

POLY_PBUS:16V (FROM SD REF DESIGN)

REF_USBC_LFKA_MACAW_DUAL_KIS

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_SPI_UPC0
USBC_LAPTOP
PKGS:SMALL_PITCH
KEEP_SMALL_ARKANOID_CONN
ACE2_SS_CAP
ACTIVE_READY:LARGE_PITCH
DUAL_KIS:YES
INV:SON
TADFU:YES
ATC_RTMR_ROM:XSON
ATC_PU_PD:YES
USBC_GATE_PACKAGE:SOT
ATC_BOUNDARYSCAN:YES

REF_USBC_VR_LT8642_1

PACK_OPTIONS TO INCLUDE IN NETLIST
5VUSBC01_PBUS-B12
5VUSBC01_THICKSTNCL
5VUSBC01_AND:PP

REF_SDCARD_GL9755_V2

PACK_OPTIONS TO INCLUDE IN NETLIST
SD_VR_3V3:THICKSTNCL
POLY_PBUS:16V

PKGS:SMALL_PITCH (FROM USB REF DESIGN)

REF_HDMI_COBRA

PACK_OPTIONS TO INCLUDE IN NETLIST
HDMICONN:PORT
HDMI14UF:NORM
HDMI_SAK:INSTALL
HDMI_SAK:BYPASS

REF_WIRELESS_WILLAMETTE

PACK_OPTIONS TO INCLUDE IN NETLIST
SUNWAY
3X_ANTENNA

REF_SPKRAMP_SN012776

PACK_OPTIONS TO INCLUDE IN NETLIST
SPKRAMP_A
SPKRAMP_B
SPKRAMP_C
SPKRAMP_D
SPKRAMP_E
SPKRAMP_F
SPKRAMP_ICC_GB

TOUCHID

PACK_OPTIONS TO INCLUDE IN NETLIST

PKGS:SMALL_PITCH (FROM USB REF DESIGN)

REF_TPAD_IF_PKG_LARGE

PACK_OPTIONS TO INCLUDE IN NETLIST
IPD_TOUCH_CLK_SRC:TPAD
IPD_RESETS_LS:LVL_SHIFTER
IPD_MCU_INT_WAKE_LS:SOT
IPD_WAKE_PU_EN
IPD_PACK_MTP_FUNC1_CIRCUIT
IPD_PACK_MTP_FUNC1_FLEX:PULLUP

PAGE TITLE: PACK OPTIONS

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REVISION: 6.0.0
BRANCH: dvt-1
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PIN DELAY MAPPING FILE	
REFERENCE DESIGNATOR	PIN DELAY CSV FILE NAME
UF000	2020_12_28_usbc_ballmap_spec_v0p5_pin_delay_v1_uf000_fe.csv
UF100	2020_12_28_usbc_ballmap_spec_v0p5_pin_delay_v1_uf100_fe.csv
U0600	2022_04_06_SOC_BALLMAP_SPEC_0V15_PIN_DELAY_V5.CSV

<RDAR://72706458>
<RDAR://72706458>
<RDAR://91220094>

PAGE TITLE
PIN DELAYS

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I2C PULL UP WAIVERS

114 110 107 IN — CKPLUS_WAIVE=I2C_PULLUP — I2C_KBD_SCL

114 110 107 BI — CKPLUS_WAIVE=I2C_PULLUP — I2C_KBD_SDA

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CHECKPLUS SUPPORT

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